行政院國家科學委員會補助專題研究計畫成果報告

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※　　奈米 CMOS 高頻與類比元件模型研發　　※
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奈米 CMOS 高頻與類比元件模型研發(3/3)
Nanoscale CMOS RF and Analog Device Modeling

計畫編號：NSC 96-2221-E009-186
執行期間（第三年）：96年08月01日 至 97年07月31日
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一、 中文摘要

近年來奈米 CMOS 技術之精進帶來積體電路應用之新紀元，主要優點除了高速，尚有高密度與低成本適於系統單晶片設計與製造。其中，奈米 MOSFET 之訊號傳輸效能可高達 f_T>100GHz，成為高頻電路之關鍵元件，然而高頻雜訊成為一重要問題必須克服。尤以奈米元件於矽晶片上執行高頻操作時，矽基板與傳輸線偶合效應導致嚴重而複雜之雜訊問題。本三年期計畫之前二年已完成一套精準的損耗矽基板模型(lossy substrate model)，可正確地模擬 80-65 奈米元件量到的雜訊參數，並萃取元件內在的高頻雜訊。當元件由 80 奈米微縮至 65 奈米，其本質雜訊在 10 GHz 時可減少約 0.2 dB (0.7 dB 降至 0.5 dB)。如此低的高頻雜訊表明奈米元件於高頻電路應用之優點，亦證明 lossy substrate model 在低雜訊與低功率射頻電路方面之應用價值。

根據此 model 得知 GSG 探針墊(pad)與傳輸線(TML)於矽基板之積體電路中，乃是額外雜訊(excess noise)之主要來源，其影響隨著元件微縮而急遽增加，於小尺寸(finger number N and width W_F)之奈米元件，往往超過元件本質雜訊，而嚴重劣化高頻電路效能。因此如何有效抑制此額外雜訊成為本計畫進一步努力目標。此第三年計畫完成各式結構之高頻雜訊遮蔽法(RF noise shielding method)，並建立相對應之等效電路模型，可成功模擬高頻雜訊遮蔽法對於奈米元件之影響。此等效電路模型乃以 lossy substrate model 為基礎，而根據探針墊、傳輸線與雜訊遮蔽結構作適當修改，稱為 extended lossy substrate model。本計畫已將各式高頻雜訊遮蔽法建立於雙埠高頻測試鍵(two-port test key)，其中含奈米 MOSFET 為 DUT (device under test)。一理想之高頻雜訊遮蔽法可以完全抑制額外雜訊，不需要繁複的雜訊去寄生程序(noise deembedding process)，而直接量到元件本質雜訊參數。此高頻雜訊遮蔽法可以降低實部最佳雜訊阻抗($Re(Y_{opt})$)而使最小雜訊參數(NF_{min})降低但是雜訊電阻(Rn)值幾乎不隨著探針墊架構而改變，根據 extended lossy substrate model 可以準確地預測此雜訊遮蔽法的影響與物理機制，另一方面，一個值得探討的問題是，雖然此高頻遮蔽法可以有效的遮蔽經由矽基板損耗所貢獻的外在雜訊使雜訊減低，但是會使探針墊的寄生電容大幅增加，進而導致 f_T 降低與 NF_{50} 增加。

Abstract:

The advancement of CMOS technology to nanoscale regime has driven MOSFET f_T to super-100GHz and makes RF CMOS an attractive technology in realizing high frequency communication ICs due to the advantages of high speed, high integration and low cost. The nanoscale CMOS devices become a key element in RF ICs, attributed to the features of high speed and easy integration with standard logic circuits. However, the abnormally large RF noises measured from sub-100nm MOSFETs with miniaturized dimensions emerges as a critical concern in RF circuit design and fabrication using nanoscale CMOS technology. In our previous work, a lossy substrate model was developed, which can accurately simulate measured RF noise in sub-100 nm MOSFETs with various N and W_F. Furthermore, the intrinsic RF noise can be extracted easily and precisely by the lossy substrate de-embedding using circuit simulation. The extracted intrinsic NF_{min} at 10 GHz can be pushed to as low as 0.5 dB for 65nm nMOS that is around 0.2 dB lower than 80nm counterpart. The results suggest the advantages of aggressive gate length scaling to sub-100nm regime.

The successful prediction from lossy substrate model for measured noise suggests that most of the excess noises were contributed from the lossy substrate coupled through GSG pads and TML. What's worse, the excess noises increase dramatically with device miniaturization and dominate the intrinsic noise, as a major factor responsible for the degradation of RF circuit performance. As a result, an effective noise shielding method for suppressing RF noise in nanoscale devices becomes a major subject worthy of extensive research effort. In this third year project, RF noise shielding methods with various structures were implemented and the corresponding equivalent circuit models were developed for simulating noise shielding effect on nanoscale devices. Note that, the equivalent

circuit models, so called extended lossy substrate models were built based on the original lossy substrate model plus a relevant modification according to the structures of pads, TML, and shielding features. In this work, pad and TML shielding features were fabricated in two port test structures incorporating nanoscale devices. The ultimate goal is to fully eliminate excess noises and measure the intrinsic noise, without resort to the complicated noise deembedding process. The noise shielding method can effectively reduce NF_{min} due to suppression of $Re(Y_{opt})$ but noise resistance (R_n) is kept nearly the same. An impact of awareness is the increase of parasitic capacitance from the shielding structures will lead to degradation of f_T and NF_{50}. The results provide an important insight and guideline for low noise RF circuit design.The extended lossy substrate model can predict noise shielding effect and explain the underlying mechanisms.

I. Introduction

Noise coupling through Si substrate has been a critical killer in mixed signal IC with digital and analog circuits on a single chip. To overcome this failure mechanism, many works have been done on substrate noise isolation techniques, such as heavily doped guard ring (GR), triple well, and deep trench **[1-3]**. However, the noise isolation capability of the mentioned methods is generally limited to few GHz [3] and become ineffective in advanced RF CMOS circuits with operating frequency driven by nanoscale technology to well beyond 10 GHz. Besides, most of the characterization and analysis focused on the isolation between two features like port-to-port, pad-to-pad, or device-to-device isolation in terms of $|S_{12}|$ but quite few research results are available for a systematic study of shielding effect on RF noise in miniaturized devices. A ground shielded bond pad structure was proposed and fabricated in Si bipolar technology **[4]**. A significant improvement over pad-to-pad isolation ($|S_{12}|$) and suppression on LNA noise figure (NF) was presented. The experimental results prove the ground shielding effect on isolation ($|S_{12}|$), gain ($|S_{21}|$), and noise (NF). However, a simple resistance model was assumed and implemented to simulate the substrate coupling effect. This simplified model may be valid at sufficiently low frequency ($\leqq$10 GHz) but is no longer accurate to fit high frequency domain up to tens of GHz. An investigation through a serious comparison between electroquasistatic (EQS) and electrodynamic (ED) models **[5]** indicates that the simple RC model is no longer valid in higher frequency well above 10GHz and suggests an inductive like characteristics in noise propagation through the substrate. Unfortunately, the EM analysis in this approach requires complicated computation and extensive memory, and is not suitable for circuit simulations. All the mentioned challenges trigger our motivation of this work.

In our previous work, a lossy substrate model in an equivalent circuit form has been developed to accurately predict the RF noise measured from sub-100 nm MOSFETs under high frequency up to 18 GHz **[6-8]**. The substrate RLC networks, for the first time proposed in our original model, incorporating inductive impedance together with RC networks can simulate the substrate noise coupling through the pad and transmission line (TML) with a broadband accuracy and scalability over different pad structures and TML topologies **[9]**. In this report, we will present that the original lossy substrate model for standard structure without shielding can be easily extended for those with shielding to predict the influence on high frequency S-parameters and noise parameters. An interesting result with an opposite trend in minimum noise figure (NF_{min}) and 50Ω noise figure (NF_{50}) will be discussed.

II. RF Noise Shielding Structure Design and Extended Lossy Substrate Model

100 nm RF n-MOSFETs with multi-gate-finger structures were fabricated in tsmc 0.13um RF CMOS process (T13-RF). The finger widths and finger numbers were varied simultaneously (W/N=4μm/6, 2μm/12, 1μm/24) under a fixed total width W_{tot}=WxN=24μm to investigate the trade-off between gate resistance (R_g) and capacitances. The smaller W and larger N can reduce R_g but increase parasitic capacitances at gate terminal. The former one can help suppress gate induced excess noise. Unfortunately, the later one generally degrades f_T due to increased gate capacitances and may overwhelm the advantage of smaller R_g. In this report, W/N=4μm/6 is selected due to the best high frequency performance represented by highest f_T. Note that W_{tot}=24μm is a relatively small dimension selected for achieving lower current and low power, but taking a trade-off with lower g_m and higher noise resistance (R_n), and raised challenge to low noise design.

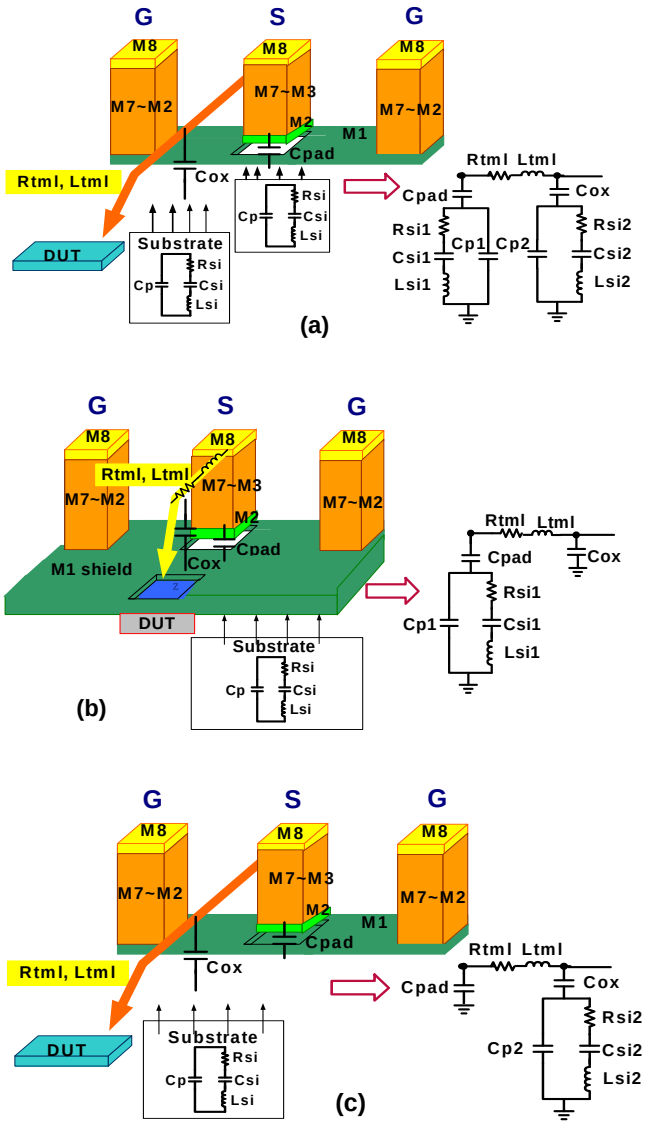

Fig. 1 3D RF test structures with different shielding schemes (a) standard without shielding (b) TML shielding (c)pad shielding, and the corresponding equivalent circuit model.

Two different shielding schemes were implemented as RF noise shielding methods in miniaturized devices for low noise RF CMOS design. 0.13μm BEOL process with 8 layers of Cu and FSG as IMD was used to fabricate the noise shielding structures. G-pads for grounding were constructed with stacked metals from M1 to M8. S-pads for signal supply were built from M2 to M8, i.e. stacked metals excluding M1. The preserved M1 is employed as the noise shielding plate deployed under the TML and pad, defined as TML shielding and pad shielding respectively. Fig. 1 illustrates the 3D structures for DUT, GSG pads, TML, and the proposed shielding schemes. Fig.1(a) is a standard structure without shielding. On the other hand, Fig.1(b) and (c) illustrate those with TML and pad shielding respectively. Following the test structures, equivalent circuit models adapted to two shielding schemes can be easily developed based on our original lossy substrate model in Fig.1(a). For an ideal shielding, the substrate loss can be eliminated and then the substrate RLC networks (R_{Si}, C_{Si}, L_{Si}, and C_P) under the TML or pad can be removed to leave a simple capacitor, as shown in Fig.1(b) and (c).

The definition of lossy substrate model parameters and extraction method can be referred to our original work [6-7]. A perfect shielding can eliminate substrate loss and remove substrate networks under the pad and TML. Then, the original lossy substrate model is reduced to a simple capacitor, such as C_{pad} and C_{ox} corresponding to pad and TML shielding. Note that C_{pad} and C_{ox} can be calculated from layout and process parameters to serve as the initial values. This simplified equivalent circuit can reduce the parameter extraction flow. The model parameters extracted in this reduced flow assuming an ideal shielding, act as an initial model for further optimization to ensure accuracy over extremely high frequency.

Table 1 summarizes a full set of model parameters extracted through an optimal fitting to the measured S-parameters up to 50 GHz. The results indicate that pad shielding can fully eliminate substrate network under the pad but TML shielding cannot. It suggests that pad shielding enables a more effective isolation against substrate loss compared with TML shielding. Note that pad shielding leads to a dramatic increase of C_{pad} by around 2.5 times and may degrade high frequency performance due to the added parasitic capacitance. Fig. 2 presents open pad S-parameters over a broadband of 50 GHz, and a good agreement between measurement and simulation using the optimized lossy substrate models adapted to various shielding schemes.

Table 1. RLC model parameters of the extended lossy substrate models for four test structures with different shielding schemes

W4N6	Pad RLC model parameters						
Shielding	C_{pad} (fF)	C_{p1} (fF)	C_{Si1} (fF)	L_{Si1} (pH)	R_{Si1} (Ω)	L_{tml} (pH)	C_c (fF)
X	60.54	84.17	234.2	10.44	230.9	46.71	1.50
TML (M1)	64.25	58.62	119.6	211.4	259.4	18.92	0.58
Pad (M1)	161.1	x	x	x	x	20.92	0.70
	C_{ox} (fF)	C_{p2} (fF)	C_{Si2} (fF)	L_{Si2} (pH)	R_{Si2} (Ω)	R_{tml} (Ω)	
X	21.63	1.106	34.94	65	429.7	0.2	
TML (M1)	29.75	21.61	45.2	248.2	207.5	0.19	
Pad (M1)	22.31	59.66	53.53	744.7	136.9	0.199	

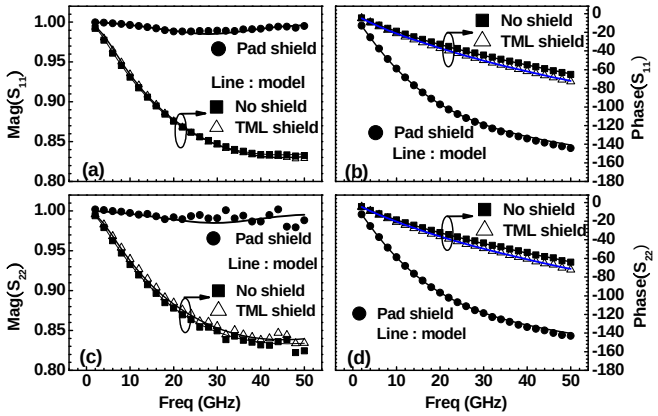

Fig.2 Open pad S parameters for three test structures with different shielding methods (no, TML and pad shielding). A comparison between measurement and simulation by extended lossy substrate models over wide frequency up to 50 GHz (a) mag(S_{11}) (b) phase(S_{11}) (c) mag(S_{22}) (d) phase(S_{22})

III. Noise Shielding Effect on High Frequency Performance

The extended lossy substrate models proven for open pads adopting specified shielding schemes were integrated with intrinsic MOSFET for a two-port network circuit simulation to identify the impact on high frequency and noise characteristics [6-7]. The high frequency accuracy is validated by a satisfactory fitting to the measured S-parameters up to 50 GHz, as shown in Fig.3 for a standard one without shielding and another one with pad shielding. Note that the apparent drop of mag(S_{11},S_{22}) with increasing frequency due to substrate loss, revealed by the standard structure without shielding can be recovered in devices with pad shielding.

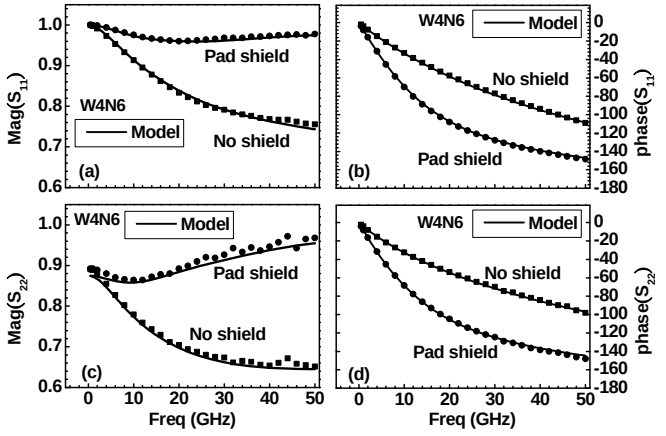

Fig. 3 100 nm nMOS (W/N=4μm/6) S parameters for two test structures (no and pad shielding). A comparison between measurement and simulation by extended lossy substrate models over wide frequency up to 50 GHz (a) mag(S_{11}) (b) phase(S_{11}) (c) mag(S_{22}) (d) phase(S_{22})

Fig. 4 indicates the cut-off frequency f_T corresponding to three test structures and the dramatic degradation suffered by those with pad shielding. The two-port network circuit simulation using the proven lossy substrate models can consistently predict the degradation, shown in Fig. 4(a). The impact considered due to parasitic capacitances introduced from shielding plate (M1) is proven by an analytical expression of f_T, given as $g_m/2\pi(C_{gg}^2-C_{gd}^2)^{1/2}$ and a good match with that extracted from unit current gain, i.e. $|H_{21}|=1$, shown in Fig. 4(b).

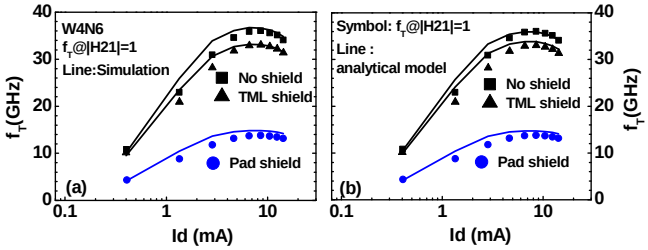

Fig. 4 100 nm nMOS (W/N=4μm/6) measured and simulated f_T for three test structures with different shielding schemes (a) f_T extracted from $|H_{21}|=1$ (b) f_T extracted at $|H_{21}|=1$ and calculated by analytical model $f_T=g_m/2\pi(C_{gg}^2-C_{gd}^2)^{1/2}$

IV. Noise Shielding Effect on RF Noise Parameters

Four noise parameters (NF_{min}, R_n, $Re(Y_{opt})$, $Im(Y_{opt})$) were measured by ATN-NP5B to investigate the influence of shielding structures on RF noise. The bias was fixed at V_{gs}=0.8V for max. g_m and the frequencies were swept from 1GHz to 18 GHz Fig. 5 exhibits four noise parameters measured from 100 nm nMOS in two port test structure with various shielding schemes in Fig.1(a)~(c). The results indicate an effective NF_{min} suppression of around 1.8/2.05 dB at 10/18 GHz realized by pad shielding but very minor effect from TML shielding. It can be understood from shielding effect on S-parameters demonstrated in Fig.2 that substrate loss can be effectively eliminated by pad shielding but not for TML shielding. The reduction of $Re(Y_{opt})$ in Fig.5(c) makes a major contribution to NF_{min} suppression whereas R_n keeps nearly the same. The results infer an important insight that R_n represents intrinsic device property independent of substrate loss and shielding. On the other hand, $Re(Y_{opt})$ closely reflects excess noises introduced from the lossy substrate and can be reduced through an effective shielding against the substrate coupling. $Im(Y_{opt})$ is one more important noise parameter, which performs an optimal matching to the source admittance at the input of DUT.

Regarding NF_{50}, the noise figure normally used in the practice of RF circuit design reveals an interesting result in shielding effect. Fig. 6 demonstrates a significant increase of NF_{50} corresponding to pad shielding that is going a direction opposite to what NF_{min} behaves. The adverse effect on NF_{50} from shielding is considered due to lack of admittance matching for compensating excess capacitances introduced by shielding plate. The proposed mechanism is supported by a consistent correlation with the degradation of f_T shown in Fig. 6(a). The dramatic drop of f_T incurred by shielding can explain the increase of NF_{50} accelerated at higher frequency. The result provides an important guideline in RF circuit design that an appropriately selected inductor is indispensable to realize a compensation for parasitic capacitances, which is particularly critical for low noise design incorporating shielding schemes.

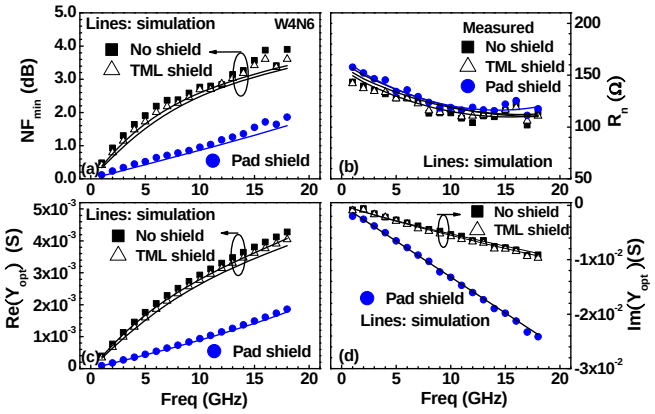

Fig. 5 100 nm nMOS (W/N=4μm/6) noise simulation and measurement for three test structures with different shielding schemes (no, TML, and pad shielding) (a) NF_{min} (b) R_n (c) $Re(Y_{opt})$ (d) $Im(Y_{opt})$

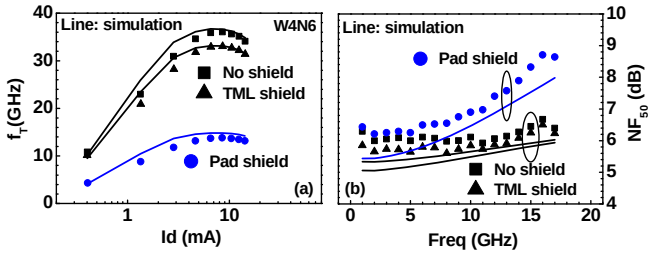

Fig. 6 100 nm nMOS (W/N=4μm/6) f_T before de-embedding and NF_{50} for three test structures with different shielding schemes (a) f_T (b) NF_{50}. Simulation (lines) can consistently predict measurement.

Note that noise simulation based on an improved thermal noise model (a replacement of default noise model in BSIM3) and the proven lossy substrate model can accurately predict the measured noise parameters. The major features incorporated in the improved noise model are short channel effects (velocity saturation, CLM, and carrier heating), substrate resistance induced potential fluctuation effect in drain current noise, and gate resistance induced excess noises in both drain and gate current noises.

V. Conclusion

RF noise shielding methods have been implemented and demonstrated an effective suppression of NF_{min} in 100 nm MOSFETs. A lossy substrate model incorporating inductive impedances in the substrate network can accurately predict substrate loss effect over extremely high frequency up to 50 GHz and the impact on noise parameters. The extended lossy substrate model adapted to noise shielding schemes proves the noise reduction due to elimination of substrate loss through the removal of substrate RLC network from the original one without shielding. The adverse effect on NF_{50} from shielding reveals an impact from the introduced excess capacitances and suggests an appropriate compensation required for RF circuit design. The proposed noise shielding methods and lossy substrate models with proven broadband accuracy for various shielding schemes can facilitate low noise RF CMOS design.

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