

**Program for Promoting Academic Excellence of Universities (Phase V)**

**Final Report**

**前瞻電性微波科技發展計畫一**

**子計畫五：前瞻性微波半導體元件與電路技術**

**(1/4), (2/4), (3/4), (4/4)**

**Advanced Microwave Technologies for  
Telecommunications**

**Sub-project 5: Advanced Microwave Semiconductor  
Devices and Circuit Technologies**

**(1/4), (2/4), (3/4), (4/4)**

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**PD : Edward YiChang**

**Co-PD : Chin-Chun Meng**

**Overall Duration: 04.2004 – 03.2008**

**National Taiwan University (NTU)  
National Chiao Tung University (NCTU)**

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## I. BASIC INFORMATION OF THE PROGRAM

Program Title: Advanced Microwave Technologies for Telecommunications					
<b>Sub-project 5: Advanced Microwave Semiconductor Devices and Circuit Technologies</b>					
<b>前瞻電性微波科技發展計畫—子計畫五：前瞻性微波半導體元件與電路技術</b>					
93 Serial No.: NSC 94-2752-E-009-001-PAE 95 96		Affiliation		National Chiao Tung University 交通大學	
Program Director	Name	Edward Yi Chang 張翼	Program Coordinator	Name	Yueh-Chin Lin 林岳欽
	Tel:	886-3-5712121-52971		Tel:	886-3-5712121-52976
	Fax:	886-3-575-1826		Fax:	886-3-5745497
	E-mail	edc@mail.nctu.edu.tw		E-mail	nctulin@yahoo.com.tw
		Expenditures(in NT\$1,000)		Manpower(Person-Months)	
		Projected	Actual	Projected	Actual
FY2004		10,836	10,825	51	59
FY2005		12,216	10,565	172	174
FY2006		10,879	7,580	360	517
FY2007		12,369	7,206	360	429
Overall		46,300	36,176	943	1,179

**Principal Investigator's Signature:**

## II. LIST OF WORKS, EXPENDITURES, MANPOWER, AND MATCHING SUPPORTS FROM THE PARTICIPATING INSTITUTES (REALITY)

93 Serial No.:NSC94-2752-E-002-001-PAE 95 96		Program Title: Advanced Microwave Technologies for Telecommunications Sub-project 5:Advanced Microwave Semiconductor Devices and Circuit Technologies 前瞻電性微波科技發展計畫—子計畫五：前瞻性微波半導體元件與電路技術										
Subproject -5	Major Tasks and Objectives	Expenditures (in NT\$1,000) (2004.4~2008.3)						Manpower (person-month) (2004.4~2008.3)				
		Salary	Seminar/ Conference- Related Expenses	Project- Related Expenses	Cost for Hardware & Software	Over- head	Total	Principal Investigators	Consultants	Research/ Teaching Personnel	Supporting Staff	Total
2004	Device and circuit Technology	1,613	200	295	8,513	204	10,825	5	0	54	0	59
2005	Device and circuit Technology	2,698	291	382	6,897	297	10,565	5	0	154	15	174
2006	Device and circuit Technology	2,626	183	417	3,714	640	7,580	12	0	481	24	517
2007	Device and circuit Technology	3,752	256	704	1,702	792	7,206	12	0	400	17	429
SUM		10,689	930	1,798	20,826	1933	36,176	34	0	1,089	56	1,179

核定

Subproject t-5	Major Tasks and Objectives	Expenditures (in NT\$1,000) (2004.4~2008.3)						Manpower (person-month) (2004.4~2008.3)				
		Salary	Seminar/ Conference- Related Expenses	Project- Related Expenses	Cost for Hardware & Software	Over- head	Total	Principal Investigators	Consultants	Research/ Teaching Personnel	Supporting Staff	Total
2004	Device and circuit Technology	1,634	200	288	8,510	204	10,836	8	0	36	7	51
2005	Device and circuit Technology	2,495	300	427	8,697	297	12,216	12	0	145	15	172
2006	Device and circuit Technology	5,015	300	488	4,436	640	10,879	12	0	300	48	360
2007	Device and circuit Technology	5,260.1	460	402	5,455	791.9	12,369	12	0	300	48	360
SUM		14,404.1	1,260	1,605	27,098	1,932.9	46,300	44	0	781	118	943

### III. STATISTICS ON RESEARCH OUTCOMES OF THIS PROGRAM (2004/4~2008/3)

LISTING		TOTAL	DOMESTIC	INTERNATIONAL	SIGNIFICANT <sup>1</sup>	Citations <sup>2</sup>
PUBLISHED ARTICLES	JOURNALS	94	-	69	25	2.68
	CONFERENCES	80	-	69	11	
	TECHNOLOGY REPORTS	-	-	-	-	
PATENTS	GRANTED	12	11	1	-	
	PENDING	-	-	-	-	
COPYRIGHTED INVENTIONS	ITEM	-	-	-	-	
WORKSHOPS/ CONFERENCES <sup>3</sup>	ITEM	11	11	-	-	
	PARTICIPANTS	1030	1030	-	-	
TRAINING COURSES (WORKSHOPS/ CONFERENCES)	HOURS	-	-	-	-	
	PARTICIPANTS	-	-	-	-	
PERSONAL ACHIEVEMENTS	HONORS/ AWARDS <sup>4</sup>	-	-	-	-	
	KEYNOTES GIVEN BY PIs	-	-	-	-	
	EDITOR FOR JOURNALS	-	-	-	-	
TECHNOLOGY TRANSFERS	ITEM	7	6	1	-	
	LICENSING FEE (NT\$)	10,093,452	4,243,452	USD 180,000	-	
	ROYALTY	-	-	-	-	
INDUSTRY STANDARDS <sup>5</sup>	ITEM	-	-	-	-	
TECHNOLOGY SERVICES <sup>6</sup>	ITEM	8	3	5	-	
	SERVICE FEE (NT\$)	20,592,000	8,242,000	USD 380,000	-	

<sup>1</sup> Indicate the number of items that are significant. The criterion for “significant” is defined by the PIs of the program. For example, it may refer to Top journals (i.e., those with impact factors in the upper 15%) in the area of research, or conferences that are very selective in accepting submitted papers (i.e., at an acceptance rate no greater than 30%). Please specify the criteria in Appendix IV.

<sup>2</sup> Indicate the number of citations. The criterion for “citations” refers to citations by other research teams, i.e., exclude self-citations.

<sup>3</sup> Refers to the workshop and conferences hosted by the program.

<sup>4</sup> Includes Laureate of Nobel Prize, Member of Academia Sinica or equivalent, fellow of major international academic societies, etc.

<sup>5</sup> Refers to industry standards approved by national or international standardization parties that are proposed by PIs of the program.

<sup>6</sup> Refers to research outcomes used to provide technological services, including research and educational programs, to other ministries of the government or professional societies

## IV . EXECUTIVE SUMMARY ON RESEARCH OUTCOMES OF THIS PROGRAM

### 1. GENERAL DESCRIPTION OF THE PROGRAM

The demand for high-performance compound semiconductor devices for both commercial and military electronic applications at millimeter wave is increasing rapidly. Due to the advantages of inherent properties of most III-V materials, III-V based device technology has been one promising substitute for Si based device technology. Therefore, the research focus on the device technology development, and RFIC designs of GaAs HEMTs (High Electron Mobility Transistors) and HBTs (Heterojunction Bipolar Transistors) devices to integrate the 60 GHz front-end circuits and the GHz IF circuits into one chip with the existing HEMT and HBT technologies.

During the past four years, extensive work has been done in the fields of novel device process development, device wafer epitaxy, device modeling technologies, device package, circuit design, and performance characterization, etc. Sub-project 5 has established the world-class advanced MHEMT and HBT technologies with cutoff frequency ( $f_t$ ) up to 500GHz. The research achievements in this sub project have shown great potential for high end communication industry applications. Technical know-how has been transferred to industry through technology licensing. During the four project years, high-speed and very low-power InP HEMT, high linearity MHEMT and InGaP PHEMT and enhancement-mode InGaP HEMT were fabricated. Nano gate technology down to 40nm has been demonstrated. Low-cost Cu metallization process was realized for the first in HEMTs and HBTs metallization process and was transferred to Win semiconductor in Taiwan. GaAs on Si and GaN on Si technologies were demonstrated with record high electron mobility AlGaSb/InAs HEMT on Si substrate. Novel device package technologies for up to 60GHz application are proposed and developed. HEMT and HBT device modeling based on the device developed were performed. Highly intergraded RFIC using the GaInP/GaAs HBT, SiGe HBT and advance technologies are demonstrated. Several RF integrated circuits including a Weaver image rejection down-converter, a wideband Gilbert mixer using on-chip LO Marchand balun, a sub-harmonic Gilbert mixer using the octet-phase LO generator, four 50% duty-cycle divide-by-3 prescalers, two interstage-matched gain-enhanced LNAs, low-phase-noise quadrature VCOs, two up-converters using the passive and active LC current combiners, a rat-race mixer, a dual-band reactive IQ downconverter, a dual-band reactive SSB upconverter, and an IQ downconverter using a quadrature coupler are also demonstrated.

## **2. BREAKTHROUGHS AND MAJOR ACHIEVEMENTS**

### **(1) Use of $WN_x$ as the Diffusion Barrier for Interconnect Copper Metallization of InGaP/GaAs HBTs**

Use of  $WN_x$  as the Diffusion Barrier for Interconnect Copper Metallization of the InGaP/GaAs HBTs was studied. The X-ray diffraction (XRD) data clearly indicate that the Cu/ $WN_x$ /SiN structure remained quite stable up to 550 °C. The device was annealed at 250°C for 25 hours for the thermal stability test, there was no change in the offset voltage, knee voltage, and saturation current after annealing. The results show that the Cu/ $WN_x$  interconnect layers are quite stable and can be used for the copper metallization for HBT devices.

### **(2) RF and Logic Performance Improvement of $In_{0.7}Ga_{0.3}As$ /InAs/ $In_{0.7}Ga_{0.3}As$ Composite Channel HEMT Using Gate Sinking Technolog**

80-nm-gate  $In_{0.7}Ga_{0.3}As$ /InAs/ $In_{0.7}Ga_{0.3}As$  composite channel high-electron mobility transistors (HEMTs) fabricated using platinum (Pt) buried gate as the Schottky contact metal were evaluated for RF and logic application. After gate sinking at the 250 °C for 3 minutes, the device exhibited a high  $g_m$  value of 1590mS/mm at  $V_d = 0.5V$  and the current gain cutoff frequency  $f_T$  was increased from 390 GHz to 494 GHz after gate sinking and the gate delay time was decreased from 0.83 to 0.78 psec at supply voltage of 0.6 V. These superior performances are attributed to the reduction of distance between gate and channel, and the reduction of parasitic gate capacitances during gate-sinking process.

### **(3) High performance 5 GHz GaInP/GaAs HBT RFICs.**

The 5 GHz Radio is demonstrated using the GaInP/GaAs HBT technology and several high performance RFICs are implemented. These demonstrated RFICs include interstage-matched gain-enhanced LNA, image-reject Gilbert VLIF downconverter with polyphase filter, Gilbert direct conversion sub-harmonic down-conversion mixers, Gilbert up-conversion mixers with output LC current mirror, low-phase-noise parallel-coupled quadrature VCOs and world class superharmonic-coupled QVCO. These RFICs show the potential of a fully integrated GaInP/GaAs HBT RF front-end total solution. An invited talk was given at APMC 2005 for these results.

A GaInP/GaAs HBT (Heterojunction Bipolar Transistor) down-converter using the Weaver architecture is demonstrated. The Weaver down-converter has the image rejection ratios of 48 dB and 44 dB when the RF (Radio Frequency) frequency is 5.2 GHz and 5.7 GHz, respectively. A new frequency quadrupler is employed in the down-converter to generate the LO (Local Oscillator) signals. The frequency quadrupler

is designed to minimize the phase error when generating LO signals and thus the image rejection performance is improved. A diagrammatic explanation using the complex mixing technique to analyze the image rejection mechanism of the Weaver architecture is also developed. The GaInP/GaAs HBT Weaver down-converter is highly integrated. This down-converter includes 166 HBTs.

#### **(4) Passive Components (Hybrids, Baluns, and Couplers) Integrated into ICs Using Standard Silicon Process**

Passive components like hybrids, baluns and couplers are implemented directly on a low-resistivity ( $\sim 10\Omega\text{cm}$ ) silicon substrate and merged into ICs for radio-frequency, microwave, and millimeter-wave applications. The demonstrations include wideband Marchand balun micromixer, UWB micromixer, IQ downconverter using a quadrature coupler, dual-band IQ downconverter with a reactive quadrature generator, and dual-band SSB upconverter with a reactive quadrature generator, rat-race mixer and Marchand balun resistive sub-harmonic mixer.

Thanks to the balanced structure, the passive components still function even at the presence of lossy silicon substrate. The dissipated loss is about 4~6 dB and it is acceptable. The implementation directly on the silicon substrate brings high dielectric constant and then reduces the passive size. Besides, the size reduction is achieved by using spiral coupled lines and lumped-element technique.



### 3. CATEGORIZED SUMMARY OF RESEARCH OUTCOMES

The developed high-frequency device and circuit technologies and related research outcomes in the four project years are as follows.

- (1) A MHEMT with  $\text{In}_{0.55}\text{Ga}_{0.45}\text{As}/\text{In}_{0.67}\text{Ga}_{0.33}\text{As}/\text{In}_{0.55}\text{Ga}_{0.45}\text{As}$  composite channel layers was developed for high linearity application. The use of a composite channel result in high electron mobility and good confinement of electrons in the channel region. A flatter extrinsic transconductance versus applied gate voltage curve was obtained. Low noise device with high linearity was thus obtained by the use of the composite channel designed.
- (2) A 0.1- $\mu\text{m}$  T-gate fabricated using e-beam lithography and thermally reflow process was developed for MHEMTs. Comparing with the two-step lithography of hybrid T-shaped gate and the Y-shaped gate, the reflowed gate process is a much simpler, relatively inexpensive and flexible process. The device also demonstrated an ft higher than 150 GHz.
- (3) An InGaP/AlGaAs/InGaAs PHEMT was developed to improve the device performance of the InGAP/InGaAs PHEMT device. The higher energy bandgap of InGaP layer was used to reduce the gate leakage current. The AlGaAs layer was used as the spacer layer to enhance the electron mobility between InGaP and InGaAs. Therefore, it result in a HEMT device with higher gate breakdown voltage, lower noise figure and higher linearity.
- (4) An InGaP/AlGaAs/InGaAs enhancement-mode PHEMT was developed. The device had a threshold voltage( $V_{\text{th}}$ ) of 0.1V and a low knee voltage of 0.3V. The  $I_{\text{DS}}$  was 375 mA/mm at  $V_{\text{GS}}=0.8\text{V}$ , and the maximum transconductance was 550mS/mm measured at  $V_{\text{DS}} = 2.5\text{V}$ . The calculated  $f_{\text{T}}$  and  $f_{\text{max}}$  of the E-mode PHEMT measured at the  $V_{\text{DS}} = 2.5\text{V}$  and  $V_{\text{GS}} = 0.5\text{V}$  were 60 GHz and 128 GHz, respectively. When the device was biased at  $V_{\text{DS}} = 2\text{V}$ ,  $V_{\text{GS}} = 0.4\text{V}$ , output power of 16.2dBm with 52% PAE was obtained and the device had a high linear gain of 25.3dB at 6Hz.

- (5) Use of  $W_NX$  as the Diffusion Barrier for Interconnect Copper Metallization of the InGaP/GaAs HBTs was studied. The X-ray diffraction (XRD) data clearly indicate that the Cu/ $W_NX$ /SiN structure remained quite stable up to 550 °C. The device was annealed at 250°C for 25 hours for the thermal stability test, there was no change in the offset voltage, knee voltage, and saturation current after annealing. The results show that the Cu/ $W_NX$  interconnect layers are quite stable and can be used for the copper metallization for HBT devices.
- (6) A Gold Free Fully Cu Metallized InGaP/GaAs HBT was studied. It used Pd/Ge and Pt/Ti/Pt/Cu for n-type and p+-type ohmic contacts, respectively, and Ti/Pt/Cu for interconnect metals with platinum as the diffusion barrier. It is evident from the X-ray analytic data that the Ti/Pt/Cu material system is quite stable during annealing up to 350 °C. The copper metallized device was annealed at 250°C for 24 h, and there was no change in the offset voltage, knee voltage, or saturation current after annealing process. The results shows that fully Cu-metallized HBT can be realized using Pt as the diffusion barrier and Pd/Ge and Pt/Ti/Pt/Cu as the ohmic contacts.
- (7) Interface-blocking mechanism for reduction of threading dislocations in SiGe and Ge epitaxial layers on Si(100) substrate was investigated. The XTEM data showed that the high-density dislocations that generatd within the  $Si_{0.08}Ge_{0.92}$  layer were blocked drastically by the Ge/  $Si_{0.08}Ge_{0.92}$ .interface. The results imply that the mechanism of interface blocking can be easily used to control the dislocations for growth of the relaxed SiGe and Ge layers on the Si substrates.
- (8) A novel GeSi buffer structure for growth of high-quality GaAs epitaxial layers on Si substrate was investigated. Three layers of the  $Si_{0.1}Ge_{0.9}$  layer, the  $Si_{0.05}Ge_{0.95}$  layer, and the Ge layer were grown to approach high-quality GaAs epitaxial layer on the Si substrate using a Ge buffer layer. because of the proper lattice-mismatch strains at the upper interfaces of  $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$  and Ge/ $Si_{0.05}Ge_{0.95}$ , the upward propagated dislocations can be bent sideward and terminated effectively. Almost no threading dislocation can propagate into the top Ge layer. As a result, using this Ge/ $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$  layers as a buffer, a high-quality GaAs layer was successfully

grown on the Si(100) substrate with a 6° off-cut toward the [110] direction.

- (9) The uniformly-doped and the  $\delta$ -doped  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$  metamorphic HEMT were fabricated and compared for device linearity. Due to the more uniform electron distribution in the quantum well region, the uniformly-doped MHEMT exhibits more flat  $G_m$  (transconductance) vs  $I_{DS}$  (drain to source current) curve and also showed a much better linearity with higher  $\text{IP}_3$  of 19.83dBm and higher  $\text{IP}_3$  to PDC ratio of 6.21. The results indicate the uniformly-doped MHEMT is more suitable for communication systems that require high linearity operation.
- (10) Copper metallized AlGaAs/InGaAs PHEMT Single-Pole-Double- Throw (SPDT) switches utilizing platinum (Pt, 70 nm) as the diffusion barrier was investigated. These switches were annealed at 250°C for 20 hrs for thermal stability test and showed no degradation of the DC characteristics after the annealing. Also, after 144hrs of HTSL (High Temperature Storage Life test) environment test, these switches still remained excellent and reliable RF characteristics. It is demonstrated that the copper metallization using Pt as the diffusion barrier could be applied to the GaAs monolithic microwave integrated circuits (MMICs) switch fabrication with good RF performance and reliability.
- (11) Fully Copper-Metallized InP HBTs was investigated. Ti/Pt/Cu and Pt/Ti/Pt/Cu metals are used for the n-type and p-type ohmic contacts, respectively, and Ti/Pt/Cu is used as the interconnect metals with platinum as the diffusion barrier to fabricate the Au-free, fully Cu-metallized InP HBTs. The AES depth profiles showed that for the InGaAs/Ti/Pt/Cu sample, there was no atomic inter-diffusion between Cu and the InGaAs layer after annealing at the temperature of 350°C for 30 min. Also, for the fully Cu-metallized InP HBT, there was no change in the offset voltage, knee voltage, or saturation current before and after annealing at 200°C for 3 h, and no significant change in the current gain of the device after 24 h current-accelerated stress test. It suggests that there was no ohmic degradation, copper oxidation, or copper diffusion in the fully Cu-metallized InP HBTs using non-alloyed ohmic contacts with Pt as the diffusion barrier.

- (12) A flip-chip bonding technique was developed for high frequency devices. Alumina ( $\text{Al}_2\text{O}_3$ ) was chosen as the substrate. Gold (Au) was used as the metallization metal for the vertical transition bumps and Ti was used as the adhesion layer. The I-V characteristics of the flip-chip packaged GaAs MHEMT shows minor variation in the DC and RF characteristics as compared to that of the GaAs MHEMT bare die. The maximum available gain (MAG) was almost unchanged up to 70 GHz. The return loss and isolation of the packaged MHEMT device show no degradation as compared to those of the MHEMT bare die and a noise figure (NF) of 1.5 dB with an associated gain of 12 dB at 18 GHz was observed for the packaged MHEMT devices.
- (13) A nano-meter  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$  MHEMT for power applications was developed. The double  $\delta$ -doped structure was used to increase the total sheet charge density and the In content in the channel was increased to 0.6 in order to enhance the barrier height, improve the carrier confinement and increase the speed of carrier transport. The measured drain-source saturation current was 890mA/mm and the maximum transconductance was 827mS/mm. The MHEMT demonstrated P1dB of 11.1 dBm and Gain of 9.5 dB at 32 GHz. The developed nano-meter MHEMT device technology is suitable for power applications at Ka band frequencies and above.
- (14) A high-linearity and high-efficiency enhancement-mode (E-mode) InGaP/AlGaAs/InGaAs pseudomorphic HEMT (PHEMT) for single supply operation was developed. The linearity was improved by optimizing the concentrations of the two  $\delta$ -doped layers. When biased at  $V_{\text{DS}} = 2$  V, the fabricated  $0.5\mu\text{m}\times 200\mu\text{m}$  device exhibits a minimum noise figure (NF<sub>min</sub>) of 0.86 dB with 12.21 dB associated gain at 10 GHz. The device shows excellent linearity with OIP3-P1dB of 13.2 dB and a high linear power efficiency of 35% when under wide-band code-division multiple-access (W-CDMA) modulation. The developed E-mode InGaP/AlGaAs/InGaAs PHEMTs with low noise and high OIP3 and demonstrated highest CDMA linear power efficiency reported.
- (15) A GaAs pseudomorphic HEMT (PHEMT) with Cu-metallized interconnects was successfully developed. Sputtered WNx was used as the diffusion barrier and Ti was

used as the adhesion layer to improve the adhesion between WN<sub>x</sub>/Cu interface in the thin-metal structure. The Ti adhesion layer plays a significant role on the gm and V<sub>p</sub> uniformity of the Cu-metallized PHEMTs. The fabricated Cu-metallized GaAs PHEMT with Ti/WN<sub>x</sub>/Ti/Cu multilayer has a noise figure of 0.76 dB and an associated gain of 8.8 dB at 16 GHz. The cutoff frequency (f<sub>t</sub>) is 70 GHz when biased at V<sub>DS</sub> = 1.5 V. It is demonstrated that the novel Ti/WN<sub>x</sub>/Ti multilayer structure can serve as a good diffusion barrier for Cu metallized airbridge interconnects on GaAs low-noise PHEMTs.

**(16)** Formation of Ti/Pt/Cu gate contact durable under high-temperature operation was successfully realized on InAlAs Schottky layer. Electrical characteristics and thermal stability of the Ti/Pt/Cu Schottky contact on InAlAs were both investigated. The Ti/Pt/Cu Schottky contact had comparable electrical properties compared to the conventional Ti/Pt/Au contact. Ti/Pt/Cu Schottky contact using Pt as the diffusion barrier is also very stable up to 350 °C thermal annealing. The technology can be used for the fabrication of InAlAs/InGaAs high-electron mobility transistors and monolithic microwave integrated circuits.

**(17)** Novel Cu/Mo/Ge/Pd ohmic contacts on n-GaAs were developed for heterojunction bipolar transistors (HBTs) fabrication. The measured specific contact resistance of the Cu/Mo/Ge/Pd ohmic contact was  $2.8 \times 10^{-7} \text{ cm}^2$  after thermal annealing at 350<sup>0</sup>C. Judging from the data of sheet resistance, X-ray diffraction analysis, Auger electron spectroscopy, and transmission electron microscopy, the Cu/Mo/Ge/Pd structure was very stable up to 350<sup>0</sup>C annealing. An InGaP/GaAs HBT with Cu/Mo/Ge/Pd contact metals was fabricated and compared with conventional HBT using Au/Ni/Ge/Au ohmic contacts. Under high current-accelerated stress test at a current density of 120 kA/cm<sup>2</sup> for 24 h, the device with Cu/Mo/Ge/Pd ohmic contacts exhibits excellent electrical characteristics. The Cu/Mo/Ge/Pd structure is thus an effective copper-based ohmic contact structure and can be used for copper metallization of GaAs based HBTs.

**(18)** MOVPE (metal organic vapour-phase epitaxy) growth of very thin and high-quality InGaP etch-stop layer without the formation of intermixing In<sub>x</sub>Ga<sub>1-x</sub>As<sub>y</sub>P<sub>1-y</sub> layer was achieved in an InGaP/GaAs structure. InGaP etch-stop layer has high etching selectivity

to GaAs and can increase the uniformity and manufacturability of the InGaP/GaAs HBT devices. By using the optimized growth temperature and gas switching sequence time, an effective 20Å InGaP etch-stop layer was grown on GaAs successfully and can sustain the wet etching by the solution of  $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:20$  for 45 s.

(19) An  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$  with 0.15- $\mu\text{m}$   $\Gamma$ -Shaped Gate using deep ultraviolet lithography and tilt dry-etching technology is demonstrated. The gate length is controllable by adjusting the tilt angle during the dry-etching process. The developed submicrometer gate technology is simple and of low cost as compared to the conventional E-beam lithography or other hybrid techniques.

(20) An 80-nm InP HEMT with InAs channel and InGaAs subchannels was developed for high frequency ( $>100$  GHz) applications. Because device performance degradation was observed on the  $f_T$  and the corresponding gate delay time which was caused by impact ionization due to the low energy bandgap in the InAs channel. With the design of InGaAs/InAs/InGaAs composite channel, the impact ionization was not observed until the drain bias reached 0.7V, and at this bias, the device demonstrated a very low gate delay time of 0.63 ps with  $f_T$  higher than 300 GHz. It was demonstrated that with the use of composite channel, the device breakdown can be improved and the device shows improved performance in  $f_T$  and delay time and is suitable for high frequency and high-speed and very low-power logic applications.

(21) 80-nm-gate  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{InAs}/\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  composite channel high-electron mobility transistors (HEMTs) fabricated using platinum (Pt) buried gate as the Schottky contact metal were evaluated for RF and logic application. After gate sinking at the 250 °C for 3 minutes, the device exhibited a high  $g_m$  value of 1590mS/mm at  $V_d = 0.5\text{V}$  and the current gain cutoff frequency  $f_T$  was increased from 390 GHz to 494 GHz after gate sinking and the gate delay time was decreased from 0.83 to 0.78 psec at supply voltage of 0.6 V. These superior performances are attributed to the reduction of distance between gate and channel, and the reduction of parasitic gate capacitances during gate-sinking process.

- (22) An enhancement-mode InGaP/AlGaAs/InGaAs PHEMT using platinum (Pt) as the Schottky contact metal was investigated. Following the Pt/Ti/Pt/Au gate metal deposition, the devices were thermally annealed at 325°C for gate sinking. After the annealing, the device shows a positive threshold voltage ( $V_{th}$ ) shift from 0.17 to 0.41 V and a reduced drain leakage current from 1.56 to 0.16  $\mu\text{A}/\text{mm}$ . These improvements in device performance are attributed to the Schottky barrier height increase and the decrease of the gate-to-channel distance as Pt sinks into the InGaP Schottky layer during gate-sinking process.
- (23)  $\delta$ -doped InGaP/InGaAs PHEMT with doping profile modifications are investigated in order to improve the device linearity. Doping modifications in the Schottky layer and in the channel layer of the conventional  $\delta$ -doped InGaP/InGaAs PHEMT were fabricated. It was found that extra doping either in the channel region or in the Schottky layer improved the flatness of the  $G_m$  distribution under different gate-bias conditions. The power performances testing show that even though it had the lowest electron mobility among the three different types of devices studied, the channel-doped device demonstrated the best overall linearity performance, the highest IP3 value, the lowest IM3 level and the best ACPR under CDMA modulation.
- (24) An alloyed Pd/Ge/Cu Ohmic contact to n-type GaAs was studied. The Pd/Ge/Cu Ohmic contact exhibited a very low specific contact resistance of  $5.73 \times 10^{-7} \Omega \text{ cm}^2$  at a low annealing temperature of 250 °C. This result is comparable to the reported Pd/Ge and Au/Ge/Ni Ohmic contact systems to n-type GaAs with doping concentrations about  $1 \times 10^{18} \text{ cm}^{-3}$ . The Ohmic contact behavior was related to the formation of  $\text{Cu}_3\text{Ge}$  and  $\text{PdGa}_x\text{As}_y$  compounds after annealing.
- (25) The diffusion behavior and microstructure evolution of Cu/Ta/GaAs multilayers after thermal annealing were studied and the mechanism is proposed. A thin 30 nm tantalum layer was sputtered as a diffusion barrier to block Ga and As diffusion into the Cu layer. From the results of sheet resistance measurement, X-ray diffraction analysis, Auger electron spectroscopy and transmission electron microscopy, the Cu/Ta films on GaAs were found to be very stable up to 500 °C without Cu migration into GaAs. After

annealing at 550 °C, the interfacial mixing of Ta with GaAs substrate occurred, resulting in the formation of TaAs<sub>2</sub>, and the diffusion of Ga through the Ta layer formed the Cu<sub>3</sub>Ga phase at the Cu/Ta interface. After annealing at 600 °C, the reaction of GaAs with Ta and Cu formed TaAs and Cu<sub>3</sub>Ga owing to Ga migration and interfacial instability.

**(26)** Si<sup>+</sup> pre-ion-implantation combined with a Ge<sub>x</sub>Si<sub>1-x</sub> metamorphic buffer structure for the growth of Ge layer on Si substrate is proposed. Enhanced strain relaxation of the Ge<sub>x</sub>Si<sub>1-x</sub> metamorphic buffer layer on Si substrate was achieved due to the introduction of the point defects by heavy dose Si<sup>+</sup> pre-ion-implantation. Because of the strain relaxation enhancement and the interface blocking of the dislocations in the Ge<sub>x</sub>Si<sub>1-x</sub> metamorphic buffer structure, the total thickness of the buffer layers was only 0.45 μm. No cross-hatch pattern was observed on the Ge surface and the dislocation density for the top Ge film was only  $7.6 \times 10^6 \text{ cm}^{-2}$ .

**(27)** The growth of the AlGaSb/InAs HEMT epitaxial structure on the Si substrate is investigated. Buffer layers consisted of UHV/CVD-grown Ge/GeSi and MBE-grown AlGaSb/AlSb/GaAs were used to accommodate the strain induced by the large lattice mismatch between the AlGaSb/InAs HEMT structure and the Si substrate. Very high room-temperature electron mobility of 27,300 cm<sup>2</sup>/Vsec was achieved. It is demonstrated that a very-high-mobility AlGaSb/InAs HEMT structure on the Si substrate can be achieved with the properly designed buffer layers.

**(28)** High quality GaN film growth on Si (111) substrate was studied by MOVPE. Using multilayer AlN films grown at different temperatures combined with graded Al<sub>1-x</sub>Ga<sub>x</sub>N film as the buffer, the tensile stress on the buffer layer was reduced and the compressive stress on the GaN film was increased. Finally, high quality 0.5 μm crack-free GaN epitaxial layer was successfully grown on 6 inch Si substrate.

**(29)** Novel coaxial transition for CPW-to-CPW flip chip interconnect is presented and experimentally demonstrated. To realize the coaxial transition on the CPW circuit, benzocyclobutene was used as the interlayer between the vertical coaxial transition and



the CPW circuit. The demonstrated interconnect structure shows excellent interconnect performance up to 55GHz with low return loss below 20 dB and insertion loss less than 0.5 dB even when the underfill was applied to the structure.

**(30)** The microstrip-to-coplanar waveguide hot-via flip interconnect has been experimentally demonstrated. The interconnect structures with the hot-via transitions were designed and optimized by using the electromagnetic simulation tool. The optimized interconnect structure with compensation design demonstrated excellent RF characteristics with the insertion loss less than 0.5 dB and the return loss below 18 dB over a very broad bandwidth from DC to 67GHz.

**(31)** The RF-via interconnect structure from the 0- to the 1-level package for coplanar RF-MEMS devices packaging was evaluated. The 0/1-level interconnect structure was designed and optimized using the electromagnetic simulation tool. The measured and simulated results show good agreement, demonstrating DC to 60 GHz broadband interconnect performance through the two levels package with return loss below 15dB and insertion loss within 0.6 dB.

**(32)** A 5.2-GHz 11-dB gain,  $IP_{1dB} = 17$  dBm and  $IIP_3 = 10$  dBm double-quadrature Gilbert downconversion mixer with polyphase filters is demonstrated by using GaInP/GaAs heterojunction bipolar transistor (HBT) technology. The image rejection ratio is better than 40 dB when LO = 5.17 GHz and intermediate frequency (IF) is in the range of 15 MHz to 40 MHz. The Gilbert downconverter has four-stage RC-CR IF polyphase filters for image rejection. Polyphase filters are also used to generate local (LO) and radio frequency (RF) quadrature signals around 5 GHz in the double-quadrature downconverter because GaAs has accurate thin film resistors and the low parasitic semi-insulating substrate.

**(33)** A compact 5.2-GHz Gilbert upconversion mixer is demonstrated using the GaInP/GaAs HBT technology. A miniature lumped-element rat-race hybrid and an LC current combiner are used in the LO port and the RF port of the upconversion Gilbert mixer, respectively. An active IF balun is incorporated in the Gilbert upconverter with no extra

power consumption.

- (34)** A 5.2 GHz three-level sub-harmonic downconversion Gilbert mixer using GaInP/GaAs HBT (Heterojunction Bipolar Transistor) technology is demonstrated.
- (35)** Two 5.2 GHz two-level sub-harmonic downconversion Gilbert mixer using GaInP/GaAs HBT (Heterojunction Bipolar Transistor) technology are demonstrated. One is the top-lo configuration and the other is the bottom-lo configuration.
- (36)** The GaInP/GaAs HBT Quadrature VCO Using Stacked Transformers is realized at 5.4 GHz. The parallel coupling scheme is used between two cross-coupled differential VCOs. This QVCO has the phase noise of -127.4 dBc/Hz at 1 MHz offset frequency at the oscillation frequency of 5.38 GHz. The FOM is -191 dBc/Hz. The low phase noise comes from the excellent low-frequency noise properties of the GaInP/GaAs HBT device and the high coupling stacked transformers.
- (37)** Transformer-Based Superharmonic-Coupled GaInP/GaAs HBT QVCO is achieved around 5 GHz. The superharmonic coupling scheme does not change the oscillation frequency from the LC tank resonant frequency and thus accurate quadrature signals can be obtained without phase noise degradation. The superharmonic-coupled GaInP/GaAs HBT QVCO has the phase noise of -131 dBc/Hz at 1 MHz offset frequency when the oscillation frequency is 4.87 GHz. The FOM of our GaInP/GaAs HBT superharmonic-coupled QVCO shows a record of -198 dBc/Hz and is much better than the FOMs of CMOS superharmonic-coupled QVCO. The FOM of our oscillator is also the best FOM ever reported among all the monolithic VCOs to the best of our knowledge.
- (38)** A GaInP/GaAs HBT (Heterojunction Bipolar Transistor) down-converter using the Weaver architecture is demonstrated. The integration level of this GaInP/GaAs IC in this work is quite high and the IC contains 166 GaInP/GaAs HBTs. Instead of frequency dividing, a frequency multiplying circuit is incorporated to generate the LO signals in this work. The quadrupler used in this work is able to minimize the time delay when it

multiplies, the  $LO_1$  signal will contain much less phase errors. The Weaver down-converter has the image rejection ratios of 48 dB and 44 dB when the RF (Radio Frequency) frequency is 5.2 GHz and 5.7 GHz, respectively.

**(39)** A single-ended wideband downconversion Gilbert micromixer is demonstrated in this work using 0.35- $\mu\text{m}$  SiGe BiCMOS technology. A transimpedance amplifier with resistive feedback is utilized in the IF stage while a broadband Marchand balun is employed to generate wideband differential LO signals. The planar Marchand balun topology employed in this work can generate truly balanced signals even in the presence of the lossy low-resistivity ( $\sim 10 \Omega\text{cm}$ ) silicon substrate.

**(40)** A 5.7 GHz GaInP/GaAs heterojunction bipolar transistor (HBT) sub-harmonic Gilbert down-conversion mixer with the octet-phase LO generator is demonstrated. The conversion gain is 15 dB,  $IP_{1\text{dB}}$  is  $-13$  dBm,  $IIP_3$  is 0 dBm, and  $IIP_2$  is 24 dBm when the LO power equals 3 dBm. The measured IF quadrature output waveforms indicate that the phase difference between the in-phase and quadrature-phase output channels is only 1.3 degrees.

**(41)** We realized four 50% duty cycle divide-by-3 prescalers using the 2- $\mu\text{m}$  GaInP/GaAs Heterojunction bipolar transistor (HBT) technology and the 0.35- $\mu\text{m}$  SiGe BiCMOS technology: sample-sample-hold (SSH) and sample-hold-hold (SHH) prescalers. The current switchable emitter couple logic D flip-flops are employed to form both prescalers. The maximum operating frequency of SHH prescaler is enhanced about 50% when compared with that of the SSH prescaler due to better signal synchronization.

**(42)** Two SiGe HBT upconverter are realized using the passive and active LC current combiners. A passive LC (inductor – capacitor) current mirror is applied at the output of the Gilbert mixer core to provide the differential-to-single conversion and to double the output current at the resonant frequency. The passive inductors employed in the LC current mirror always occupy large chip area. There is the other up-converter using the active inductors consisting of the common-collector transistors and feedback resistors to save die area and still preserve upconverter performance.

- (43) A 10-GHz sub-harmonic Gilbert mixer is demonstrated using GaInP/GaAs hetero-junction bipolar transistor technology. The local oscillator (LO) signal time-delay path in the sub-harmonic LO stage is compensated using the fully symmetrical stacked-LO doubler; therefore, the balance of the sub-harmonic LO stage, the radio frequency to intermediate frequency isolation, and  $IIP_2$  are improved. The demonstrated 10-GHz sub-harmonic mixer achieves 10 dB conversion gain,  $IP_{1dB}$  of 12 dBm,  $IIP_3$  of 2 dBm and  $IIP_2$  of 33 dBm.
- (44) A frequency divider with super-dynamic D-type flip-flop is demonstrated in 2  $\mu$ m GaInP/GaAs HBT ( $f_T = 40$  GHz) technology. By biasing the HBT devices around the peak transit-time frequency ( $f_T$ ), the operating frequency of a D-FF with ECNFP (emitter-coupled negative feedback pairs) can be improved. At a supply voltage of 5 V, a divide-by-two function of 9.5 GHz is achieved.
- (45) A regenerative frequency divider with a differential transimpedance amplifier (TIA) active load using 0.35  $\mu$ m SiGe HBT technology is demonstrated. The differential TIA is beneficial for higher frequency and lower sensitivity operation, and the inductive peaking enhances the bandwidth of the output buffer. From the experimental results, the operating frequency ranges from 5 to 27 GHz ( $f_{max}/f_{min}=5.2$ ) for a supply voltage of 5 V and core power consumption of 49.5 mW.
- (46) A 5.7 GHz I/Q downconversion mixer is demonstrated in this letter using 0.35  $\mu$ m SiGe BiCMOS technology. A quarter-wavelength coupled line and two center-tapped transformers are utilized to generate differential quadrature LO signals. A miniaturized Marchand balun is placed before the common-base-configured RF input stage of each I/Q Gilbert mixer to generate balanced RF signals. All the reactive passive elements are placed directly on the standard silicon substrate. The 5.7 GHz I/Q downconverter achieves 7 dB conversion gain, -26 dBm  $IP_{1dB}$ , and -18 dBm  $IIP_3$  at the power consumption of 3.875 mW and 2.5 V supply voltage.
- (47) The V-band coplanar waveguide (CPW)-microstrip line (MS)-CPW two-stage amplifier with the flip-chip bonding technique is demonstrated using 0.15  $\mu$ m

AlGaAs/InGaAs pseudomorphic high electron mobility transistor technology (pHEMT). The CPW is used at input and output ports for flip-chip assemblies and the MS transmission line is employed in the interstage to reduce chip size. This two-stage amplifier employs transistors as the CPW-MS transition and the MS-CPW transition in the first stage and the second stage, respectively. The CPW-MS-CPW two-stage amplifier has a gain of 14.8 dB, input return loss of 10 dB and output return loss of 22 dB at 53.5 GHz. After the flip-chip bonding, the measured performances have almost the same value.

- (48) The fully integrated GaInP/GaAs heterojunction bipolar transistor (HBT) transformer-based top-series quadrature voltage controlled oscillator (QVCO) is demonstrated at 4 GHz. The transformers on the semi-insulating GaAs substrate possess good electrical properties at high frequencies. The quadrature VCO at 4.1 GHz has phase noise of -120 dBc/Hz at 1MHz offset frequency, output power of 2 dBm and the figure of merit (FOM) -178 dBc/Hz.
- (49) A K-band sub-harmonically pumped resistive mixer (SPRM) is demonstrated using standard 0.13 um CMOS technology. A miniature Marchand Balun is integrated with the resistive mixer to generate equal amplitude and out-of-phase signals for mixer's LO port directly on the lossy silicon substrate. The sub-harmonic resistive mixer with the integrated Marchand balun has conversion loss of 11~12 dB at  $f_{IF} = 100$  MHz and  $P_{LO} = 7$  dBm for RF frequencies from 18 to 26 GHz. The LO-RF and LO-IF isolations are approximately 30 dB and 33 dB, respectively.
- (50) An integrated GaInP/GaAs heterojunction bipolar transistor (HBT) regenerative frequency divider (RFD) with active loads is demonstrated from 4 GHz to 26 GHz. In this work, the RFDs with resistive loads and active loads are fabricated in the same chip for comparison. From the measured results, the active loading type obviously has wider operating frequency and lower input sensitivity. The  $f_{max}/f_{min}$  ratio of 6.5 is higher than that of general RFDs. The core power consumption is 36.7 mW at the supply voltage of 5 V. The chip size is 1.0 X 1.0 mm<sup>2</sup>.

- (51) A 5.2 GHz 1 dB conversion gain,  $IP_{1\text{ dB}} = -19\text{ dBm}$  and  $IIP_3 = -9\text{ dBm}$  double quadrature Gilbert downconversion mixer with polyphase filters is demonstrated by using 0.35  $\mu\text{m}$  SiGe HBT technology. The image rejection ratio is better than 47 dB when LO=5.17 GHz and IF is in the range of 15 MHz to 45 MHz. The Gilbert downconverter has fourstage RC-CR IF polyphase filters for the image rejection. Polyphase filters are also used to generate LO and RF quadrature signals around 5 GHz in the double quadrature downconverter.
- (52) An effective way to boost power gain without noise figure degradation in a cascode low noise amplifier (LNA) is demonstrated at 4 GHz using 0.35  $\mu\text{m}$  SiGe HBT technology. This approach maintains the same current consumption because a low-pass  $\pi$ -type LC matching network is inserted in the inter-stage of a conventional cascode LNA. 5 dB gain enhancement with no noise figure degradation at 4 GHz is observed in the SiGe HBT LNA with inter-stage matching.
- (53) A 10-GHz sub-harmonic Gilbert mixer is demonstrated in this paper using the 0.35  $\mu\text{m}$  SiGe BiCMOS technology. The timedelay when the sub-harmonic LO (Local Oscillator) stage generates subharmonic LO signals is compensated by using fully symmetrical multiplier pairs. High RF-to-IF isolation and sub-harmonic LO Gilbert cell with excellent frequency response can be achieved by the elimination of the timedelay. The SiGe BiCMOS sub-harmonic micromixer exhibits 17 dB conversion gain, -74 dB 2LO-to-RF isolation,  $IP_{1\text{ dB}}$  of -20 dBm, and  $IIP_3$  of -10 dBm. The measured double sideband noise figure is 16 dB from 100-kHz to 100-MHz because the SiGe bipolar device has very low 1/f noise corner.
- (54) A 2.4/5.7 GHz dual-band Gilbert upconversion mixer is demonstrated using 0.35  $\mu\text{m}$  SiGe BiCMOS technology. A bias-offset cross-coupled transconductance amplifier (TCA) is employed in the intermediate frequency port for the linearity improvement. The dual-band LC current combiner and the output shunt-shunt feedback buffer amplifier are in the radio frequency (RF) port. The mechanisms of the high linearity upconverter and the design flow of the dual-band LC current combiner are established in this letter. The dual-band upconverter has conversion gain of 1.5/-0.2 dB,  $OP_{1\text{ dB}}$  of

-10.5/-9 dBm, and OIP<sub>3</sub> of 12/13 dBm for IF=100 MHz, RF= 2.4/5.7 GHz, respectively.

(55) A GaInP/GaAs HBT broadband RF front-end consisting of a low noise wideband amplifier and a micromixer is demonstrated in this paper. The major advantage of this work is the elimination of inductors and thus the chip area can be greatly saved. The bandwidth of the RF front-end is up to 7 GHz. The measured conversion gain is higher than 25 dB from 1 GHz to 7 GHz and the noise figure of the RF front-end is less than 8 dB within the bandwidth.

#### 4. PROGRAM MANAGEMENT

Sub-project 5 provides high-frequency MHEMT and HBT device foundry service and device modeling techniques to support sub-project 2 for the development of high-performance microwave and millimeter wave MMICs up to 60GHz. Sub-project 5 also develops advanced device technologies and makes improvements in terms of structure design and fabrication process targeting manufacturing cost down as well as performance enhancement.

#### 5. INTERNATIONAL COOPERATION ACTIVITIES

Due to the remarkable achievements in the former stage of this project, cooperation activities with overseas research institutes or companies are plenty and the number is increasing every year.. The collaboration work provides opportunities for exchange of technical experience or propaganda of project achievements.

The following is a list of international cooperation undergoing:

- (1) **Chalmber University (Sweden):** GaN power amplifier developement and high-frequency circuit testing.
- (2) **NTT Basic Research Lab. (Japan):** Epitaxial growth of advanced material system for high-speed electronics application.
- (3) **Quantum Nanoelectronics Research Center (QNERC), Tokyo Institute of Technology (Japan):** development of nano-lithography process for high-speed device fabrication.
- (4) **Sharp Laboratories of America (U.S.A.):** deposition of thick crack-free GaN film on Si

substrate to reduce the material cost for GaN devices.

- (5) **Telekom Research & Development Sdn Bhd(TMR&D) (Malaysia):** device physics and technology training course on compound semiconductor devices.
- (6) **Intel Corporation (USA):** feasibility Study of InAs-based QWFETs for Ultra High Speed, Low Power Logic Applications.
- (7) **Hitach Research Center (Japan) :** MHEMT MMIC research cooperation.
- (8) **Ulvac Corporation (Japan ) :** GaN MBE abd ICP etch materials and process technology developement.
- (9) **Samsung Cheil Corp. (Korea):** Hard mask materials development for submicron technology application.
- (10) **Penn State University (USA):** InAs device development.



# Appendix II

## VI. APPENDIX II

### (1) Publication List

#### A1. Journal (Significant)

- [1]. Shang-Wen Chang, Edward Yi Chang, Cheng-Shih Lee, Ke-Shian Chen, Chao-Wei Tseng, and Tung-Ling Hsieh, "Use of  $WN_x$  as the Diffusion Barrier for Interconnect Copper Metallization of InGaP/GaAs HBTs", IEEE Transactions on Electron Device, Vol.51, No. 7, 2004.
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2007.

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- [63]. J. Y. Su, C. C. Meng, Y. H. Li, S. C. Tseng and G. W. Huang, "2.4 GHz 0.35  $\mu$ m CMOS Single-Ended LNA and Mixer with Gain Enhancement Techniques," in 2005 Asia Pacific Microwave Conference, pp. 1550-1553, Dec. 2005.
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### **B3. Conference (Domestic)**

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- [2] Tsung-Hsi Yang, Guangli Luo, Edward Yi Chang, Y. C. Hsien, and Chun-Yen Chang, "Interface-blocking mechanism for reduction of threading dislocations in SiGe and Ge epitaxial layers on Si(100) substrate," in the *Asian CVD*, Taiwan, 2004.
- [3] L. H. Chu, E. Y. Chang, S. H. Chen, Y. C. Lien, and C.Y. Chang, "InGaP/AlGaAs/InGaAs enhancement-mode pseudomorphic HEMT for high frequency application," *2004 International Electron Devices and Materials Symposia*, Hsinchu,



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## (2) Patent list

- [1]. 張翼, 張晃崇, 傅國貴, "深次微米級 T 型閘極半體裝置之製造方法", R.O.C. I226666
- [2]. 張翼, 李晃銘, "利用熱回流光阻技術製造奈米級閘極於半導體裝置中之方法", R.O.C. 569077, 2003.5~2023.4
- [3]. 張翼, 張尚文, 李承士, "具銅金屬化之複合物半導體元件", R.O.C. 200636934
- [4]. C. S. Lee, E. Y. Chang, "Schottky structure in GaAs semiconductor device", US 200118
- [5]. 李承士, 張翼, 陳克弦, "一種在砷化鎵半導體上的蕭基(Schottky)結構", R.O.C. 540160
- [6]. 李承士, 張翼, "半導體製程之新型對準標記", R.O.C. 528204
- [7]. 李承士, 張翼, "可調式準直器與具有此種可調式準直器之濺鍍設備", R.O.C.200531181
- [8]. 羅廣禮, 楊宗火喜, 張俊彥, 張翼, "在矽晶片上成長鍍薄膜之方法", R.O.C. 221009, 2004.9.11~2023.7.27
- [9]. 張翼, 羅廣禮, 楊宗火喜, 張俊彥, "在矽鍍磊晶片上成長砷化鎵磊晶之方法", R.O.C. 221001, 2004.9.11~2023.7.27
- [10]. 李承士, 張翼, "砷化鎵元件背面銅金屬化之製作方法", R.O.C.I222675
- [11]. 李承士, 張尚文, 張翼, "III-V 族半導體元件的內連銅導線、銅空氣橋及其製作方法", R.O.C. 200501319
- [12]. 陳仕鴻, 郭建億, 張翼, "形成電子裝置閘極圖案之方法", R.O.C.I265564

### **(3) LIST OF WORKSHOP/CONFERENCE HOSTED BY THE PROGRAM**

#### **2004**

- [1]. “Millimeter Wave GaAs MMICs and High Frequency Packaging”, May 21, 2004, 180 PERSON-TIMES
- [2]. “Novel Nitride Semiconductor Devices”, June 10, 2004, 150 PERSON-TIMES

#### **2005**

- [3]. “NEW GAN MATERIALS DEVELOPMENT FOR OPTOELECTRONIC AND ELECTRONIC DEVICES”, JUN 1, 2005, 150 person-times
- [4]. “Development of MMICs and widebandgap devices at Chalmers University”, May 26, 50 person-times

#### **2006**

- [5]. Seminar on High Speed Semiconductor Devices (Dec 22, 2006), Participants: 30
- [6]. Ultra-Low Power Nanoelectronics for Logic Applications (Dec 18, 2006), Participants: 40
- [7]. Growth of Super Wide-bandgap Semiconductors and Their Applications to Devices (Nov. 15, 2006), Participants: 160

#### **2007**

- [8]. GaN for Electronics Application (Nov. 18, 2006) , Participants: 30
- [9]. Multifunctional millimeterwave MMICs for emerging applications (Dec 15, 2006), Participants: 70
- [10]. Photovoltaic Projects in Japan and Recent Achievements in Tokyo Tech (Dec 20, 2006), Participants: 70
- [11]. Panel Discussion on IEEE 2008 RFIC Symposium “Millimeter-wave IC: Is silicon winning? Is GaAs still alive?” (June, 2008). Panelists: 7
- [12]. “Design of RF-CMOS Integrated Circuits for Wireless communications” and “Next Generation Handset Transmitters” (Dec 18, 2006), Participants: 100

### **(4) LIST OF PERSONAL ACHIEVEMENTS OF THE PIs**

- [1]. Edward Yi Chang: 獲得九十六年度經濟部第一屆大學產業經濟貢獻獎
- [2]. Edward Yi Chang, Organizing Committee, IEEE Conference on Indium Phosphide & Related Materials (IPRM)
- [3]. Edward Yi Chang, Sub Program Committee, IEEE IEDM

- [4]. Edward Yi Chang, Distinguished Lecturer, IEEE EDS
- [5]. Edward Yi Chang, International Advisory Committee, IEEE ICSE
- [6]. Edward Yi Chang, Organizing Committee, IEEE ISCS (Japan)
- [7]. Edward Yi Chang, Invited speaker, IEEE TWHM 2007
- [8]. Edward Yi Chang, Invited speaker, SSDM 2007
- [9]. Edward Yi Chang, Invited speaker, ISCS 2007
- [10]. Edward Yi Chang, Invited speaker, ECS 2008
- [11]. Edward Yi Chang, Invited speaker, MRS 2008
- [12]. Edward Yi Chang, Organizing Committee, SSDM 2008
- [13]. Edward Yi Chang, Organizing Committee, Invited speaker, European Microwave Conference 2008.
- [14]. Edward Yi Chang:國立交通大學：第一屆『產學技術交流卓越貢獻獎』銀翼獎 (2005/12)
- [15]. Edward Yi Chang:國立交通大學：第二屆『產學技術交流卓越貢獻獎』銅翼獎 (2006/12)
- [16]. Edward Yi Chang:國立交通大學：第三屆『產學技術交流卓越貢獻獎』金翼獎 (2007/12)
- [17]. Chinchun Meng, Personal Royalty Income: U.S. pattern number 5,466,965. “High efficiency, high power multiquantum well IMPATT device with optical injection locking” 2,400 U.S.D. royalty received from U.C.L.A. in 2005 (Total Royalty Income from Limo Mobile Data to U.C.L.A.: 22,000 U.S.D. in 2005), 500 U.S.D. royalty received from U.C.L.A. in 2006, 191 U.S.D. royalty received from U.C.L.A. in 2007. Expect to receive the royalty on yearly basis.
- [18] Chinchun Meng, T. H. Wu, M. C. Lin, C. H. Chen, J. C. Jhong, Y. W. Chang, S. C. Tseng, B. C. Tsou, D. W. Sung, S. K. Hsu, M. H. Chiang, S. S. Lu, H. C. Chen, M. C. Chiang, S. A. Yu, and G. W. Huang, Dec 2005, “High Performance GaInP/GaAs HBT Radio Frequency Integrated Circuits at 5 GHz”, 2005 Asia Pacific Microwave Conference, invited paper, pp. 823-826.
- [19] Chinchun Meng, invited speaker, GSMM 2008.

## **(5) LIST OF TECHNOLOGY TRANSFER**

### **2005**

- [1]. “Copper Metallization for GaAs MMICs”, Technology Transferred to Win Semiconductor corporation.
- [2]. “Development of ITO Film and Reflector Technology”, Technology Transferred to Ring Light Technology.

## **2006**

- [3]. "Copper Metallization for GaAs MMICs", Win Semiconductor corporation (2006.01.10~); Amount: NT 800,000 (2006~)
- [4]. "Thick-film photoreist technology for III-V device package applications", Everlight Group (2006.05.01~ 2007.04.30); Amount: NT 500,000
- [5]. "Device Physics and Technology Course On Compound Semiconductor Devices In TM Research & Development", Telekom Research & Development Sdn Bhd(TMR&D) (2007); Amount: NT 1,943,452
- [6]. "Dry etch process for III-V based materials", ULVAC TAIWAN Co., Ltd (2005.5.31~2006.05.30); Amount: NT 1,000,000.

## **2007**

- [7]. Transfer of technology in the development of active and passive devices for the realization of high performance MMICs" Amount: USD 180,000.

## **(6) LIST OF TECHNOLOGY SERVICE**

### **2004**

- [1]. Collaboration with Ministry of Transportation and Communications for "Side Warning System Development & Demonstration for Vehicle Collision Avoidance Radar"  
Budget: NT \$2,892,000      Duration: 93.02.01~93.11.30

The purpose of this research project is "The Side Warning System Development and Demonstration for Vehicle Collision Avoidance". We collect associated information and references of side warning collision avoidance techniques for trunk, and select a realistic approach, which is suitable for domestic trunk driving conditions. During this research phase, we also developed a prototype of side warning system for trunk collision avoidance. Through this project, we expect to get a best performance for side collision avoidance. Furthermore, we try to solve the engineering issues as well as to propose some suggestions for the government.

- [2]. Collaboration with Semiconductor Research Corporation for "Development of Data Bases and Optimization Simulation Packages for RFIC Inductors"  
Budget: NT \$3,350,000      Duration:93.07.01~94.06.30

The objective is to develop a comprehensive, reliable, and efficient design system for RFIC inductors. Anticipated results are as follows:

1. Extraction of material EM parameters in silicon wafer.
2. Development of data bases for RFIC inductors.
3. Development of EM simulation and optimization software for RFIC inductors.
4. Analysis of coupling effects and shielding designs

- [3]. Collaboration with AirWave Technologies Inc. for “60-GHz Millimeter-wave Communication Technology”

Budget: NT \$2,000,000      Duration:91.06.01~93.05.31

The project is to develop a reliable, robust, and efficient 60-GHz communication system platform. Major results are as follows:

1. Development of the active components, such as LNA, PA, oscillator, and mixer, for 60-GHz system.
2. Development of the passive components, such as filter, antenna, switch, and coupler, for 60-GHz system.
3. Development of high frequency flip-chip interconnection technology for 60-GHz system integration.

#### **2005**

- [4]. “Feasibility Study of InAs-based QWFETs for Ultra High Speed, Low Power Logic Applications”, Intel Corporation (Phase I : Q4, 2005 – Q3, 2006) ; Amount: USD 60,000

#### **2006**

- [5]. “Feasibility Study of InAs-based QWFETs for Ultra High Speed, Low Power Logic Applications”, Intel Corporation (Phase II : Q4, 2006 – Q3, 2007) ; Amount: USD 60,000

#### **2007**

- [6]. “Feasibility Study of InAs-based QWFETs for Ultra High Speed, Low Power Logic Applications”, Intel Corporation (Phase II : Q4, 2007 – Q3, 2008) ; Amount: USD 60,000

- [7]. “Development of GaN Epi materials on 6 inch Si substrate”, Sharp electronic (Japan); Amount: USD 60,000

- [8]. “Development of Hard Mask Materials for Submicron technology”, Amount: USD 200,000

**Appendix III**  
**List of Publications in Top Journals and**  
**Conferences**

### **VII. APPENDIX III : LIST OF PUBLICATIONS IN TOP JOURNALS AND CONFERENCES**

- [1]. Shang-Wen Chang, Edward Yi Chang, Cheng-Shih Lee, Ke-Shian Chen, Chao-Wei Tseng, and Tung-Ling Hsieh, 2004, "Use of  $WN_x$  as the Diffusion Barrier for Interconnect Copper Metallization of InGaP/GaAs HBTs", IEEE Transactions on Electron Device, Vol.51, No. 7.
- [2]. Chien-I Kuo, Heng-Tung Hsu, Edward Yi Chang, Chia-Yuan Chang, Yasuyuki Miyamoto, Suman Datta, Marko Radosavljevic, Guo-Wei Huang, and Ching-Ting Lee, "RF and Logic Performance Improvement of  $In_{0.7}Ga_{0.3}As$  /InAs/ $In_{0.7}Ga_{0.3}As$  Composite Channel HEMT Using Gate Sinking Technology" IEEE Electron Device Lett. 2008.
- [3]. S. C. Tseng, C. C. Meng, C. H. Chang, C. K. Wu and G. W. Huang, "Monolithic broadband Gilbert micromixer with an integrated Marchand balun using standard silicon IC process", IEEE transaction on Microwave Theory and Techniques, Dec 2006.
- [4]. T. H. Wu and C. C. Meng, "5.2/5.7GHz 48dB Image Rejection GaInP/GaAs HBT Weaver Down-Converter Using LO Frequency Quadruple", IEEE Journal of solid-state circuits, vol. 41, no. 11, pp.2468-2480, Nov 2006.

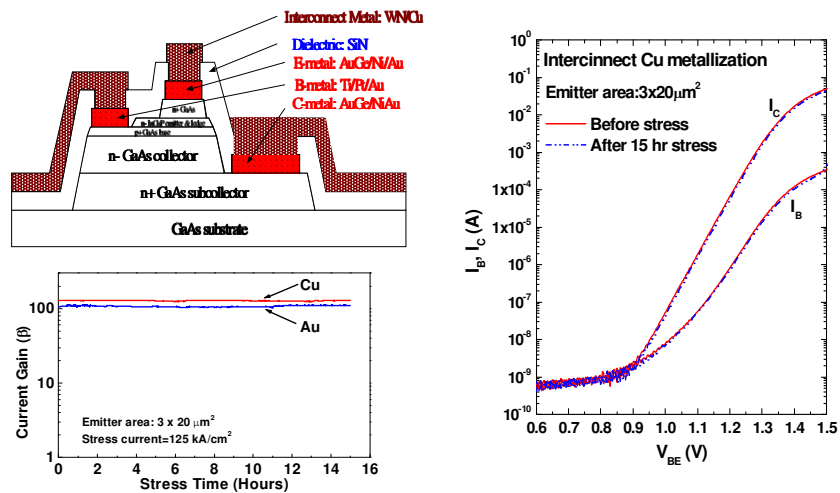
**Appendix IV**  
**Slides on Science and Technology**  
**Breakthroughs**



## VIII. APPENDIX IV : SLIDES ON SCIENCE AND TECHNOLOGY BREAKTHROUGHS

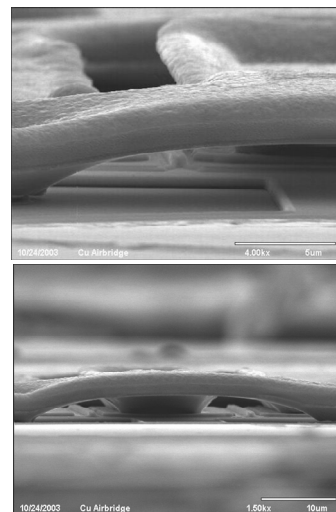
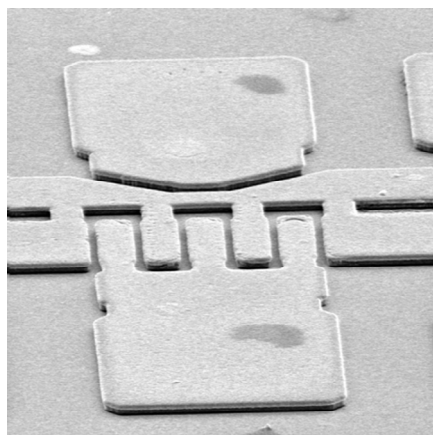
(1) Copper metallization on GaAs device is demonstrated for the first time. Use of  $WN_x$  as the Diffusion Barrier for Interconnect Copper Metallization of the HBTs were fabricated. The XRD data clearly indicate that the  $Cu/WN_x/SiN$  structure remained quite stable up to  $550\text{ }^\circ\text{C}$ . The device was annealed at  $250^\circ\text{C}$  for 25 hours for the thermal stability test, the device exhibited excellent stability with no change in with  $WN_x$  diffusion barrier.

### Structure of InGaP/GaAs HBT with Interconnect Copper Metallization and Current Accelerated Test Data



- Reliability test for the Cu and Au metallized HBT at high current density  $J_c=125\text{ kA/cm}^2$  and  $V_{CE}=3\text{V}$ . The devices show no degradation after 15 hours.

### SEM Image of Cu Airbridge



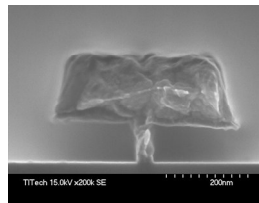
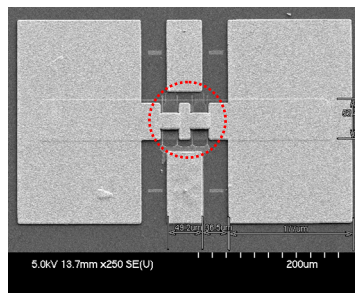
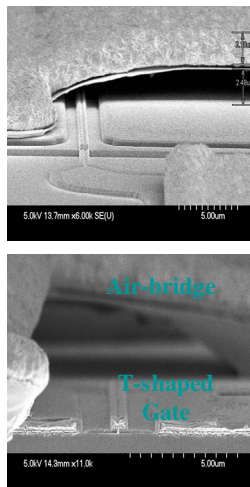
(2) 80-nm-gate  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{InAs}/\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  composite channel HEMTs fabricated using platinum (Pt) buried gate as the Schottky contact metal were evaluated for RF and logic application. After gate sinking at the  $250\text{ }^\circ\text{C}$  for 3 minutes, the current gain cutoff frequency  $f_T$  was increased from 390 GHz to 494 GHz after gate sinking at supply voltage of 0.6 V. These superior performances are attributed to the reduction of distance between gate and channel, and the reduction of parasitic gate capacitances during gate-sinking process.

## Structure and Layout of the Composited Channel

### InAs HEMT

Au electro-plating: 2.1  $\mu\text{m}$   
Height of Air-Bridge: 2.5  $\mu\text{m}$

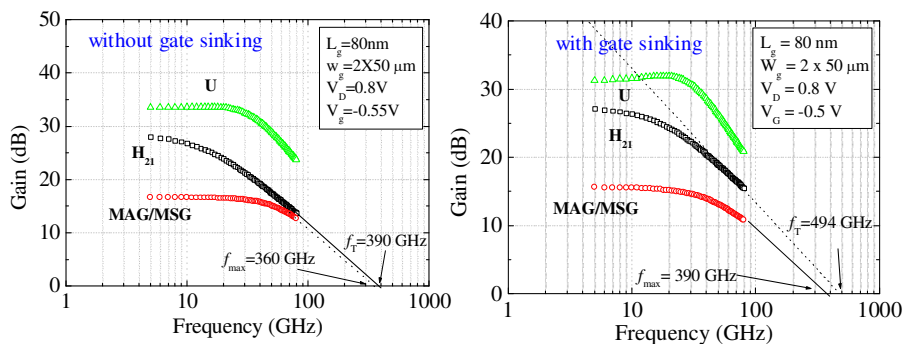
### Epitaxial Structures



Cap	n $\text{In}_x\text{GaAs}$ , $x = 0.53$
Etch stop layer	InP
Barrier	i $\text{In}_x\text{AlAs}$ , $x = 0.52$
$\delta$ doping	Si
Barrier	i $\text{In}_x\text{AlAs}$ , $x = 0.52$
Channel	$\text{In}_x\text{GaAs}$ , $x = 0.7$
Channel	InAs
Channel	$\text{In}_x\text{GaAs}$ , $x = 0.7$
Buffer	i $\text{In}_x\text{AlAs}$ , $x = 0.52$

2 Inch S. I. InP Substrate

## Improvement of RF Performance of InAs HEMTs by Gate Sinking



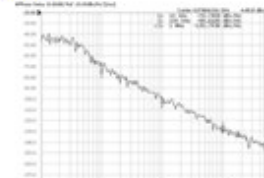
InAs/ $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ HEMTs	$C_{gs}$	$C_{gd}$	$C_{ds}$	$G_m(\text{RF})$	$f_T(\text{GHz})$	$f_{max}(\text{GHz})$
Without gate sinking	73.3 fF	16.3 fF	5.3 fF	201 mS	390 GHz	360 GHz
Gate sinking	60.5 fF	16.6 fF	3.7 fF	208 mS	494 GHz	390 GHz

(3) The 5 GHz Radio is demonstrated using the GaInP/GaAs HBT technology and several high performance RFICs are implemented. These demonstrated RFICs include interstage-matched gain-enhanced LNA, image-reject Gilbert VLIF downconverter with polyphase filter, Gilbert direct conversion sub-harmonic down-conversion mixers, Gilbert up-conversion mixers with output LC current mirror, low-phase-noise parallel-coupled quadrature VCOs and world class superharmonic-coupled QVCO. These RFICs show the potential of a fully integrated GaInP/GaAs HBT RF front-end total solution.

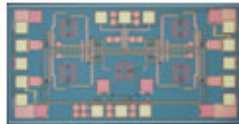
## High Performance GaInP/GaAs HBT Radio Frequency Integrated Circuits at 5 GHz (I)



- (1) Inter-stage matched LNA for gain enhancement
- (2) Three-level and two-level sub-harmonic mixers
- (3) Double Quadrature Image-reject Down-converter
- (4) Up-converter with LC current combiner
- (5) Parallel-coupled quadrature VCOs
- (6) Superharmonic-coupled quadrature VCOs



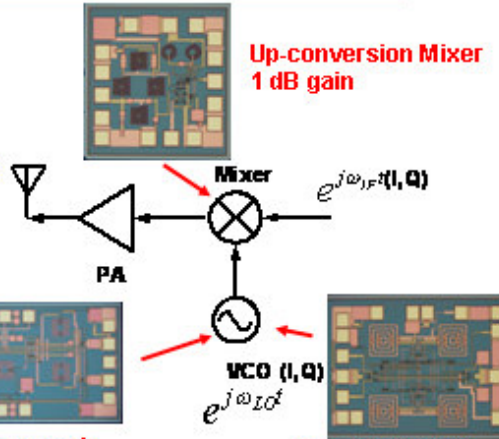
FOM: -197 dBc/Hz  
Phase noise: -131 dBc/Hz at 1 MHz offset



Superharmonic Coupled VCO

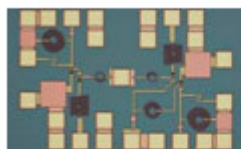


Up-conversion Mixer  
1 dB gain

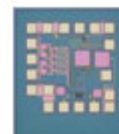


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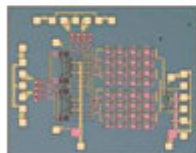
## High Performance GaInP/GaAs HBT Radio Frequency Integrated Circuits at 5 GHz (II)



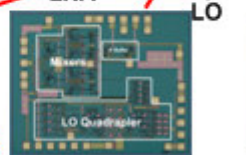
Inter-stage matched LNA  
19.5 dB Gain  
2.22 dB Noise Figure



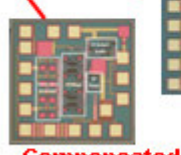
Two-level Bottom-LO Sub-harmonic Mixer  
0 dB Gain



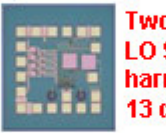
Double Quadrature Image-reject Down-converter  
40 dB Image Rejection



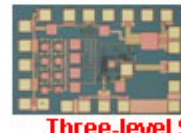
Dual-Band Weaver LO Quadrupler  
48 dB Image Rejection



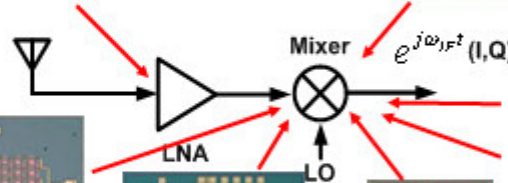
Compensated Sub-harmonic Mixer



Two-level Top-LO Sub-harmonic Mixer  
13 dB Gain



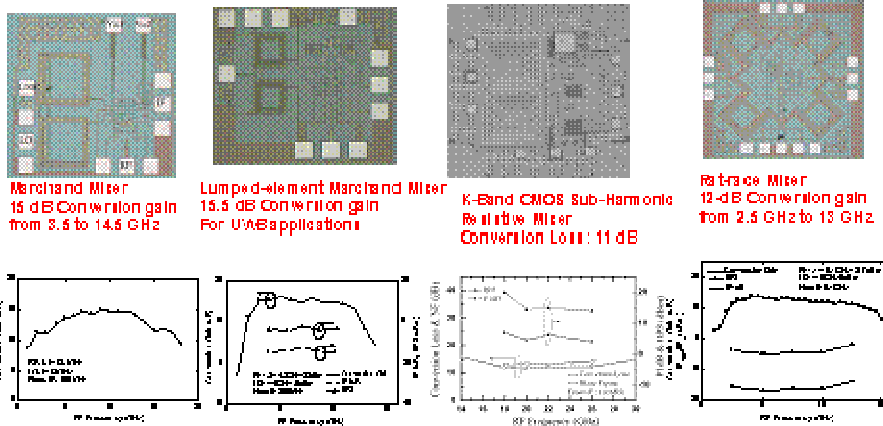
Three-level Stacked LO Sub-harmonic Mixer  
31 dB Gain



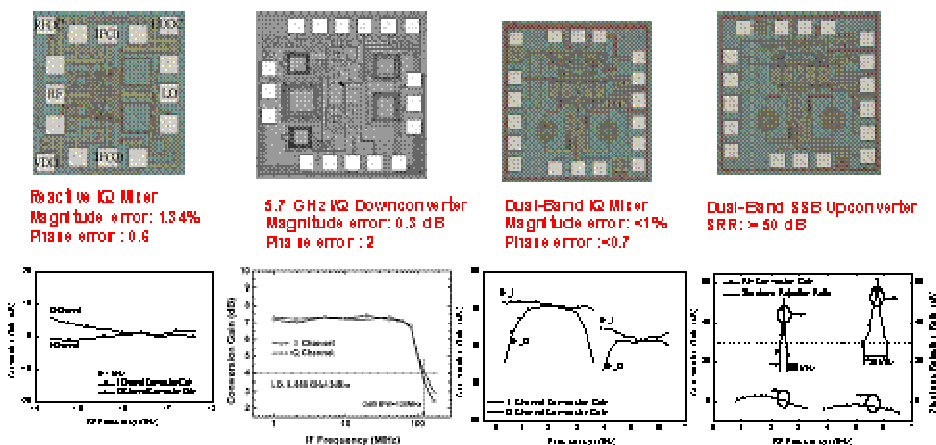
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National Chiao Tung University

- (4) Passive components like hybrids, baluns and couplers are implemented directly on a low-resistivity ( $\sim 10 \Omega \text{ cm}$ ) silicon substrate and merged into ICs for radio-frequency, microwave, and millimeter-wave applications. The demonstrations include wideband Marchand balun micromixer, UWB micromixer, IQ downconverter using a quadrature coupler, dual-band IQ downconverter with a reactive quadrature generator, and dual-band SSB upconverter with a reactive quadrature generator, rat-race mixer and Marchand balun resistive sub-harmonic mixer.

### Passive Components (Hybrids, and Baluns) Integrated into ICs Using Standard Silicon Process



### Passive Components (Quadrature Generators) Integrated into ICs Using Standard Silicon Process



# **Appendix V**

## **Self-Assessment**

**IX. APPENDIX V: SELF-ASSESSMENT (子計畫五)**

**PROGRAM TITLE: ADVANCED MICROWAVE TECHNOLOGIES FOR TELECOMMUNICATIONS**

**前瞻電信微波科技發展計畫**

**1. First Reviewer**

	<b>ASSESSMENT SUBJECT</b>	<b>SCORE (1~5, LOW TO HIGH)</b>
<b>PROGRAM'S CONTENTS &amp; PERFORMANCE</b>	Importance & Innovation of the Program's Major Tasks	
	Clarity and Presentation of the Report	
	Viability of the Program's Approaches & Methodologies	
	Program Director's Competence for Leading the Program	
	Interface & Integration between Overall & Sub-Project(s)	
	Interface & Integration among All Sub-Projects	
	Manpower & Expenditures	
<b>PROGRAM'S RESULTS</b>	Contribution in Enhancing the Institute's International Academic Standing	
	Impact on Advancing Teaching or on Technology Development	
	<b>OVERALL</b>	<b>4/</b>

**REVIEWER'S COMMENTS & SUGGESTION:**

1. Sub-project 5 concentrated on developing semi-conductor microwave devices in the range of a few hundred GHz.
2. The project is some what independent from the main integrated platform work. Rather, it focused on investigating various forward-looking techniques at the frontier of semi-conductor microwave device research.
3. The group has achieved some solid, good results in III-V devices and has done original work on III-V high mobility transistor on Si substrate.
4. The tech-transfer efforts of the group are rather impressive.
5. The work of the sub-project and that of sub-project S2 can be compared and see how the two efforts are complementary to each other.



## PROGRAM DIRECTOR'S FEEDBACK

### 委員一意見回覆：

1. Sub-project 5 concentrated on developing semi-conductor microwave devices in the range of a few hundred GHz.

Ans: 謝謝委員肯定。

2. The project is some what independent from the main integrated platform work. Rather, it focused on investigating various forward-looking techniques at the frontier of semi-conductor microwave device research.

Ans: 謝謝委員肯定。

3. The group has achieved some solid, good results in III-V devices and has done original work on III-V high mobility transistor on Si substrate.

Ans: 謝謝委員肯定。

4. The tech-transfer efforts of the group are rather impressive.

Ans: 謝謝委員肯定。

5. The work of the sub-project and that of sub-project S2 can be compared and see how the two efforts are complementary to each other.

Ans: 在此計畫中，著重於製程的開發，而子計畫二著重於高頻微波電路設計。在本計畫中亦有晶片實作成果，有別於子計畫二，實作的電路運用類比電路設計的觀念，操作頻率較為低頻，兩計畫有互補作用，此外除了製程開發，本計劃亦提供高頻電路所需的覆晶構裝技術，供子計畫二收發機整合使用。彼此相輔相成。



## 2. Second Reviewer

	ASSESSMENT SUBJECT	SCORE (1~5, LOW TO HIGH)
PROGRAM'S CONTENTS & PERFORMANCE	Importance & Innovation of the Program's Major Tasks	5
	Clarity and Presentation of the Report	4
	Viability of the Program's Approaches & Methodologies	5
	Program Director's Competence for Leading the Program	5
	Interface & Integration between Overall & Sub-Project(s)	3
	Interface & Integration among All Sub-Projects	3
	Manpower & Expenditures	5
PROGRAM'S RESULTS	Contribution in Enhancing the Institute's International Academic Standing	5
	Impact on Advancing Teaching or on Technology Development	5
	OVERALL	5

## **REVIEWER'S COMMENTS & SUGGESTION:**

1. 本計畫重點在研發 III-V 族半導體元件及 IC 技術，與其他子計畫的關連性與系統整合較弱，但不影響計劃的成就與學術卓越。
2. 主要成就包括
  - a. InAs HEMT ( $f_T > 500\text{GHz}$ )
  - b. 銅製程(III-V 族半導體製程)
  - c. 覆晶構裝技術，及相關連接技術
  - d. Si 製程被動元件與模擬整合技術

## PROGRAM DIRECTOR'S FEEDBACK

### 委員二意見回覆：

1. 本計畫重點在研發 III-V 族半導體元件及 IC 技術，與其他子計畫的關連性與系統整合較弱，但不影響計劃的成就與學術卓越。

Ans: 謝謝委員肯定與寶貴意見，未來將提高與其他子計畫的整合性。

2. 主要成就包括

a. InAs HEMT ( $f_T > 500\text{GHz}$ )

b. 銅製程(III-V 族半導體製程)

c. 覆晶構裝技術，及相關連接技術

d. Si 製程被動元件與模擬整合技術

Ans: 謝謝委員肯定。

### 3. Third Reviewer

	ASSESSMENT SUBJECT	SCORE (1~5, LOW TO HIGH)
PROGRAM'S CONTENTS & PERFORMANCE	Importance & Innovation of the Program's Major Tasks	4
	Clarity and Presentation of the Report	4
	Viability of the Program's Approaches & Methodologies	4
	Program Director's Competence for Leading the Program	4
	Interface & Integration between Overall & Sub-Project(s)	4
	Interface & Integration among All Sub-Projects	3.5
	Manpower & Expenditures	4.5
PROGRAM'S RESULTS	Contribution in Enhancing the Institute's International Academic Standing	5
	Impact on Advancing Teaching or on Technology Development	4.5
OVERALL		37.5

**REVIEWER'S COMMENTS & SUGGESTION:**

1. 本計畫主要發展 III-V 族半導體元件，最近幾年國外委託研究超出 1000 萬台幣，技轉國內廠商 8 家，已申請國內專利 16 件，國外專利 3 件，發表期刊論文 41 篇。

## **PROGRAM DIRECTOR'S FEEDBACK**

### **委員三意見回覆：**

1. 本計畫主要發展 III-V 族半導體元件，最近幾年國外委託研究超出 1000 萬台幣，技轉國內廠商 8 家，已申請國內專利 16 件，國外專利 3 件，發表期刊論文 41 篇。

Ans: 謝謝評審委員的肯定，本研究團隊，將繼續努力，在國際舞台上，實現卓越計畫的精神。

#### 4. Fourth Reviewer

	<b>ASSESSMENT SUBJECT</b>	<b>SCORE (1~5, LOW TO HIGH)</b>
<b>PROGRAM'S CONTENTS &amp; PERFORMANCE</b>	Importance & Innovation of the Program's Major Tasks	5
	Clarity and Presentation of the Report	4
	Viability of the Program's Approaches & Methodologies	5
	Program Director's Competence for Leading the Program	5
	Interface & Integration between Overall & Sub-Project(s)	3
	Interface & Integration among All Sub-Projects	4
	Manpower & Expenditures	4
<b>PROGRAM'S RESULTS</b>	Contribution in Enhancing the Institute's International Academic Standing	5
	Impact on Advancing Teaching or on Technology Development	5
	<b>OVERALL</b>	<b>40</b>

## **REVIEWER'S COMMENTS & SUGGESTION:**

### **COMMENTS :**

1. 子計畫 (S5) 開發微波半導體元件與電路前瞻技術，在論文發表上成果豐碩。國內外技轉及技服績效優異，為各子計畫之冠，請持續推廣應用。
2. Page 1：FY95、96 年經費實際支用遠低於核定數，而人力支應卻遠高於核定數，原因為何？請補充說明。
3. 請比照其他子計畫將民國 (FY9X) 統一採用公元 (FY200X)。

### **SUGGESTION :**

1. 請將計畫建案當 (2004) 年起規劃之 5 年以上技術路程圖 (Road map) 附上，以利審閱者明瞭技術的前瞻性及執行成效。
2. 本計畫成果具產業效益，請積極做好專利佈局及標準制定，以利行銷推廣及提高市場競爭力。



## PROGRAM DIRECTOR'S FEEDBACK

### 委員四意見回覆：

#### COMMENTS：

1. 子計畫（S5）開發微波半導體元件與電路前瞻技術，在論文發表上成果豐碩。國內外技轉及技服績效優異，為各子計畫之冠，請持續推廣應用。

Ans: 謝謝委員肯定與寶貴意見，將繼續努力加以落實。

2. Page 1：FY95、96年經費實際支用遠低於核定數，而人力支應卻遠高於核定數，原因為何？請補充說明。

Ans: FY95、96年經費支出，因採購在每年一月份並未完全交貨，而使用經費期限已延期至六月，儀器採購也陸續交貨，屆時經費使用將達成預期。而前三年實際支用為前一年度結案書面報告內容，計畫結束時之經費實際支用符合核定之經費支用。

在人力支應上，因培育人才與維持實驗室的運作，在製程開發上，需要龐大的研究人力，除了仰賴本計畫，許多人力經費的支出來自於學界科專的輔助，而在95、96年度，正處於第一階段科專結束與第二階段科專申請的過渡時期，為延續研究與開發，部分人力支應移轉至本計畫。

3. 請比照其他子計畫將民國（FY9X）統一採用公元（FY200X）。

Ans: 謝謝寶貴意見，將遵照辦理。

#### SUGGESTION：

1. 請將計畫建案當（2004）年起規劃之5年以上技術路程圖（Road map）附上，以利審閱者明瞭技術的前瞻性及執行成效。

Ans: 謝謝寶貴意見，將遵照辦理。如下頁。

2. 本計畫成果具產業效益，請積極做好專利佈局及標準制定，以利行銷推廣及提高市場競爭力。

Ans: 謝謝寶貴意見，將遵照辦理。數個專利持續申請中，提高本身的競爭力。

S5

交通大學複合物半導體實驗室毫米波元件開發及製作服務計畫時程

Task	Technology	Characteristics	93	93	93	94	94	94	94	95	95	95	95	96	96	96	96	97	97	97	97
			Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
1.0	pHEMT, Gate Length .2 um	Ft~80GHz, Fmax~100GHz																			
1.1	R and C Process Verify		▲	▽																	
1.2	開始提供 Test Key 試作			△	===	===	▽														
1.3	提供 MMIC 製作					◇	===	>													
2.0	pHEMT, Gate Length .15 um	Ft~100GHz, Fmax~120GHz																			
2.1	Gate Process Developing		▲	===	===	===	===	▽													
2.1	開始提供 Test Key 試作						△	===	===	▽											
2.1	提供 MMIC 製作								◇	===	>										
3.0	mHEMT, Gate Length .2 um	Ft~150GHz, Fmax~290GHz																			
3.1	元件製程、材料及模型研究開發		▲	===	===	===	===	===	===	===	===	===	▽								
3.2	開始提供 Test Key 試作									△	===	===	===	▽							
3.3	提供 MMIC 製作											◇	===	>							
4.0	mHEMT, Gate Length .15um	Ft~180GHz, Fmax~360GHz																			
4.1	Gate Process Developing											△	===	▽							
4.2	開始提供 Test Key 試作												△	===	===	▽					
4.3	提供 MMIC 製作													◇	===	>					
5.0	InP Based HBT	Ft~90GHz, Fmax~200 GHz																			
5.1	元件製程、材料及模型研究開發		▲	===	===	===	===	===	===	===	===	===	===	===	===	▽					
5.2	開始提供 Test Key 試作																	△	===	▽	
5.3	提供 MMIC 製作																			◇	==>