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Citation: Applied Physics Letters **91**, 132111 (2007); doi: 10.1063/1.2789788
View online: http://dx.doi.org/10.1063/1.2789788
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/91/13?ver=pdfcov
Published by the AIP Publishing

Realization of In_2O_3 thin film transistors through reactive evaporation process

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(Received 11 July 2007; accepted 5 September 2007; published online 27 September 2007)

In_2O_3 thin films have been grown by reactive evaporation of indium in ambient oxygen. The films were structurally characterized by x-ray diffraction (XRD) and atomic force microscopy techniques. The results of XRD revealed that the films were polycrystalline in nature with preferred (222) orientation. The as-grown films were subjected to various annealing treatments to modulate the conductivity of the films for thin film transistors (TFTs). TFTs fabricated on SiO_2 gate dielectric exhibited an on/off ratio of 10^4 and a field-effect mobility of 27 $cm^2/V\,s$. High on-state current makes them potential candidates for flat-panel display devices. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2789788]

Indium oxide (In_2O_3) is a *n*-type oxide semiconductor with a wide band gap (~3.6) at room temperature. Thin films of In_2O_3 are superior to other transparent oxide counterparts such as ZnO, CdO, and SnO_2, largely due to their high mobility of $10-75\ cm^2\ V^{-1}\ s^{-1}$ at a carrier density of $\sim 10^{19}-10^{20}\ cm^{-3}$.[1] It belongs to a complex cubic bixbyte structure with a lattice parameter $a=10.11$ Å.[2] The coexistence of high optical transmittance in the visible region and high electrical conductivity makes them potential candidate as active layers in thin film solar cells.[3] Moreover, the electrical property of this material could easily be controlled by simple heat treatments.[4] Such a heat treatment changes the composition of the film due to the annihilation of the oxygen vacancy, thereby leading to stoichiometric films.

Due to the large mobility and low processing temperatures, transparent amorphous oxide semiconductors have received much attention in the current research field of thin film transistors. Combinatorial approach[5] has been utilized by the earlier researchers to find a suitable material for the active channel layer, for example, In–Ga–Zn–O,[6] In–Zn–O,[7] Zn–Sn–O,[8] and In–Sn–O.[9] However, the different vapor pressures of the individual element lead to the difficulty in tuning the optimum composition and the reproducibility. Hence, finding a best composition becomes difficult in such a multicomponent systems. According to the earlier researchers, such a multicomponent system was necessary to reduce the electron background concentration and to enhance the channel resistivity. For example, to suppress the channel conductivity in In_2O_3, divalent Zn partially replaces In, i.e., 90 wt % In_2O_3 – 10 wt % ZnO and were reported in the literature.[10] Moreover, most of these multicomponent oxide TFTs reported in the literature were amorphous in nature. Perhaps it will be more interesting if undoped In_2O_3 could be used as a channel layer in its crystalline form. So the motivation of the present work is to utilize In_2O_3 as a channel layer in its undoped form. In the present article, we demonstrate the fabrication of undoped In_2O_3 thin film transistors without any external doping. This was feasible with a simple thermal evaporation technique in high purity oxygen ambient and the subsequent annealing treatments. In_2O_3 thin films are shown to be promising candidates as channel material with high mobility for the TFTs.

The cross-sectional view of the device structure used in the present work is presented in Fig. 1. Bottom gate TFTs were fabricated on heavily doped *n*-type silicon substrates with 300 nm of thermally oxidized silicon dioxide. A 20 nm In_2O_3 thin film was then deposited on SiO_2 gate dielectric through thermal evaporation process. Prior to the deposition, the chamber was pumped down to $\sim 10^{-6}$ Torr. Indium and oxygen of high purity were used as evaporation source and reactive gas, respectively. The flow rate of the gas was controlled by means of a mass flow controller. Subsequently, deposition was carried out at a partial pressure of $\sim 2 \times 10^{-4}$ Torr. The substrate temperature was fixed at 100 °C. The deposition rate (0.2 Å/s) and thickness (~20 nm) of the film were *in situ* monitored by means of quartz crystal monitor. The as-deposited films had a sheet resistance of 50 kΩ. The films were subjected to air annealing in the temperature range of 200–300 °C for 2 h to modulate the conductivity. Finally, silver source and drain electrodes were deposited onto the In_2O_3 channel layer by thermal evaporation through

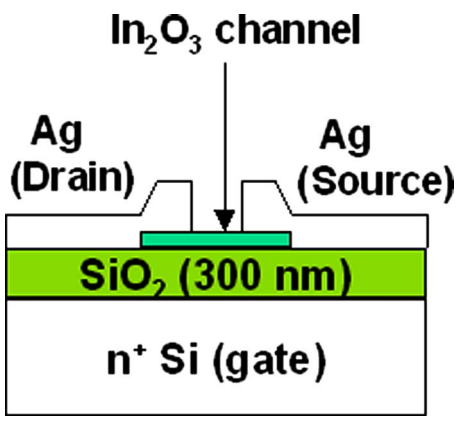

FIG. 1. (Color online) Schematic diagram of the In_2O_3 thin film transistor.

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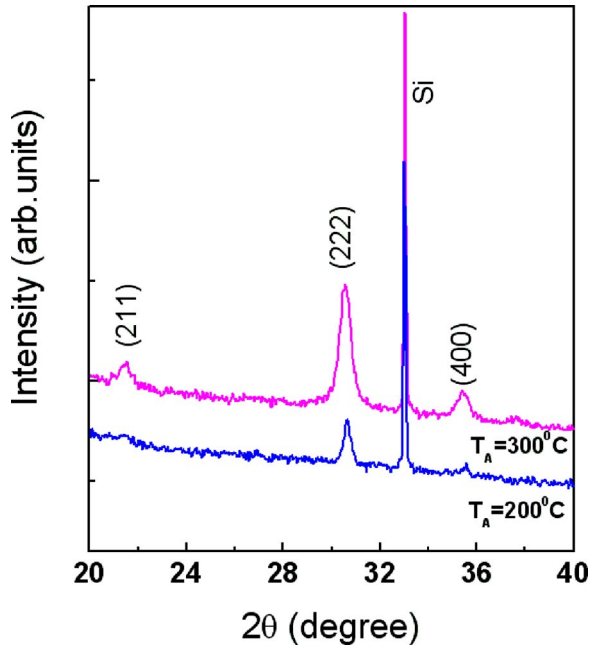

FIG. 2. (Color online) X-ray diffraction pattern of the In_2O_3 thin films annealed at different temperatures.

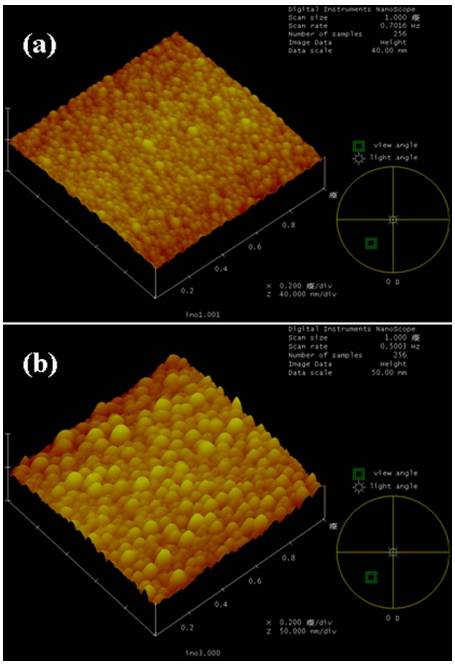

FIG. 3. (Color online) AFM images of the In_2O_3 thin films annealed for 2 h at (a) 200 °C and (b) 300 °C.

a mechanical shadow mask. The typical channel length and width were 100 and 2000 μm, respectively. To ensure better source and drain contacts on the In_2O_3 active channel layers, air annealing of the device was carried out at 200 °C for 15 min. The structure details of the In_2O_3 thin films were determined by x-ray diffraction using Cu Kα radiation. Atomic force microscopy was used to get an insight into the surface morphology and roughness of the films. A semiquantitative analysis of the film composition was carried out using energy-dispersive analysis of x rays. Electrical characterization of the film was carried out using an HP 4156 semiconductor parameter analyzer. Device testing was realized in a glovebox under N_2 environment.

Figure 2 shows the x-ray diffraction (XRD) pattern of the In_2O_3 thin films annealed at two different temperatures, namely, 200 and 300 °C for 2 h. The semitransparent as-deposited films were found to be amorphous in nature and hence, not displayed in Fig. 2. The air annealing of the samples at 200 and 300 °C induces crystallinity in the films and the films exhibited the preferred (222) orientation, confirming bixbyite structure.[11] The full width at half maximum (FWHM) of (222) diffraction peak was 0.48° and 0.32° for the films annealed at 200 and 300 °C, respectively. Such a small FWHM ensures the high quality of the films. Moreover, the composition of the films was measured using the energy dispersive analysis of x rays and it was found that the ratio of O/In is well above the stoichiometric value (=1.5) (Ref. 12) for In_2O_3, indicating excess of oxygen in the films. Such a composition (In=27 and O=73 at. %) was desirable for getting the proper channel resistivity for the TFTs.

Atomic force microscopy (AFM) image of the In_2O_3 thin films that were annealed at 200 and 300 °C for the TFT fabrication are displayed in Figs. 3(a) and 3(b), respectively. To compare the smoothness of the films annealed at different temperatures, their root-mean-square (rms) roughness was analyzed. The films were atomically smooth and dense grain morphology was observed. The surface roughness plays a major role in the device performance and it has been reported in the literature.[13] It has been found that the active channels with minimal surface roughness leads to better device performance.[14,15] The rms roughness of the films derived from AFM was around 1.4 and 4.2 nm for the films annealed at 200 and 300 °C, respectively. It was found that the thin film transistors fabricated with In_2O_3 thin films grown at 300 °C exhibited a large leakage current and hence poor on/off ratio (data not shown) compared to the films grown at 200 °C. This is mainly due to the higher surface roughness of the samples grown at 300 °C compared to the films grown at 200 °C and earlier researchers have observed such a phenomena previously.[14] The rms roughness and the relative intensity of the (222) peak (Fig. 2) have shown a similar variation with annealing temperature and such phenomena were observed in Sn doped In_2O_3 systems by the earlier researchers..[16] Hence, the surface roughness plays a major role in the performance of the device and the annealing temperature of 200 °C was found to be optimal for the better performance of the device. Moreover, increase in grain size with increase in annealing temperature was observed. In other words, there was a decrease in the grain boundary density due to the agglomeration of the grains, which leads to decrease in grain boundary scattering of the carriers. This, in turn, results in increase in the conductivity. Hence, the overall carrier concentration of the films increases drastically with the increased grain size and the channel becomes too conductive, thereby resulting in a poor on/off ratio and a large leakage current of the device. Hence, from the AFM investigations, it infers that air-annealing temperature of 200 °C is desirable for the In_2O_3 thin films for getting better performance of the device.

Figure 4 shows the representative drain-source current (I_D) as a function of drain to source voltage (V_{DS}) at various gate voltages of the In_2O_3 based TFTs with SiO_2 gate insulators. Typical channel width (W) to length (L) ratio used in the present study, i.e., W/L was 20. The I_D-V_{DS} curve indicates that the drain current increases with increase in gate

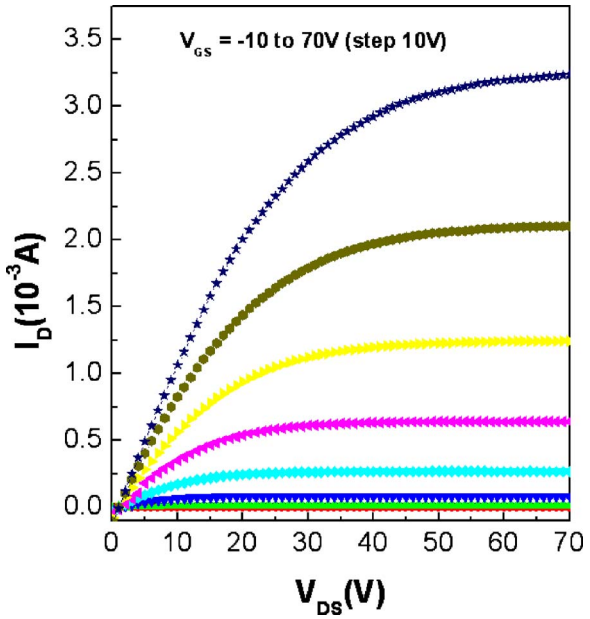

FIG. 4. (Color online) Drain current-drain voltage (I_D-V_{DS}) characteristics of In_2O_3 thin film transistors.

voltage, exhibiting the apparent field effect. The transistor operates in *n*-type depletion mode and exhibits a well-defined pinch-off and saturation region. The channel resistivity of ~10 Ω cm was calculated from the linear slope of the output characteristics at zero gate voltage. Similar to most of the inorganic oxide TFTs, such as ZnO,[17] the fabricated In_2O_3 TFTs obey the standard field-effect transistor theory, with the Fermi level in the channel fully modulated by the gate and the drain voltages. Moreover, the device had a high output current of the order of milliamperes, which makes it a promising candidate for devices such as smart cards, electric motors and light emitting diodes.

Figure 5 shows the variation of I_{DS} as a function of V_{GS} at a fixed drain voltage. The typical on/off ratio of 10^4 was estimated. The threshold voltage and field-effect mobility in the saturated regime were estimated using the following relation:

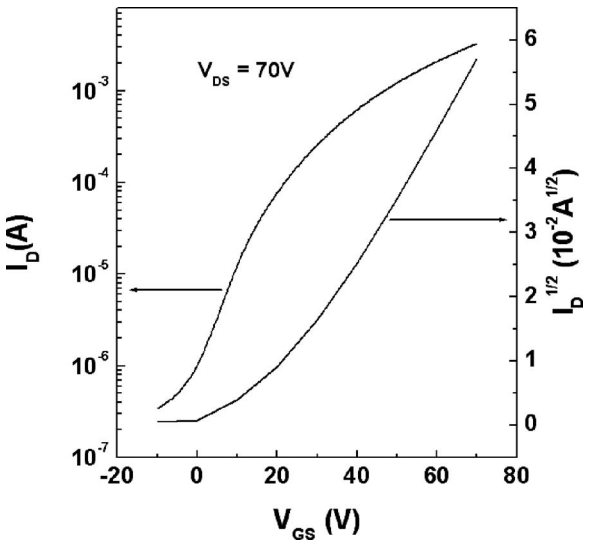

FIG. 5. Source to drain current as a function of gate voltage (V_{GS}) at a fixed drain voltage of 70 V.

$$I_D = \frac{WC_i\mu_{FE}}{2L}(V_{GS} - V_T)^2, \quad (1)$$

where C_i is the capacitance per unit area of the gate dielectric, V_T is the threshold voltage, and μ_{FE} is the field-effect mobility. The threshold voltage and the field effect mobility computed from the *x*-axis intercept of the square root of I_D versus V_{GS} plot and the slope of the plot were found to be 10.5 V and 27 $cm^2/V/s$, respectively. The obtained value of mobility was one order magnitude order higher than those obtained for indium-zinc-oxide systems reported in the literature.[18] This could be mainly attributed to (i) the crystalline phase of the In_2O_3 thin films used in the present study and (ii) reduced scattering centers for the carriers across the drain and source, since there are no external dopants in undoped In_2O_3 films.

In conclusion, we demonstrate that In_2O_3 thin films form a promising *n*-channel material for transparent TFTs. The devices were fabricated at low substrate temperature by reactive evaporation technique. The variation of surface roughness with annealing temperature was analyzed and it was observed that the film with minimal surface roughness is desirable for the TFTs. Transistors utilizing SiO_2 gate dielectric demonstrate good operating characteristics with an on/off ratio of 10^4, a high field-effect mobility, and an output current. Thus, In_2O_3 seems to be a viable active channel material for the emerging field of transparent thin film transistors.

The authors are grateful to the National Science Council (NSC), Taiwan (96-2221-E-001-017-MY2) and the Thematic Project of Academia Sinica, Taiwan for financial support.

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