AIP Applied Physics Letters

Formation of Ge nanocrystals using Si 1.33 Ge 0.67 O 2 and Si 2.67 Ge 1.33 N 2 film for nonvolatile memory application

Wei-Ren Chen, Ting-Chang Chang, Yen-Ting Hsieh, Simon M. Sze, and Chun-Yen Chang

Citation: Applied Physics Letters **91**, 102106 (2007); doi: 10.1063/1.2779931
View online: http://dx.doi.org/10.1063/1.2779931
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/91/10?ver=pdfcov
Published by the AIP Publishing

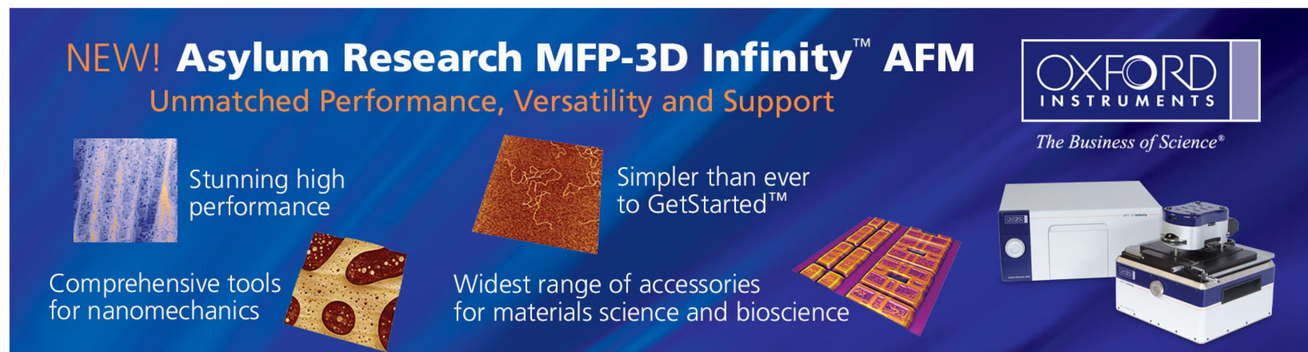
Articles you may be interested in
Noise Sources of a Si 1 x Ge x O y Microbolometers And Their Reduction By Forming Gas Passivation
AIP Conf. Proc. **1129**, 375 (2009); 10.1063/1.3140477

Planar-type spin valves based on low-molecular-weight organic materials with La 0.67 Sr 0.33 Mn O 3 electrodes
Appl. Phys. Lett. **92**, 153304 (2008); 10.1063/1.2905288

Mechanisms of arsenic segregation to the Ni 2 Si SiO 2 interface during Ni 2 Si formation
Appl. Phys. Lett. **87**, 181910 (2005); 10.1063/1.2125124

Ca F 2 Si Ca F 2 resonant tunneling diodes grown by B surfactant-mediated epitaxy
Appl. Phys. Lett. **86**, 033111 (2005); 10.1063/1.1853522

High depth resolution Secondary Ion Mass Spectrometry (SIMS) analysis of Si 1x Ge x :C HBT structures
AIP Conf. Proc. **550**, 672 (2001); 10.1063/1.1354474



This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 00:08:08

Formation of Ge nanocrystals using $Si_{1.33}Ge_{0.67}O_2$ and $Si_{2.67}Ge_{1.33}N_2$ film for nonvolatile memory application

Wei-Ren Chen
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

Ting-Chang Chang[a)]
Department of Physics and Institute of Electro-Optical Engineering, Center for Nanoscience and Nanotechnology, National Sun Yat-set University, 70 Lien-hai Road, Kaohsiung 804, Taiwan, 70 Lien-hai Road, Kaohsiung 804, Taiwan

Yen-Ting Hsieh, Simon M. Sze, and Chun-Yen Chang
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

(Received 20 July 2007; accepted 15 August 2007; published online 4 September 2007)

The authors proposed a formation mechanism of Ge nanocrystals embedded in the dielectric by using $Si_{1.33}Ge_{0.67}O_2$ and $Si_{2.67}Ge_{1.33}N_2$ films for nonvolatile memory application in this study. Because of internal competition reaction, this formation process reduced the thermal budget and eliminated the use of high pressure H_2 treatment or steam process. In this research, the preannealing capping oxide step is a critical process for nonvolatile memory effect. Transmission electron microscope shows the shape and density of nanocrystals in the dielectric. Moreover, the memory structure with Ge nanocrystal embedded in SiN_x has better charge storage ability and data retention than Ge nanocrystal embedded in SiO_x. *© 2007 American Institute of Physics*.
[DOI: 10.1063/1.2779931]

The nonvolatile memory (NVM) for portable electronic productions is an important industrial semiconductor because of its superiority in low-power consumption, low cost, high-memory capacity, and enough data retention.[1,2] The conventional NVM with floating gate (FG) structure, however, cannot efficaciously prevent data loss in terms of reliability trials for future scaling down process.[3,4] Due to the discrete charge storage nodes acting as charge trapping layer to reform drawbacks of conventional FG memory, the NVMs using various semiconductor nanocrystals have been widely investigated in the past few years, such as silicon (Si), germanium (Ge), and zinc oxide (ZnO) nanocrystals.[2,5] Moreover, the Ge nanocrystal has better memory performance than Si and ZnO nanocrystals because of its smaller energy band gap ($\sim$0.6 eV) and higher dielectric constant ($\sim$16.0, i.e., stronger coupling with the conduction channel). According to the current research, the self-assembled and direct growth of Ge nanocrystals embedded in SiO_2 layer has successfully been implemented.[2,6] The self-assembled method was reported by many previous studies because it could control better density and size of nanocrystals than direct growth.[2,7] Nevertheless, the self-assembled method must need a high temperature ($\sim$900–1100 °C) with long duration ($\sim$30–60 min) oxidation process to anneal the charge trapping layer which is generally deposited by various ratios of SiGe layer, and an overoxidation phenomenon of Ge nanocrystals is often obtained after foregoing oxidation process.[8] Hence, a redox step must be added to the formation flow of Ge nanocrystal by using an additional high pressure H_2 treatment or steam process.[9,10]

We therefore undertook a different line of investigation to shun the disadvantages of self-assembled method and reduce thermal budget. Our investigation focused on the use of silicon-germanium oxide (SiGeO) and silicon-germanium nitride (SiGeN) thin films to form high density and good spatial distribution of Ge nanocrystals embedded in the dielectric for NVM application. In this letter, we also found that preannealing capping oxide (PACO) was a critical step for formation and electronic characteristics of Ge nanocrystals.

The fabrication of NVM structure was started with a thermal dry oxidation at 950 °C to form a tunnel oxide about 5 nm on *p*-type (100) Si wafer which had been removed native oxide and particles by RCA process, and then a 10-nm-thick charge tapping layer was deposited by reactive sputtering of $Si_{0.5}Ge_{0.5}$ alloy target in the Ar/O_2 [24/2 SCCM (SCCM denotes cubic centimeter per minute at STP)] ambiance at room temperature. This step could obtain a $Si_{1.33}Ge_{0.67}O_2$ layer which the ratio of atom concentration was analyzed by x-ray photoelectron spectroscopy. Besides, we used nitrogen (N_2, 20 SCCM) to act for O_2 to form $Si_{2.67}Ge_{1.33}N_2$ layer during sputtering process in order to lead in nitride improved charge storage ability.[11] Before rapid thermal annealing (RTA) process at 900 °C for 30 s in the N_2 ambiance, the $Si_{1.33}Ge_{0.67}O_2$ and $Si_{2.67}Ge_{1.33}N_2$ layers must be capped by a 20-nm-thick oxide using a plasma enhanced chemical vapor deposition (PECVD) system at 300 °C (this step was called PACO). The RTA process was performed to cause the self-assembly of Ge nanocrystal in the charge trapping layer. After RTA process, a 20-nm-thick blocking oxide was deposited by PECVD and then deposited Al gate electrodes to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Transmission electron microscope (TEM) analysis was assumed for microstructure of Ge nanocrystals. Electrical characteristics of the capacitance-voltage (*C-V*) hysteresis were also measured by HP4284 precision *LCR* meter with high frequency of 1 MHz.

Figure 1 shows the electrical characteristics of *C-V* hysteresis under ±10 gate voltage operation with (1) Ge nanocrystal embedded in SiO_x (use of PACO step), (2) Ge nano-

[a)]Electronic mail: tcchang@mail.phys.nsysu.edu.tw

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 00:08:08

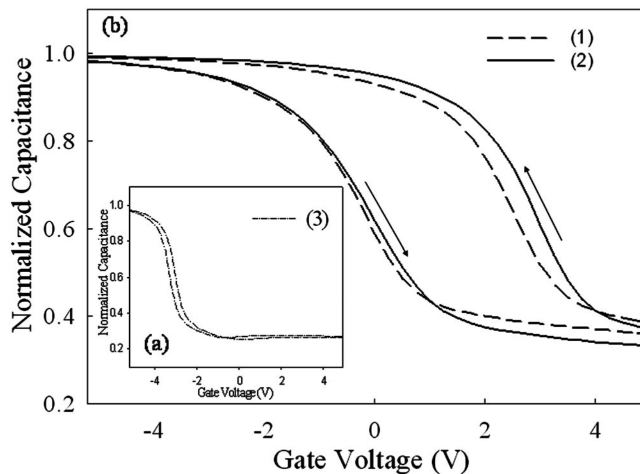


FIG. 1. Capacitance-voltage (C-V) hysteresis of MOIOS structure under ±10 gate voltage operation with (a) (3) Ge nanocrystal embedded in SiO_x (no use of PACO step) and (b) (1) Ge nanocrystal embedded in SiO_x (use of PACO step) and (2) Ge nanocrystal embedded in SiN_x (use of PACO step). PACO: preannealing capping oxide.

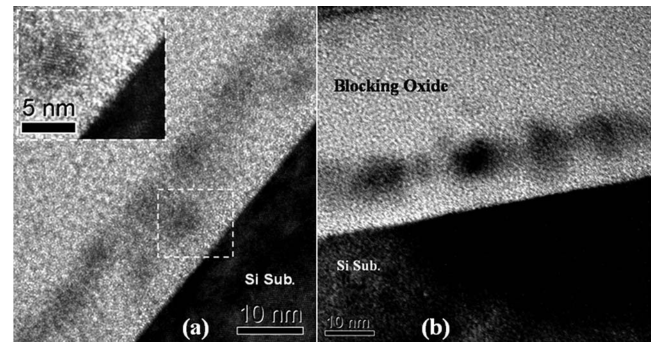


FIG. 3. Cross-sectional transmission electron microscope (TEM) analysis of MOIOS structure with (a) Ge nanocrystal embedded in SiO_x (the nanocrystal size and density are about 5–6 nm and 1.73×10^{12} cm^{-2}, respectively) and (b) Ge nanocrystal embedded in SiN_x (the nanocrystal size and density are about 7–8 nm and 1.12×10^{12} cm^{-2}, respectively.)

crystal embedded in SiN_x (use of PACO step), and (3) Ge nanocrystal embedded in SiO_x (no use of PACO step). In this case, memory window for C-V measurement was influenced by PACO process, as shown in Fig. 1(a), because the Ge atoms of charge trapping layer had outdiffused phenomenon during RTA process by secondary ion mass spectrometer (SIMS) analysis, as shown in Fig. 2.[12,13] Hence, we must use the PACO step to avoid Ge atom outdiffusion and keep higher Ge concentration in the charge trapping layer to get better charge storage ability. From Fig. 1(b), it is found that the memory windows of (1) and (2) exhibit 2.8 and 3.2 V, respectively. Due to the electronic property of SiN_x (e.g., high dielectric constant and additional trapping states), structure (2) has better charge efficiency than structure (1).

Figure 3(a) shows a cross-sectional TEM image of structure (1) containing spherical and separated Ge nanocrystals. The average diameter of the nanocrystals is approximately 5–6 nm and the area density of the nanocrystals is estimated to be about 1.73×10^{12} cm^{-2} by TEM analysis. For the formation of Ge nanocrystals, the Gibbs free energy of Si–O and Ge–O at 900 °C, are about −805 and −666 kJ mol^{-1}, respectively.[14] Because of the smaller Gibbs free energy of Si–O compared with Ge–O, the oxygen atoms can interact with Si atom easier than with Ge atom in the $Si_{1.33}Ge_{0.67}O_2$ layer during the RTA process. It can be considered that an internal competition reaction will induce self-assembled of Ge nanocrystals in the $Si_{1.33}Ge_{0.67}O_2$ layer, which is dependent on the amount of oxygen of charge trapping layer. Therefore, Ge nanocrystals could be formed at lower thermal budget and no use of further high pressure H_2 treatment or steam process in our experimental method.

We also use the internal competition reaction for $Si_{2.67}Ge_{1.33}N_2$ layer to form Ge nanocrystal embedded in SiN_x, as shown in the cross-sectional TEM image of Fig. 3(b). The average diameter of the nanocrystals is approximately 7–8 nm and the area density of the nanocrystals is estimated to be about 1.12×10^{12} cm^{-2} by TEM analysis. Besides, the charge trapping layer contains SiN_x matrix which increase trapping states to improve charge storage capacity [as shown in Fig. 1(b)] and program/erase efficiency.

The retention of nonvolatile nanocrystal memory structure with (1) and (2) are illustrated in Fig. 4. The retention mensuration was performed at room temperature by operating a ±15 V gate voltage stress for 10 s and measured up to

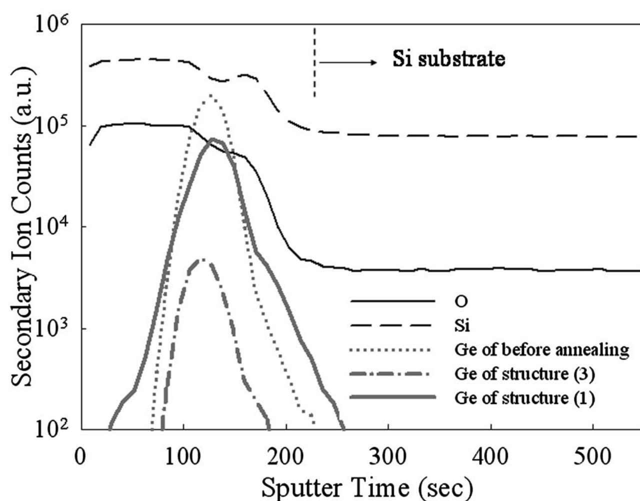


FIG. 2. Secondary ion mass spectrometer (SIMS) analysis of MOIOS structure with Ge of before annealing, Ge of structure (3) (no use of PACO step), and Ge of structure (1) (use of PACO step).

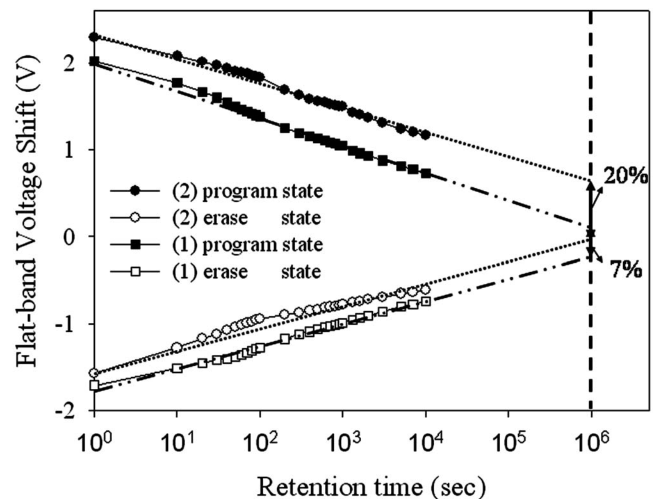


FIG. 4. Retention with structure (1) Ge nanocrystal embedded in SiO_x and structure (2) Ge nanocrystal embedded in SiN_x at room temperature operating at ±15 V gate voltage stress for 10 s. The charge holding ratio of structure (1) is 7% and that of structure (2) is 20% after 10^6 s.

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 00:08:08

10^4 s. The flatband voltage shift (ΔV_{fb}) was obtained by comparing the *C-V* curves from a charged carrier state and the quasineutral state. We find that the charge holding ratio of structure (2), 20%, is better than that of structure (1), 7%, after 10^6 s by analyzing the extrapolation value of retention data [dotted dashed line for (1) and dotted line for (2) of Fig. 4]. Because structure (2) provided trapping states of SiN_x for charging carriers, this result could reduce the Coulomb blockade effect of charge trapping layer leading to lower tunneling probability between tunnel oxide and conduction channel under retention state.[15] Hence, the nanocrystals combined with SiN_x matrix can improve the performance of nonvolatile nanocrystal memory in our investigation.

In conclusion, we successfully fabricated the Ge nanocrystals embedded in the dielectric by using the self-assembled characteristics of $Si_{1.33}Ge_{0.67}O_2$ and $Si_{2.67}Ge_{1.33}N_2$, and cut down thermal budget. The overoxidation phenomenon of Ge nanocrystals could be prevented through different Gibbs free energies of compounds. The Ge nanocrystals combined with SiN_x matrix showed better electronic performance for nonvolatile memory application. In addition, this fabrication technique can be compatible with current manufacturing process of the integrated circuit.

This work was performed at National Nano Device Laboratory and was supported by the National Science Council of the Republic of China under Contract Nos. NSC 95-2221-E-009-283, NSC 95-2221-E-009-270, NSC 95-2120-M-110-003, and NSC 95-2221-E-009-254-MY2. Furthermore, this work was partially supported by MOEA Technology Development for Academia Project No. 94-EC-17-A-07-S1-046 and MOE ATU Program "Aim for the Top University" No. 95W803.

[1] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, Proc. IEEE **91**, 4 (2003).
[2] J. D. Blauwe, IEEE Trans. Nanotechnol. **1**, 72 (2002).
[3] C. Y. Lu, T. C. Lu, and R. Liu, *Proceedings of 13th IPFA*, (IEEE, New York, 2006), pp. 18–23.
[4] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, Tech. Dig. - Int. Electron Devices Meet. **1995**, 521.
[5] J. H. Jung, J. Y. Jin, I. Lee, T. W. Kim, H. G. Roh, and Y. H. Kim, Appl. Phys. Lett. **88**, 112107 (2006).
[6] M. Kanouna, A. Souifib, T. Baron, and F. Mazen, Appl. Phys. Lett. **84**, 5079 (2004).
[7] T. C. Chang, S. T. Yan, P. T. Liu, C. W. Chen, S. H. Lin, and S. M. Sze, Electrochem. Solid-State Lett. **7**, G17 (2004).
[8] T. C. Chang, S. T. Yan, P. T. Liu, C. H. Hsu, M. T. Tang, and S. M. Sze, Appl. Phys. Lett. **84**, 2581 (2004).
[9] G. Taraschi, S. Saini, W. W. Fan, and L. C. Kimerling, J. Appl. Phys. **93**, 9988 (2003).
[10] C. H. Tu, T. C. Chang, P. T. Liu, H. C. Liu, S. M. Sze, and C. Y. Chang, Appl. Phys. Lett. **89**, 162105 (2006).
[11] Y. Yang, A. Purwar, and M. H. White, Solid-State Electron. **43**, 2025 (1999).
[12] S. K. Stanley, S. S. Coffee, and J. G. Ekerdt, Appl. Surf. Sci. **252**, 878 (2005).
[13] J. T. Law and P. S. Meigs, J. Electrochem. Soc. **104**, 154 (1957).
[14] J. D. Cox, D. D. Wagman, and V. A. Medvedev, *CODATA Key Values for Thermodynamics* (Hemisphere, New York, 1989), p. 271.
[15] C. Lee, T. H. Hou, and E. C. Kan, IEEE Trans. Electron Devices **52**, 12 (2005).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 00:08:08