Current-Scaling a-Si:H TFT Pixel-Electrode Circuit for AM-OLEDs: Electrical Properties and Stability

Hojin Lee, Yen-Chung Lin, *Member, IEEE,* Han-Ping D. Shieh, *Senior Member, IEEE,* and Jerzy Kanicki, *Senior Member, IEEE*

***Abstract*—We fabricated and characterized the hydrogenate amorphous-silicon thin-film transistor (a-Si:H TFT) pixel-electrode circuit with the current-scaling function that can be used for active-matrix organic light-emitting displays (AM-OLEDs). As expected from previously reported simulation results, the fabricated pixel-electrode circuit showed an enhanced current-scaling performance for a high-resolution AM-OLED based on a-Si:H TFTs in comparison to other types of current-driven pixel circuits. It also showed a better electrical and thermal stability for different OLED current levels in comparison to the conventional current–driven pixel-electrode circuit.**

***Index Terms*—Active-matrix organic light-emitting display (AM-OLED), current program, current scaling, hydrogenate amorphous silicon (a-Si:H), pixel-electrode circuit, thin-film transistor (TFT).**

I. Introduction

OVER THE LAST several years, it was shown by several authors [1]–[5] that the current-driving pixel-electrode circuits are among the most desirable solutions for active-matrix organic light-emitting displays (AM-OLEDs). However, as display size and resolution increase, a large timing delay can be observed at a low data current, and its importance increases with the display size [6]. To address this issue, several solutions have been proposed based on polycrystalline-silicon thin-film-transistor (TFT) technology, such as current-mirror circuit [7], [8] and series-connected TFT circuit [9]. Besides poly-Si TFTs, Sakariya *et al.* [10] reported the hydrogenate amorphous silicon TFT (a-Si:H TFT) pixel-electrode circuit based on the current-mirror circuit. We also proposed a-Si:H TFT-based current-scaling pixel-electrode circuit to address this problem [6], [11]. In this paper, for the first time, we report on electrical characteristics of the fabricated pixel-electrode circuit based on this design and present its current-scaling function in comparison with the previously published results. We also demonstrate the electrical and thermal stability of the fabricated pixel-electrode circuit in comparison to the conventional current-driven TFT circuit.

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H. Lee and J. Kanicki are with the Organic and Molecular Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor 48109 USA (e-mail: kanicki@eecs.umich.edu).

Y.-C. Lin and H.-P. D. Shieh are with the Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

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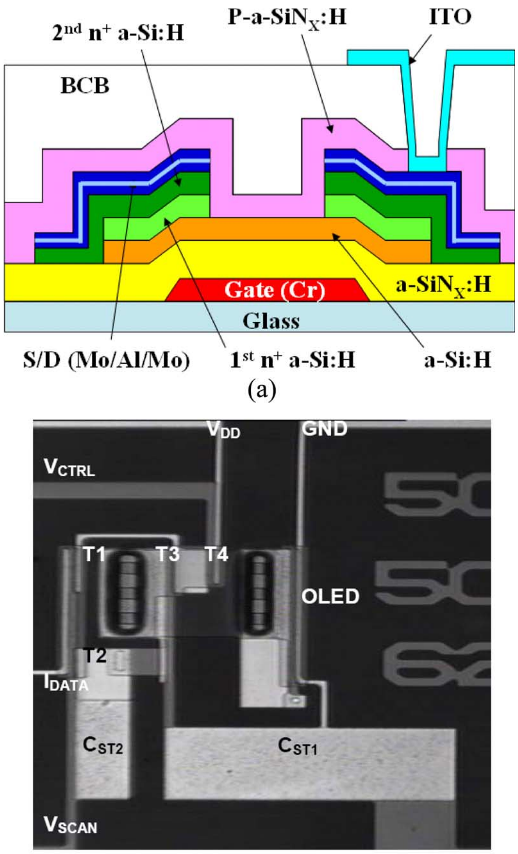
II. Fabrication of Pixel Electrode Circuits

First, chrome layer (Cr, 2000 Å) was deposited on glass substrate by a sputtering method and then was patterned by photolithography process using wet-etching CR-7 solution (Mask #1) to define gate electrodes. After soaking in GP:H_2O (1:15), acetone, and methanol, the substrate was rinsed in de-ionized (DI) water for 10 min and, finally, blown dry with N_2 gas. Trilayer that is composed of hydrogenate amorphous silicon nitride (a-SiN_X:H, 3000 Å)/(intrinsic a-Si:H, 1500 Å)/ first P-doped a-Si:H layer (n^+ a-Si:H, 200 Å) was deposited next in multichamber plasma-enhanced chemical-vapor deposition (PECVD) system at the substrate temperature of 300 °C. A gas mixture of SiH_4 and NH_3, and SiH_4 and H_2 was used for a-SiN_X:H- and a-Si:H-layer deposition, respectively. First, 200-Å-thick n^+ a-Si:H layer was used to achieve a good source/ drain (S/D) ohmic contact to a-Si:H. After definition of the device active island by wet etching (Mask #2), substrate was dipped in HF solution to remove native oxide before deposition of a second n^+ a-Si:H layer (300 Å), which was used to realized an ohmic contact to edges of the a-Si:H island. Next, molybdenum/aluminum/molybdenum (Mo/Al/Mo, 1000 Å/3000 Å/ 1000 Å) multilayer was deposited by thermal coater, and metal S/D contacts were defined by wet etching (Mask #3). Acetone supersonic solution was used to remove positive photoresist. Using S/D metal as a mask, the back-channel etching was performed by reactive-ion etching (RIE) to remove exposed n^+ a-Si:H layer between source and drain contacts. Finally, a-SiN_X:H (3000 Å) top passivation layer (P) was deposited by PECVD method followed by spin coating of the benzo-cyclo-butene (BCB) planarization layer that was cured in a furnace at 250 °C in nitrogen ambient. Planarized a-Si:H TFTs by BCB were already reported previously [12], [13]. The pixel-electrode indium tin oxide (ITO) was connected to S/D using via formed through the BCB/P-a-SiN_X:H bilayer by RIE (Mask #4). ITO (1200 Å) was deposited by a dc magnetron sputtering at room temperature and patterned by wet etching (Mask #5) in a mixture of HCl, HNO_3, and DI water at 60 °C [14]. Finally, ITO was thermally annealed at 250 °C in nitrogen. The cross section of the a-Si:H TFT is shown in Fig. 1(a).

III. Operation of the Fabricated Current-Scaling Pixel-Electrode Circuit

The fabricated current-driven pixel-electrode circuit consists of three switching TFTs (T1, T2, and T4), one driving TFT (T3), and two storage capacitors (C_{ST1} and C_{ST2}) connected between a scan line and ground (GND) with a cascade structure



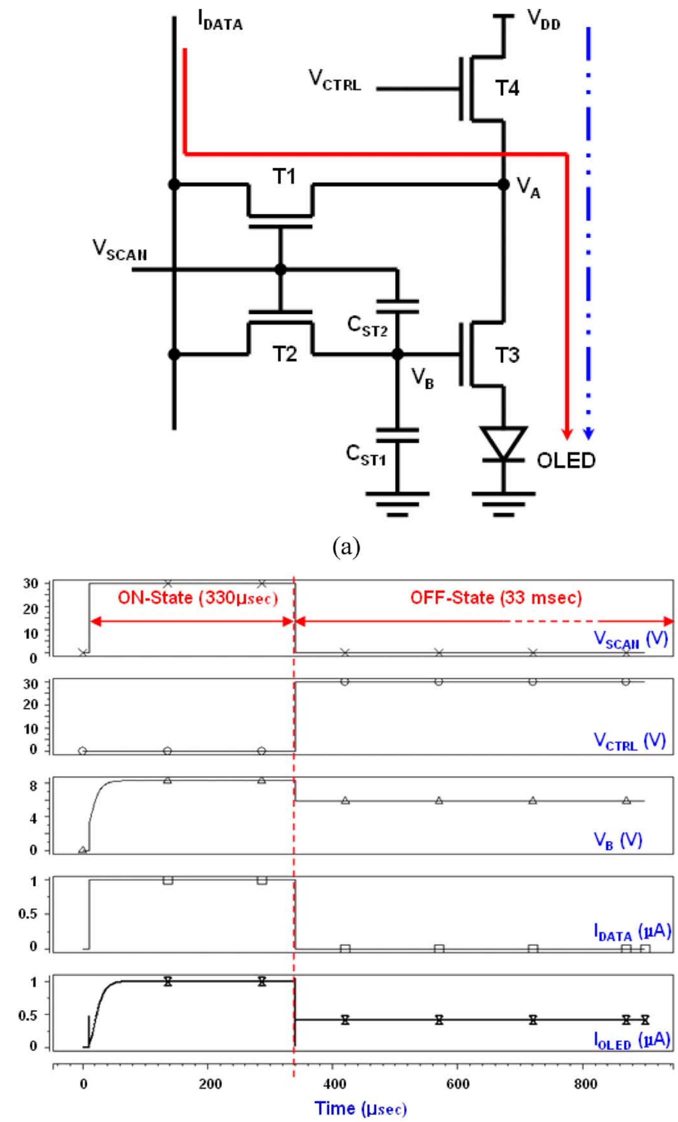
(a)

(b)

Fig. 1. Schematic cross section and top view of the fabricated a-Si:H TFT pixel-electrode circuit.

[Figs. 1(b) and 2(a)]. The OLED is represented here by a-Si:H TFT with gate and drain connected together, and the device parameters are summarized in Table I(a). Here, we define $I_{\mathrm{OLED-ON}}$ and $I_{\mathrm{OLED\text{-}OFF}}$ as the current flowing through OLED during the ON- and OFF-state, respectively. During the ON-state, V_{SCAN} turns on the T1 and T2, and $I_{\mathrm{DATA}}(= I_{\mathrm{OLED\text{-}ON}})$ passes through T1 and T3 to OLED while the T4 remains turned-off by V_{CTRL}, which is shown as the solid line in Fig. 2(a). When the pixel changes from the ON- to OFF-state, V_{SCAN} turns off T1 and T2, and V_{CTRL} simultaneously turns on T4. Since gate bias of T3 ($V_{\mathrm{B\_ON}}$) is reduced to $V_{\mathrm{B\_OFF}}$ by the ratio of cascaded capacitor ($V_{\mathrm{B\_OFF}} = V_{\mathrm{B\_ON}} - \Delta V_{\mathrm{SCAN}} \cdot C_{\mathrm{ST2}}/(C_{\mathrm{ST1}} + C_{\mathrm{ST2}})$), a scaled-down data current ($I_{\mathrm{OLED\_OFF}}$) will flow through OLED, which is shown as the dashed line in Fig. 2(a). To achieve the accurate current scaling by the ratio C_{ST2} and C_{ST1}, we need to consider a parasitic capacitance effect on V_{B} node potential. Per our previously published discussion [6], when the overlap parasitic capacitance of T2 ($C_{\mathrm{OV-T2}}$) is considered, $I_{\mathrm{OLED\text{-}OFF}}$ can be expressed as

$$\begin{aligned} I_{\mathrm{OLED\text{-}OFF}} &= \beta(V_{\mathrm{GS}} - V_{\mathrm{TH}} - V_{\mathrm{offset}})^2 \\ &= \beta\left(\sqrt{\frac{I_{\mathrm{OLED\text{-}ON}}}{\beta}} - V_{\mathrm{offset}}\right)^2 \\ &= I_{\mathrm{OLED\text{-}ON}} - 2\sqrt{\beta \cdot I_{\mathrm{OLED\text{-}ON}}} \\ &\quad \cdot V_{\mathrm{offset}} + \beta \cdot V_{\mathrm{offset}}^2 \end{aligned} \quad (1)$$



(a)

(b)

Fig. 2. Schematic of (a) cascaded-capacitor pixel-electrode circuit and (b) operational waveforms simulated by HSPICE.

with

$$V_{\mathrm{B\text{-}OFF}} = V_{\mathrm{B\text{-}ON}} - V_{\mathrm{offset}}$$

where

$$V_{\mathrm{offset}} = \Delta V_{\mathrm{SCAN}} \frac{C_{\mathrm{ST2}} \| C_{\mathrm{OV}\text{-}T2}}{C_{\mathrm{ST1}} + C_{\mathrm{ST2}} \| C_{\mathrm{OV}\text{-}T2}} \quad (2)$$

where $\beta = 1/2\mu_{\mathrm{FE}} \cdot C_{\mathrm{OX}} \cdot W_{T3}/L_{T3}$. As shown in the equation, since the parasitic capacitance of T2 is connected to C_{ST2} in parallel, when the status of T2 is changed from ON to OFF, a kickback effect can occur. The kickback effect is defined here as the abrupt drop of $V_{\mathrm{B\text{-}OFF}}$ originated from the charge sharing between the parasitic and the storage capacitances. To prevent this effect, we designed and fabricated T2 as small as possible. Hence, we could minimize this effect in pixel-circuit operation. More details of the analysis of this pixel-circuit operation can be found in [6].

TABLE I
LISTING OF THE DEVICE GEOMETRICAL PARAMETERS USED IN (a) PROPOSED CASCADE-CAPACITOR [FIG. 1(a)], (b) CONVENTION CURRENT-DRIVEN [FIG. 5(a)], AND (c) CURRENT-MIRROR [FIG. 5(b)] PIXEL-ELECTRODE CIRCUITS

Proposed pixel circuit	
W/L (T1, T3) [μm]	50/4
W/L (T2) [μm]	30/4
W/L (T4) [μm]	40/4
W/L OLED [μm]	150/4
C_{ST1} [pF]	2.5
C_{ST2} [fF]	210 / 312 / 625

(a)

Conventional current-driven pixel circuit	
W/L (T1, T2, T3) [μm]	100/4
W/L (T4) [μm]	150/4
W/L OLED [μm]	150/4
C_{ST} [pF]	2.5

(b)

Current-mirror pixel circuit	
W/L (T1, T2) [μm]	100/4
W/L (T3) [μm]	200/4
W/L (T4) [μm]	50/4
W/L OLED [μm]	150/4
C_{ST} [pF]	2.5

(c)

IV. PIXEL-ELECTRODE-CIRCUIT MEASUREMENT DETAILS

To analyze the electrical performance of the pixel circuit, we measured $I_{\text{OLED-ON}}$ and $I_{\text{OLED-OFF}}$ flowing through the OLED by applying I_{DATA}, V_{CTRL}, and V_{SCAN}, as shown in Fig. 2(b). At the same time, constant dc V_{DD} and GND were applied. All measurements were done at room temperature, and all signals were applied using HP8110A function generator through a probe station. The time for ON- and OFF-state was set to 0.33 and 33 ms, respectively. During the ON-state, V_{SCAN} and V_{CTRL} were held at 30 and 0 V, respectively, while I_{DATA} was swept from 0.2 to 10 μA for each measurement. During the OFF-state, V_{SCAN} and V_{CTRL} were changed to 0 and 30 V, respectively, while I_{OLED} was measured with V_{DD} set at 30 V. It should be noted that the I_{DATA} must be turned off when the circuit operation changes from ON- to OFF-state. Otherwise, the measured V_{DATA}, when I_{DATA} is supplied, will increase to a high value ($>$ 40 V) to keep the current flowing when T1 and T2 are turned off, since the probe of I_{DATA} is set to the current supply mode. This high V_{DATA} can result in a large T2 leakage current, which increase the voltage at node B ($V_{\text{B\_OFF}}$). Accordingly, the $I_{\text{OLED\_OFF}}$ will also increase since $V_{\text{B\_OFF}}$ increases.

Therefore, for proper circuit operation, I_{DATA} should be turned off during OFF-state, as shown in Fig. 2(b). However, even though the I_{DATA} was turned off, the measured $I_{\text{OLED\_OFF}}$ decreased slightly during OFF-state due to T2 current leakage, which originated from the voltage difference between source and drain electrodes. This current leakage causes the $V_{\text{B\_OFF}}$ to decrease. To reduce the variation of $V_{\text{B\_OFF}}$, the following steps were taken: 1) The value of V_{DATA} during ON-state was measured while supplying dc I_{DATA}. Since the resistance of T1 was very small during ON-state, the voltage at node B ($V_{\text{B\_ON}}$) was expected to be the same as measured V_{DATA}. 2) Then, V_{DATA} obtained in step 1) was applied instead of I_{DATA} on the data line during ON-state. Since the V_{DATA} was the same as $V_{\text{B\_ON}}$ and it would supply the same current as I_{DATA}, the voltage levels during OFF-state between source and drain of T2 could be very similar so that the T2 leakage current was negligible and I_{OLED} was stable during OFF-state. When this pixel circuit is used in a display active-matrix array, in ideal case, the potential of V_B node should not change with the scan line addressing. However, in practice, due to the leakage current through T2, varying V_{DATA} can introduce a variation of V_B, resulting in the vertical crosstalk. This effect can be prevented by inserting TFT in series between data line and the common node of T1 and T2 drain.

V. ELECTRICAL PROPERTIES OF THE CURRENT-SCALING PIXEL-ELECTRODE CIRCUIT

To investigate the current scaling ratio of the fabricated pixel-electrode circuit, we changed the I_{DATA} from 0.2 to 10 μA and measured the corresponding $I_{\text{OLED\_ON}}$ and $I_{\text{OLED\_OFF}}$ flowing through the diode for different ratios of cascaded capacitors. In ON-state, the $I_{\text{OLED\_ON}}$ is identical to the data current (I_{DATA}), since the external driver directly controls the OLED current [Fig. 3(a)]. When the pixel circuit operates in OFF-state, the diode current ($I_{\text{OLED\_OFF}}$) is scaled-down by the ratio of cascade capacitor, as discussed above and in [11]. From Fig. 3(b), it is obvious that the larger $C_{\text{ST2}}/C_{\text{ST1}}$ results in significant decrease of the $I_{\text{OLED\_OFF}}$ at lower I_{DATA}. However, as shown previously [11], a very large ratio of $C_{\text{ST2}}/C_{\text{ST1}}$ ($>$ 1/3) resulted in the saturation of $I_{\text{OLED\_OFF}}$, which, eventually, deteriorate the current scaling function.

Since the OLED current value is different during ON- and OFF-state, we define the average OLED current (I_{AVE}) during one frame time [11] as $I_{\text{AVE}} = (I_{\text{OLED\_ON}} \cdot t_{\text{ON}} + I_{\text{OLED\_OFF}} \cdot t_{\text{OFF}})/(t_{\text{ON}} + t_{\text{OFF}})$, where t_{ON} and t_{OFF} is the ON- and OFF-period during the frame time, respectively. The variation of I_{AVE} versus I_{DATA} in one frame period ($t_{\text{ON}} + t_{\text{OFF}}$) for different $C_{\text{ST2}}/C_{\text{ST1}}$ ratios is shown in Fig. 3(c). Since the OFF-state period is much longer than ON-state, though $I_{\text{OLED\_OFF}}$ is very small during OFF-state, it can reduce the I_{AVE} even if the $I_{\text{OLED\_ON}}$ ($= I_{\text{DATA}}$) is large. For example, the fabricated pixel-electrode circuit can generate I_{AVE} ranging from 2 nA to 5 μA, while I_{DATA} swept from 0.2 to 10 μA. Therefore, during one frame time, we can achieve a very wide dynamic range of OLED current levels by supplying high data current levels.

The evolution of the scaling ratio ($R_{\text{SCALE}} = I_{\text{OLED-ON}}/I_{\text{OLED-OFF}}$) for different ratios of $C_{\text{ST2}}/C_{\text{ST1}}$ as a function of I_{DATA} is shown in Fig. 4(a). In this figure, we can see that, for $C_{\text{ST2}}/C_{\text{ST1}} = 1/4$, R_{SCALE} decreases from 816 to 1.9 as I_{DATA} increases from 0.2 to 10 μA, and an ideal nonlinearity of R_{SCALE} can be achieved, e.g., a very high R_{SCALE} at low I_{DATA} levels (low gray scales) and a low R_{SCALE} at high I_{DATA} levels (high gray scales) can be produced. The variation of R_{SCALE} with the $C_{\text{ST2}}/C_{\text{ST1}}$ is also shown in Fig. 4(b). The measured results show that, for

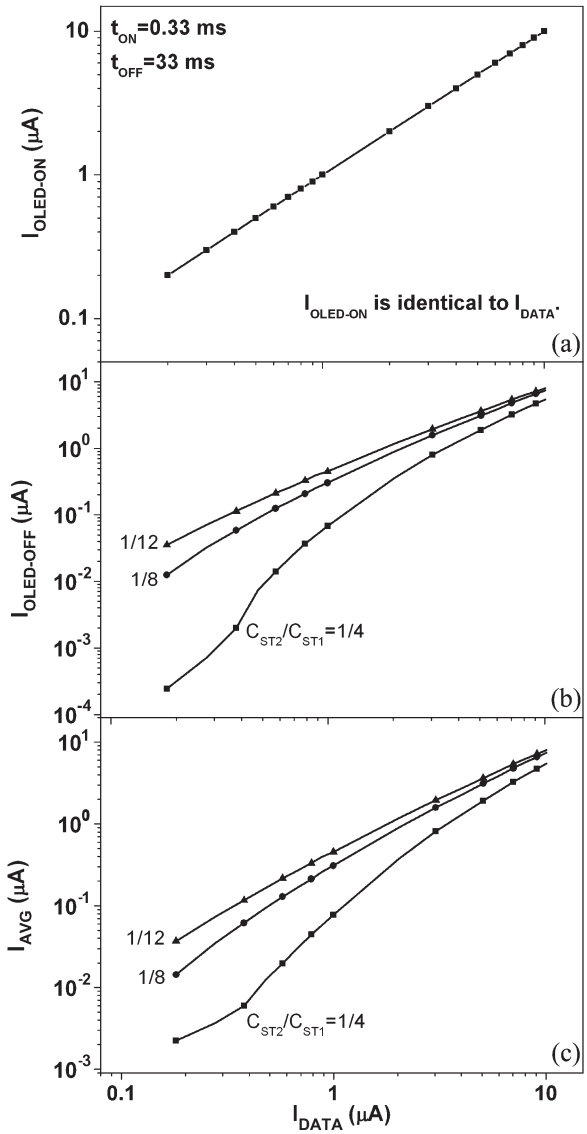


Fig. 3. Variation of the measured $I_{\mathrm{OLED\_ON}}$, $I_{\mathrm{OLED\_OFF}}$, and I_{AVE} as a function of I_{DATA} ($= I_{\mathrm{OLED\_ON}}$) for various $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ ratios.

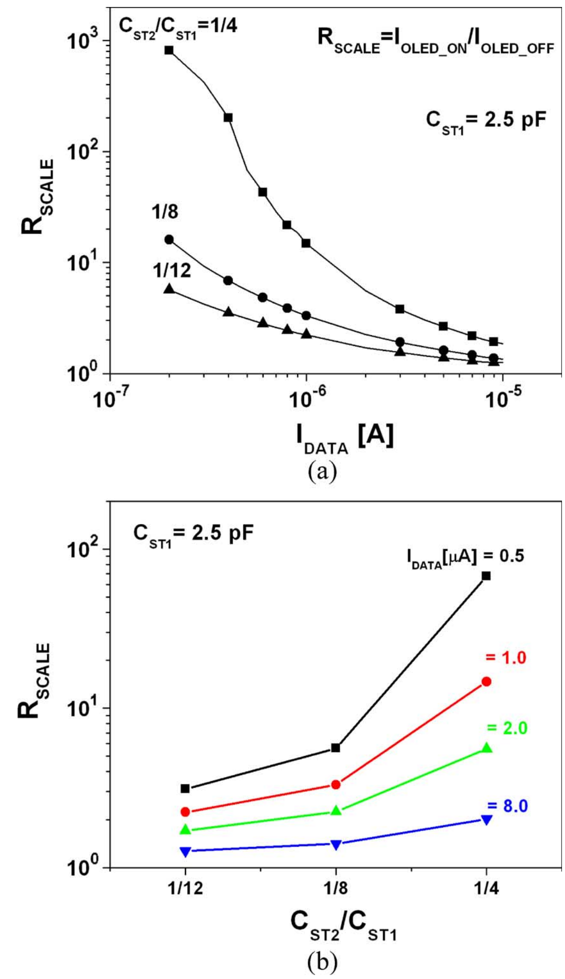


Fig. 4. Variation of the measured current-scaling ratio as a function of (a) I_{DATA} and (b) ratio of storage capacitances for fabricated cascaded-capacitor pixel circuit.

fixed I_{DATA}, R_{SCALE} increases as C_{ST2} increases from 210 to 625 fF, corresponding to an increase of $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ from 1/12 to 1/4. For constant $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$, R_{SCALE} increases as I_{DATA} decreases, as shown in Fig. 4(a). Therefore, for a fixed ratio of $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ calculated for a given pixel-electrode circuit design, we can expect to achieve a certain output OLED current range. These experimental results are in full agreement with the simulated results previously reported [11].

VI. Comparison With Other Pixel-Electrode Circuits

To demonstrate the current-scaling function of the proposed pixel-electrode circuit in comparison with both conventional current-driven [4] and current-mirror pixel circuits [7], we fabricated all three pixel-electrode circuits using the same a-Si:H TFT technology, as shown in Figs. 1 and 5. The device parameters of transistors and capacitors used in different pixel-electrode circuits are summarized in Table I. Then, we measured I_{AVE} as a function of I_{DATA} for each pixel-electrode circuit, as shown in Fig. 6. Since $I_{\mathrm{OLED\_ON}}$ for all three circuits was identical to I_{DATA}, the current-driven circuit did not show any current-scaling function. On the contrary, while the current-mirror circuit showed only a fixed current-scaling by the ratio of T4/T3 over all I_{DATA} range ($I_{\mathrm{OLED}} = (W_4 \cdot L_3)/(L_4 \cdot W_3) \cdot I_{\mathrm{DATA}}$), the proposed cascaded-capacitor pixel circuit showed nonlinear current-scaling function for variable current-scaling ratio depending on I_{DATA}. When I_{DATA} varies from 2×10^{-7} to 10^{-5} A, the proposed cascaded-capacitor pixel circuit with the ratio of $C_{\mathrm{ST2}}/C_{\mathrm{ST1}} = 1/4$ can provide I_{AVE}, ranging from 2×10^{-9} to 5.4×10^{-6} A. Hence, much wider dynamic range of I_{AVE} levels can be achieved by this circuit in comparison with the conventional current-driven pixel circuit (2×10^{-7} to 10^{-5} A) and the current-mirror pixel circuit (10^{-8} to 2×10^{-6} A).

VII. Electrical Stability of the Fabricated Pixel-Electrode Circuit

A. A-SI:H TFT Stability Measurement

To evaluate the thermal and electrical stability of our fabricated pixel-electrode circuit, we performed the

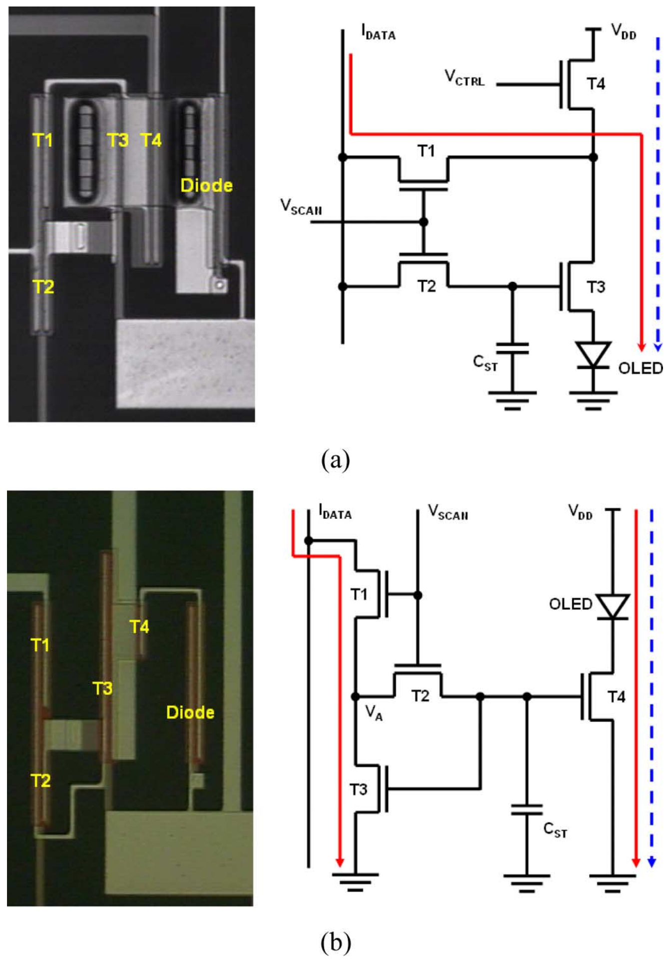


Fig. 5. Top view of fabricated (a) conventional current-driven and (b) current-mirror pixel-electrode circuits based on a-Si:H TFTs.

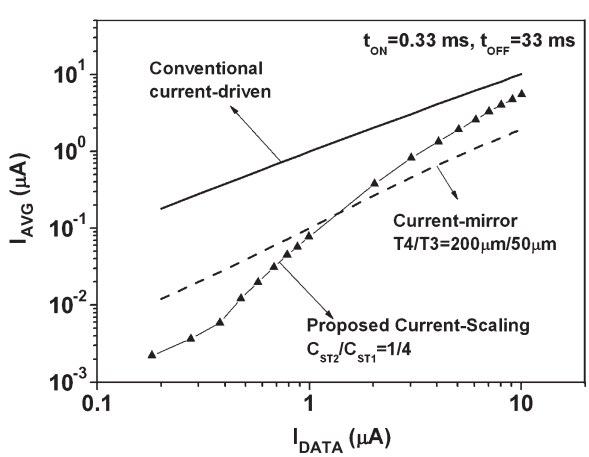


Fig. 6. Comparison of I_{AVE} versus I_{DATA} for conventional current-driven, current-mirror, and proposed pixel circuits.

current–temperature-stress (CTS) experiment for both single TFT and pixel-electrode circuit (Fig. 7). For the single TFT CTS measurement, we applied a constant gate bias of 30 V ($V_{\mathrm{GS}} = 30$ V) continuously to the TFT while the drain–current was set to 2.0 μA ($I_{\mathrm{DATA}} = 2.0$ μA) and measured the transfer characteristics of TFT with $V_{\mathrm{DS}} = 10$ V at room temperature (25 °C) for different stressing times (t_{ST}) ranging from 0 to

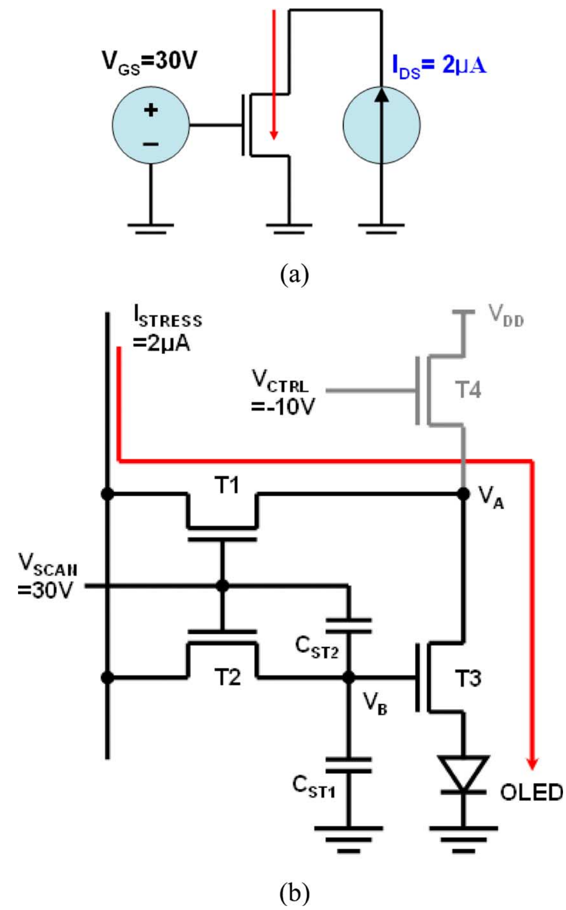


Fig. 7. Schematics of the CTS measurement setup used for (a) single a-Si:H TFT and (b) proposed pixel-electrode-circuit stability study.

20 000 s [Fig. 8(a)]. The stress-current value of 2.0 μA was determined to achieve the luminance of 500 $\mathrm{cd/m^2}$ when the emission efficiency of OLED is 2.5 cd/A for the pixel size of 100×100 $\mu\mathrm{m}^2$. We only stopped device stressing to measure the transfer curves between stress times. We also measured the transfer characteristics of TFT under the accelerated stress condition by raising the stress temperature (T_{ST}) up to 85 °C, while all bias conditions remained the same ($V_{\mathrm{GS}} = 30$ V and $I_{\mathrm{DATA}} = 2$ μA). As shown in Fig. 8(b), the transfer curve changes dramatically with the increasing stress time when the temperature is set at 85 °C. From the transfer characteristics, the threshold voltages are extracted by the maximum slope method [15] for different stressing times and temperatures. As the stressing time increases from 0 to 20 000 s, the threshold-voltage shift (ΔV_{TH}) at 25 °C increases from 0 to 1.98 V, while ΔV_{TH} at 85 °C increases from 0 to 13.99 V [Fig. 9(a)]. At the same time, the field-effect mobility (μ_{FE}) at 85 °C decreases from 0.68 to 0.52 $\mathrm{cm^2/V \cdot s}$, while μ_{FE} at 25 °C shows small variation from 0.34 to 0.32 $\mathrm{cm^2/V \cdot s}$ with the stress time. It should be noted that the subthreshold swing at 85 °C shows small variation while it does not change at 25 °C with the stress time, which can be related to the increase of the interface states at 85 °C with the stress time. The detailed mechanism responsible for these variations of TFT characteristics were discussed in the previous study [16]. All device measurements were done at the stress temperature.

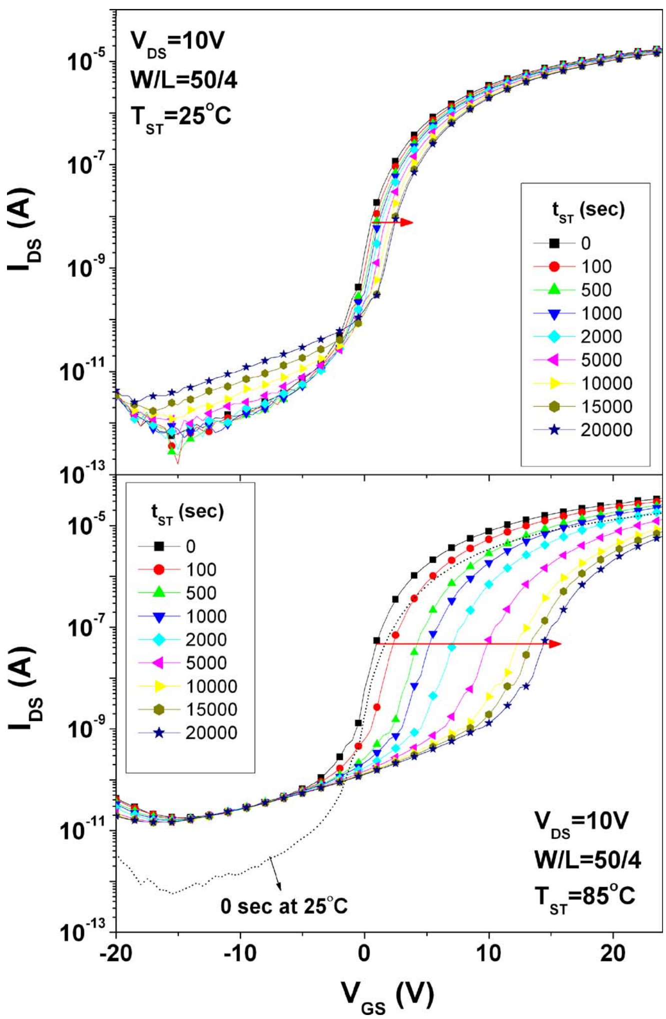


Fig. 8. Transfer characteristic of TFT ($W/L = 50/4$) after current-stress ($I_{\mathrm{DATA}} = 2\ \mu$A) as a function of stress time (a) at room temperature (25 °C) and (b) at 85 °C.

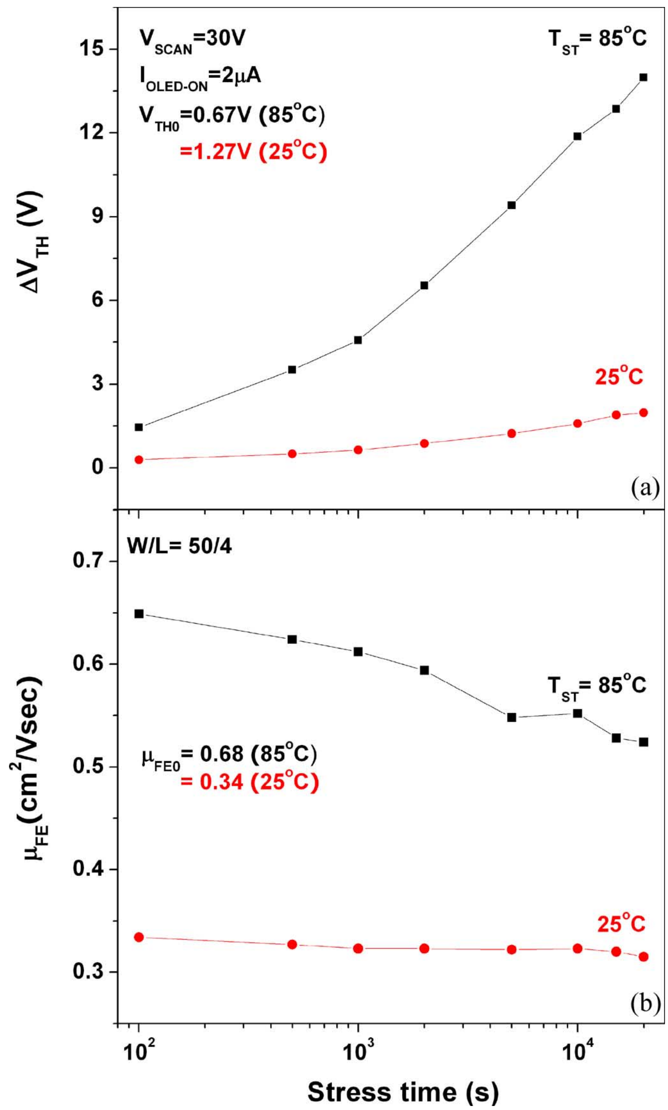


Fig. 9. Variations of threshold voltage and field-effect mobility of a-Si:H TFT ($W/L = 50/4$) as a function of stress time at 25 °C and 85 °C.

B. Pixel-Electrode Circuit Stability Measurement

Based on the CTS measurement conditions specified above, we evaluated the stability of the fabricated pixel-electrode circuit as a function of the bias stress time. For an accelerating stress condition, the stress temperature of the glass substrate was set up at 85 °C. Then, we set the scan and control bias as 30 and -10 V, respectively ($V_{\mathrm{SCAN}} = 30$ V and $V_{\mathrm{CTRL}} = -10$ V). To stress the pixel-electrode circuit, the data current (I_{DATA}) of 2 μA was supplied to the data electrode during various stress times from 0 to 20 000 s. After each current stress, we changed the bias condition to the normal measurement setup described previously and measured the OLED OFF-current ($I_{\mathrm{OLED\text{-}OFF}}$) for various data current levels ($I_{\mathrm{DATA}} = 0.2$, 1.0, and 5.0 μA) to investigate the stress effect on the OLED current behavior. For the direct comparison, we performed the CTS measurement of the conventional current-driven circuit [4] under the same experimental conditions. Fig. 10 shows the variation of $I_{\mathrm{OLED\text{-}OFF}}$ ($\Delta I_{\mathrm{OLED\text{-}OFF}}$) of the proposed pixel-electrode circuit as a function of the threshold-voltage shift (ΔV_{TH}) in comparison to the conventional current-driven pixel circuit. In Fig. 10, the threshold-voltage shift (x-axis) is the converted value from the stressing time based on the driving TFT CTS measurement at 85 °C [Fig. 8(b)].

$$\Delta V_{\mathrm{TH}} = V_{\mathrm{TH}}(t_{\mathrm{ST}}) - V_{\mathrm{TH}}(t_{\mathrm{ST}} = 0). \tag{3}$$

As expected, $\Delta I_{\mathrm{OLED\text{-}OFF}}$ of the proposed circuit is very small ($< 1.5\%$) at high data current levels ($= 5.0\ \mu$A) regardless of TFT threshold-voltage shift. However, as expected, at low current levels ($= 0.2\ \mu$A), the $I_{\mathrm{OLED\text{-}OFF}}$ shows a significant deviation ($> 40\%$) as the TFT threshold-voltage shift increases over 10 V. Nevertheless, if we compare the measured results with the previously published simulated results [6] for the TFT threshold-voltage shift ranging from 0 to 4 V, they showed a similar variation of the $I_{\mathrm{OLED\text{-}OFF}}$ ($< 10\%$) for low data current levels ($= 0.2$ and 1.0 μA), as shown in Fig. 10. In general, the proposed pixel-electrode circuit shows a smaller deviation of the $I_{\mathrm{OLED\text{-}OFF}}$ ($\Delta I_{\mathrm{OLED-OFF}}$) than the conventional current-driven pixel circuit for the same TFT threshold-voltage shift value, which means that the proposed pixel-electrode circuits have a slightly better electrical and thermal stability for

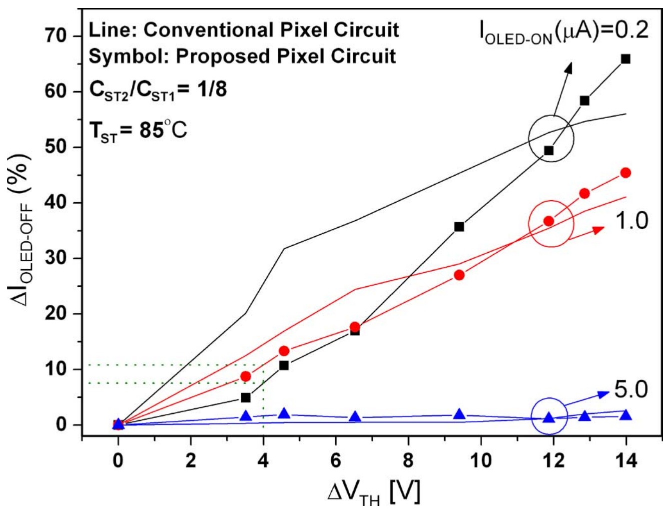


Fig. 10. Variations of the OLED OFF-current ($\Delta I_{\mathrm{OLED\text{-}OFF}}$) of the proposed pixel circuit as a function of threshold-voltage shift (ΔV_{TH}) at 85 °C in comparison to the conventional current-driven pixel circuit.

low I_{OLED} levels in comparison with the conventional current-driven pixel circuit.

The stability issues of the proposed a-Si:H TFT pixel circuit can be further mitigated by adopting novel a-Si:H TFT structures for the driving transistor in the pixel-electrode circuit, such as Corbino a-Si:H TFTs [17]. In Corbino a-Si:H TFT, since the ring-shaped electrode provides a uniform electric-field distribution in the channel and eliminates any local electric-field crowding due to sharp corners present in normal TFT, such new TFT has a better electrical stability for a larger W/L ratio required for driving TFT in comparison to normal TFTs. Therefore, we expect enhanced electrical stability of pixel-electrode circuit with the Corbino driving TFT.

VIII. Conclusion

When a low I_{DATA} is used to express a low gray scale, the conventional current-driven pixel circuit has a problem of slow programming time. On the contrary, when a high I_{DATA} is used to express a high gray scale, the current-mirror pixel circuit has a problem of a high power consumption due to a fixed current-scaling ratio. In the proposed pixel circuit, by using cascaded capacitors connected to the driving TFT, we could produce a nonlinear scaling function that has a high scaling ratio at low current levels and a low scaling ratio at high current levels. Therefore, using such pixel circuit, we expect a reduced power consumption at high current levels and minimized programming time at low current levels, which are ideal characteristics for a high-resolution a-Si:H TFT AM-OLEDs. We also showed experimentally that the proposed pixel-electrode circuit has a better electrical and thermal stability than the conventional current-driven circuit under the same experimental CTS conditions.

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Hojin Lee received the B.S. and M.S. degrees in electrical engineering from Hanyang University, Seoul, Korea, in 1996 and 1998, respectively.

He is currently with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, together with Prof. Jerzy Kanicki in the Organic Molecular Electronics Laboratory. His current researches are in the generation of white-light emission from polymer-blend, active-matrix a-Si:H TFT pixel-circuit design for AM-OLED, and a-Si:H TFT device physics.

Yen-Chung Lin (S'03–M'05) was born in Taiwan, R.O.C., in 1977. He received the B.S. degree in electrical engineering from the National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1999, and the Ph.D. degree in electro-optical engineering from the National Chiao-Tung University, Hsinchu, in 2005.

He is currently working on the liquid-crystal display driver and system on chip integrated circuit development with Sitronix Corporation, Taiwan. His research interest is in the circuit design for display applications and fabrication of thin-film transistors.

Han-Ping D. Shieh (S'79–M'86–SM'91) received the B.S. degree from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1975 and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, in 1987.

He was a Research Staff Member with the IBM T. J. Watson Research Center, Yorktown Heights, NY. He joined the Institute of Electro-Optical Engineering and Microelectronics and the Information Research Center, National Chiao-Tung University, Hsinchu, Taiwan, as a Professor in 1992. Since 1999, he has been a Research Fellow (a joint appointment) with the Center for Applied Sciences and Engineering, Academica Sinica, Taipei. He has published more than 80 journal papers and is the holder of more than 20 patents. His current research interests are display technology, optical microelectromechanical system, nanooptical components, and optical data-storage technologies.

Dr. Shieh is currently the Director of the Society for Information Display. He has served as the Program Chair or a Committee Member and has organized conferences in major data storage, including the International Symposium on Optical Memory and Optical Data Storage (ISOM), Magneto-Optical Recording International Symposium (MORIS), IEEE International Magnetics Conference (Intermag), Optical Data Storage Topical Meeting (ODS), and Asia-Pacific Data Storage Conference (APDSC), and display, including the Society for Information Display (SID), Information Display Research Conference (IDRC), Asian Symposium on Information Display (ASID), Flat Panel Display (FPD) Expo.

Jerzy Kanicki (M'99–A'99–SM'00) received the Ph.D. degree in sciences (D.Sc.) from the Universit Libre de Bruxelles, Brussels, Belgium, in 1982.

He subsequently was with IBM Thomas J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member working on hydrogenated amorphous silicon devices for the photovoltaic and flat-panel display applications. In 1994, he moved from the IBM Research Division to the University of Michigan, Ann Arbor, as a Professor with the Department of Electrical Engineering and Computer Science (EECS). His research interests within the Electrical and Computer Engineering Division, EECS, include organic and molecular electronics, thin-film transistors and circuits, and flat-panel displays technology, including organic light-emitting devices.