New Gate-Bias Voltage-Generating Technique With Threshold-Voltage Compensation for On-Glass Analog Circuits in LTPS Process

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***Abstract*—A new proposed gate-bias voltage-generating technique with threshold-voltage compensation for analog circuits in the low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) is proposed. The new proposed gate-bias voltage-generating circuit with threshold-voltage compensation has been successfully verified in an 8-μm LTPS process. The experimental results have shown that the impact of TFT threshold-voltage variation on the biasing circuit can be reduced from 30% to 5% under a biasing voltage of 3 V. The new proposed gate-bias voltage-generating technique with threshold-voltage compensation enables the analog circuits to be integrated and implemented by the LTPS process on glass substrate for an active matrix LCD panel.**

***Index Terms*—Analog circuit, biasing circuit, low-temperature polycrystalline silicon (LTPS), thin-film transistor (TFT), threshold-voltage compensation, threshold-voltage variation.**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted a great deal of attention in the applications with the integrated on-panel peripheral circuits for active-matrix liquid crystal display (AMLCD) and active-matrix light-emitting diodes (AMOLEDs) [1]–[3]. Recently, LTPS AMLCDs integrated with driving and control circuits on glass substrate have been realized in some portable systems, such as mobile phones, digital cameras, and notebooks. In the near future, the AMLCD fabricated in the LTPS process is promising toward system-on-panel (SoP) or system-on-glass (SoG) applications, especially for achieving a compact, low-cost, and low-power display system [4].

The LCD data driver contains shifter registers, level shifters, digital-to-analog converters (DACs), and output buffers. The biasing circuit is a critical circuit block for analog circuits on the LCD panel to achieve low power consumption, high speed, and high resolution. However, the poly-Si TFT device suffers from significant variation in its threshold voltage, owing to the nature of crystal growth in the LTPS process. The threshold-voltage variation across a 2.7-in panel was about 300 mV [5]. The variation could even be as large as 1 V in some high-performance TFT devices across a large substrate area [6]. The threshold-voltage variations of TFT devices will cause large mismatches on the biasing voltages and currents in analog circuits to result in nonuniformity of performances among analog circuits over the whole panel. The design with threshold-voltage compensation for analog circuits on glass substrate is a very important challenge for SoP applications. The design technique with switches and capacitors under multiphase clock operation were usually used to compensate for the threshold-voltage variation among TFT devices in LTPS AMLCDs [7]–[9]. Some design techniques with switch and capacitor under multiphase clock operation were used to reduce the offset voltage of the analog buffer in the LTPS process [7]. In LTPS technology, the on-panel output buffers with a pair of n-type and p-type TFT devices immune to the mismatch of threshold voltage were also reported [8], [9]. The mismatch of threshold voltage can be compensated by a holding capacitor or the mathematical product of voltage gain. Besides, the threshold-voltage-shift compensation technique was used to compensate for the threshold-voltage variation for differential amplifiers in analog circuits [10]. However, those techniques [7]–[10] only emphasize the impact of threshold-voltage variation on the offset voltage of the analog buffers on glass substrate. The biasing circuit with threshold-voltage compensation for analog circuits in the LTPS process is not yet reported in the literature.

In this paper, a method to reduce the influence of threshold-voltage variation on the gate-bias voltage-generating circuit for analog circuits on glass substrate is proposed. The experimental results have shown that the impact of TFT threshold-voltage variation on the biasing circuit can be reduced from 30% to 5% under a biasing voltage of 3 V. The new proposed biasing technique with threshold-voltage compensation enables the analog circuits to be integrated and implemented in the LTPS process for an AMLCD panel.

II. Impact of Threshold-Voltage Variation on TFT *I–V* Characteristics

In general, the TFT devices on glass substrate are usually designed in the saturation region for analog circuit applications. The small-signal gain and frequency response of analog circuits in the LTPS process are determined by transconductance (g_m) and output resistance (r_o) of TFT devices. The small-signal parameters of transconductance (g_m) and output resistance (r_o) in TFT devices can be expressed, respectively, as

$$g_m = \mu C_{\rm ox}\frac{W}{L}(V_{\rm GS}-V_{\rm TH}) = \frac{2I_D}{(V_{\rm GS}-V_{\rm TH})} \tag{1}$$

$$r_o = \frac{V_A}{I_D} \tag{2}$$

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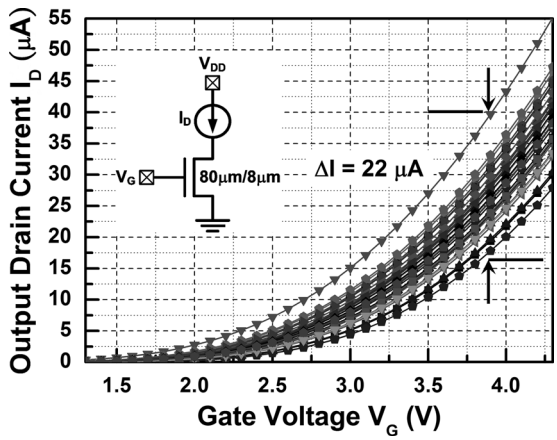

Fig. 1. Simulated waveforms of n-TFT drain current $I_{\rm D}$ with 50% threshold-voltage variation of Gaussian distribution under different gate voltages $V_{\rm G}$ in an 8-μm LTPS process.

where μ is the mobility of carrier, L denotes the effective channel length, W is the effective channel width, $C_{\rm ox}$ is the gate oxide capacitance per unit area, $V_{\rm TH}$ is the threshold voltage of the TFT device, $V_{\rm GS}$ is the gate-to-source voltage of the TFT device, V_A is the Early voltage, and $I_{\rm D}$ is the drain current of the TFT device. Comparing (1) and (2), the drain current $I_{\rm D}$ is the major factor for analog circuits in the LTPS process. Therefore, the performances of analog circuits in the LTPS process are dominated by the drain current of the TFT device. The drain current $I_{\rm D}$ of the TFT device operated in the saturation region can be expressed as

$$I_{\rm D} = \frac{1}{2}\mu C_{\rm OX}\frac{W}{L}(V_{\rm GS} - V_{\rm TH})^2. \tag{3}$$

The channel-length modulation of the TFT device is not included in (3). The threshold voltage $(V_{\rm TH})$ of the TFT device is an important parameter in (3), so the threshold-voltage variation among TFT devices will cause the variation on drain currents of TFT devices to degrade the circuit performances in analog circuits on glass substrate. How to design a stable biasing circuit with threshold-voltage compensation to reduce nonuniformity of performances in analog circuits over the whole panel in the LTPS process is an important design challenge.

The HSPICE with Monte Carlo analysis can be used to simulate and analyze the impact of threshold-voltage variation on drain current of the TFT device. The threshold-voltage variation of the TFT device on glass substrate can be modeled by Gaussian distribution. The simulated waveforms of n-TFT drain current $I_{\rm D}$ with 50% threshold-voltage variation of Gaussian distribution under different gate voltages $V_{\rm G}$ in an 8-μm LTPS process is shown in Fig. 1. The dimension of n-TFT device is 8 μm/8 μm. The gate voltage is biased from 1.3 to 4.3 V. In order to confirm that the n-TFT device is operated in the saturation region, the drain voltage of the n-TFT device is also biased from 1.3 to 4.3 V to keep the gate-to-drain voltage of 0 V. The simulated result shows that the n-TFT device with 50% threshold-voltage variation of Gaussian distribution causes the drain current with a variation as large as 22 μA in the LTPS process. Therefore, the large variations on drain currents of TFT devices will cause large mismatches on the biasing voltages and currents in analog circuits to further result in nonuniformity of performances in analog circuits over the whole panel. For the SoP applications, reducing the impact of threshold-voltage variation on performance among analog circuits in the LTPS process is a very important design challenge.

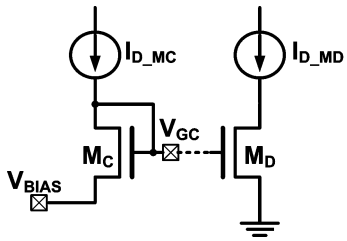

Fig. 2. Concept of the new proposed gate-bias voltage-generating technique with threshold-voltage compensation.

III. New Proposed Gate-Bias Voltage-Generating Technique With Threshold-Voltage Compensation

A. Design Concept

The new proposed gate bias voltage generating technique with threshold-voltage compensation is illustrated in Fig. 2. The biasing current $I_{\rm D\_MC}$ is a small current used to bias the $M_{\rm C}$ device operated in weak inversion region. When the $M_{\rm C}$ device is operated in the weak inversion region, the gate control voltage $V_{\rm GC}$ can be written as

$$V_{\rm GC} \cong V_{\rm BIAS} + V_{\rm TH\_MC} \tag{4}$$

where $V_{\rm TH\_MC}$ is the threshold voltage of $M_{\rm C}$ device, and $V_{\rm BIAS}$ is the applied biasing voltage. The drain current $I_{\rm D\_MD}$ of $M_{\rm D}$ device can be expressed as

$$\begin{aligned} I_{\rm D\_MD} &= \frac{1}{2}\mu C_{\rm OX}\left(\frac{W}{L}\right)_{\rm MD}(V_{\rm GC} - V_{\rm TH\_MD})^2 \\ &= \frac{1}{2}\mu C_{\rm OX}\left(\frac{W}{L}\right)_{\rm MD} \\ &\quad \times (V_{\rm BIAS} + V_{\rm TH\_MC} - V_{\rm TH\_MD})^2 \end{aligned} \tag{5}$$

where $V_{\rm TH\_MD}$ is the threshold voltage of $M_{\rm D}$ device. The $M_{\rm C}$ and $M_{\rm D}$ devices are drawn with the same device dimension. The threshold-voltage difference between $M_{\rm C}$ and $M_{\rm D}$ devices can be reduced as small as possible by symmetrical and compact layout in an adjacent location. Therefore, (5) can be further rewritten as

$$I_{\rm D\_MD} \cong \frac{1}{2}\mu C_{\rm OX}\left(\frac{W}{L}\right)_{\rm MD}(V_{\rm BIAS})^2. \tag{6}$$

The drain current $I_{\rm D\_MD}$ of $M_{\rm D}$ device can become independent of the threshold voltage and dominated by the $V_{\rm BIAS}$ voltage. The new proposed gate-bias voltage-generating technique with threshold-voltage compensation does not need any extra clock signal and capacitor to reduce the impact of

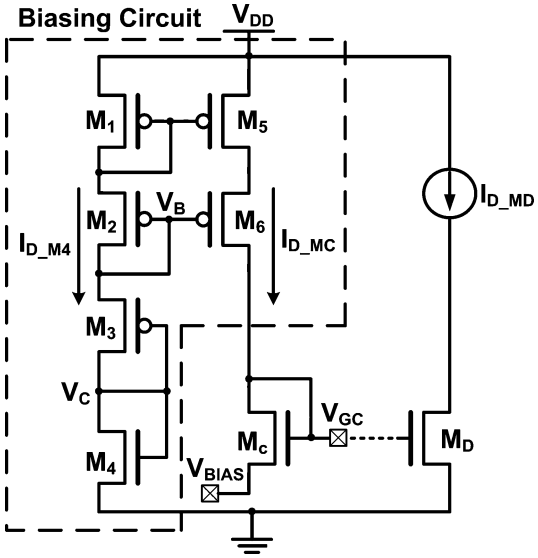

Fig. 3. Complete circuit of the proposed gate-bias voltage-generating circuit with threshold-voltage compensation for analog circuits in LTPS technology.

threshold-voltage variation on the biasing circuit for analog circuits in LTPS processes.

B. Circuit Implementation

The complete circuit of the proposed gate-bias voltage-generating technique with threshold-voltage compensation for analog circuit applications in LTPS technology is shown in Fig. 3. The new proposed gate-bias voltage-generating circuit with threshold-voltage compensation is formed with M_1, M_2, M_3, M_4, M_5, and M_6 devices. The M_1, M_2, M_5, and M_6 devices form the current mirror. In order to reduce the power consumption and chip area of the new proposed gate-bias voltage-generating circuit, the M_3 and M_4 devices are used to realize the referenced current source. The M_3 and M_4 devices are operated in the saturation region to generate a biasing current through the current mirror of M_1, M_2, M_5, and M_6 devices to bias $M_{\rm C}$ device operated in the weak inversion region. The voltage $V_{\rm C}$ can be expressed as

$$V_C = \frac{r\left(V_B - |V_{\rm TH\_M3}|\right) + V_{\rm TH\_M4}}{1+r} \tag{7}$$

$$r = \sqrt{\frac{\mu_p \left(\frac{W}{L}\right)_{\rm M3}}{\mu_n \left(\frac{W}{L}\right)_{\rm M4}}} \tag{8}$$

where $V_{\rm B}$ is the voltage at the source node of M_3 device in proposed gate-bias generating circuit. The biasing current $I_{\rm D\_M4}$ and $I_{\rm D\_MC}$ can be written, respectively, as

$$I_{\rm D\_M4} = \frac{1}{2}\mu C_{\rm OX}\left(\frac{W}{L}\right)_{\rm M4}(V_C - V_{\rm TH\_M4})^2 \tag{9}$$

$$I_{\rm D\_MC} = \left(\frac{1}{K}\right) I_{\rm D\_M1} \tag{10}$$

where the K is the dimension ratio of M_5 and M_1 in the current mirror. The K factor is especially designed much larger than one to reduce the impact of biasing current ($I_{\rm D\_M4}$) variation on gate control voltage ($V_{\rm GC}$) of the new proposed gate-bias voltage-generating circuit.

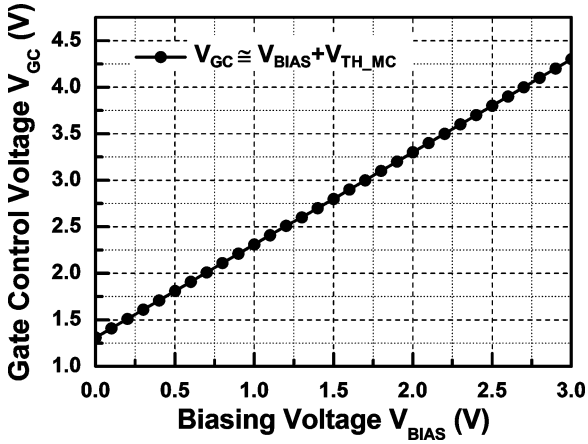

Fig. 4. Simulated gate control voltage $V_{\rm GC}$ of the proposed gate-bias voltage-generating circuit with threshold-voltage compensation under different biasing voltages $V_{\rm BIAS}$.

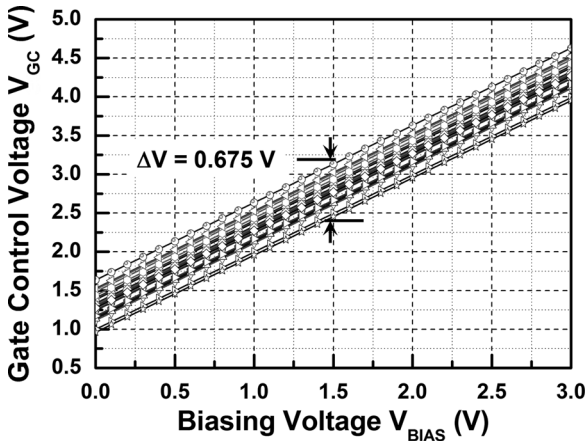

Fig. 5. Simulated gate control current $V_{\rm GC}$ of the proposed gate-bias voltage-generating circuit with threshold-voltage compensation under the different biasing voltages $V_{\rm BIAS}$ with the 50% threshold voltage variation (Gaussian distribution) on n-TFT and p-TFT devices.

The simulated gate control voltage $V_{\rm GC}$ of the new proposed gate bias voltage generating circuit with threshold-voltage compensation under different biasing voltages $V_{\rm BIAS}$ is shown in Fig. 4. The typical threshold voltage of an n-TFT device in an 8-μm LTPS process is approximately 1.3 V. The $V_{\rm BIAS}$ voltage is biased from 0 to 3 V. The gate control voltage $V_{\rm GC}$ is changed from 1.3 to 4.3 V. The gate control voltage $V_{\rm GC}$ of the new proposed gate-bias voltage-generating circuit with threshold-voltage compensation is approximately $V_{\rm BIAS} + V_{\rm TH\_MC}$. The HSPICE with Monte Carlo Analysis is used to verify the function of the new proposed gate-bias voltage-generating circuit with threshold-voltage compensation in LTPS technology. The simulated gate control current $V_{\rm GC}$ of the new proposed gate-bias voltage-generating circuit with threshold-voltage compensation under the different biasing voltages $V_{\rm BIAS}$ with the 50% threshold voltage variation (Gaussian distribution) of n-TFT and p-TFT devices is shown in Fig. 5. The variation on gate control voltage $V_{\rm GC}$, which can be used to compensate the threshold-voltage variation of TFT

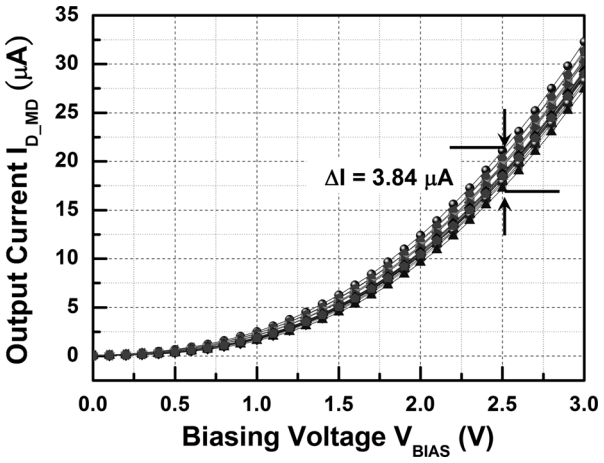

Fig. 6. Simulated drain current $I_{\mathrm{D\_MD}}$ of the proposed gate-bias voltage-generating circuit with threshold-voltage compensation under different biasing voltages V_{BIAS} with the 50% threshold voltage variation (Gaussian distribution) of n-TFT and p-TFT devices.

device in the LTPS process, is 0.675 V. The simulated drain current $I_{\mathrm{D\_MD}}$ of the new proposed gate-bias voltage-generating circuit with threshold-voltage compensation under different biasing voltages V_{BIAS} with the 50% threshold-voltage variation (Gaussian distribution) of n-TFT and p-TFT devices is shown in Fig. 6. The device dimension of M_{D} device is 80 μm/8 μm. The gate-to-drain voltage of M_{D} device is set to zero voltage to be operated in the saturation region. The simulated results show that the 50% threshold-voltage variation with Gaussian distribution of n-TFT and p-TFT devices causes only a variation of 3.84 μA on the drain current $I_{\mathrm{D\_MD}}$ in the new proposed gate-bias voltage-generating circuit with threshold-voltage compensation. Comparing the simulated results of Figs. 1 and 6, the new proposed gate-bias generating circuit with threshold-voltage compensation can effectively reduce the impact of threshold-voltage variation on the biasing circuit in the LTPS process.

IV. Experimental Results

The new proposed gate-bias generating circuit with threshold-voltage compensation has been fabricated in an 8-μm LTPS technology. Fig. 7 shows the chip photograph of the new proposed gate-bias generating technique with threshold-voltage compensation. The test chip size of the new proposed gate-bias generating circuit with threshold-voltage compensation circuit is 517 $\times$ 389 μm^2 in 8-μm LTPS technology. The averaged power consumption of the proposed gate-bias generating circuit with threshold-voltage compensation is only 47 μW under the supply voltage of 10 V. In this study, the definitions of mean value and variation (%) of currents in these measured results are adopted as

$$\text{Mean Value} = \frac{I_{\mathrm{D1}} + I_{\mathrm{D2}} + I_{\mathrm{D3}} + I_{\mathrm{D4}}}{4} \tag{11}$$

$$\text{Variation}(\%) = \frac{\text{Mean Value} - I_{\mathrm{D\_\#}}}{\text{Mean Value}} \times 100\% \tag{12}$$

where I_{D1}, I_{D2}, I_{D3}, and I_{D4} are drain currents of sample1, sample2, sample3, and sample4 of four LPTS n-TFT devices

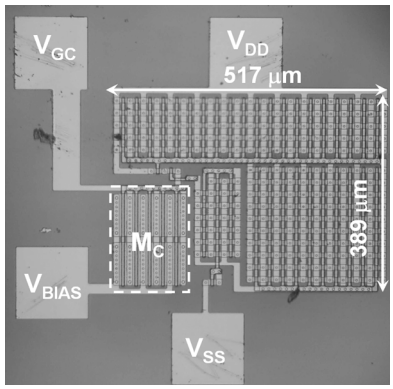

Fig. 7. Chip photograph of the proposed gate-bias generating technique with threshold-voltage compensation fabricated in an 8-μm LTPS process.

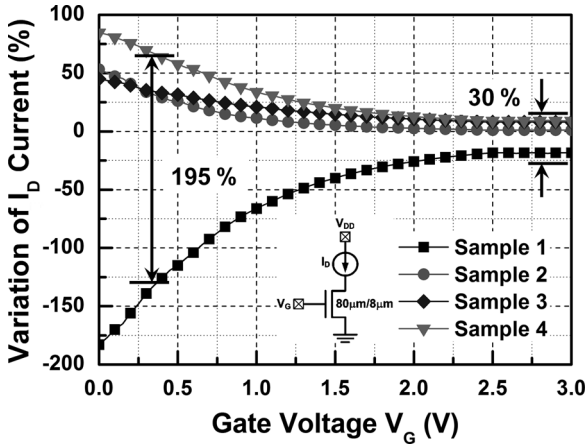

Fig. 8. Measured dependence of variation (%) on the gate voltage V_{G} among four LTPS n-TFT devices in different panel locations.

in different panel locations, respectively, and the # is a sample number from 1 to 4. The power supply voltage V_{DD} is set to 10 V. Fig. 8 shows the measured dependence of variation (%) on the gate voltage V_{G} under four LTPS n-TFT devices in different panel locations. The device dimensions of four n-TFT devices are kept at 80 μm/8 μm in an 8-μm LTPS process. The gate voltages of these samples are biased from 1.3 to 4.3 V. The gate-to-drain voltage of the n-TFT device is set to 0 V to keep the n-TFT device operating in the saturation region. Because the gate-control voltage V_{GC} of the new proposed gate-bias generating circuit is $V_{\mathrm{BIAS}}+V_{\mathrm{TH}}$, the gate voltage from 1.3 to 4.3 V is normalized from 0 to 3 V. The variation (%) among four LPTS n-TFT devices in different panel locations is decreased from 195% to 30%, when the gate voltage is increased from 0 to 3 V. The measured results have confirmed that the variation (%) of four LPTS n-TFT devices in different panel locations under low gate voltage is large, but that under high gate voltage is low.

The measured dependence of variation (%) on the biasing voltage V_{BIAS} among four LTPS test circuits of the new proposed gate-bias generating circuit with threshold-voltage compensation in different panel locations is shown in Fig. 9. The variation (%) among four LPTS test circuits in different panel locations is decreased from 73% to 5%, when the gate voltage is increased from 0 to 3 V. Comparing the measured results between Figs. 8 and 9, the new proposed gate-bias generating

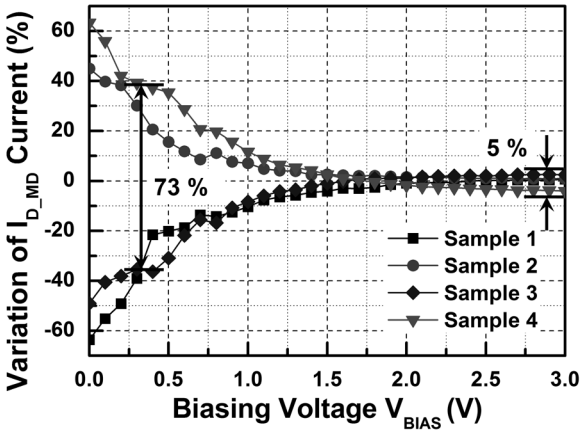

Fig. 9. Measured dependence of variation (%) on the biasing voltage $V_{\rm BIAS}$ among four LTPS test circuits of the new proposed gate-bias generating technique with threshold-voltage compensation in different panel locations.

technique with threshold-voltage compensation can effectively reduce the impact of threshold-voltage variation on the biasing current or biasing voltage for analog circuits in SoP or SoG applications.

V. Discussion

When the referenced current source $I_{\rm D\_M4}$ is realized with an ideal referenced current source, the simulated results show that variation of $I_{\rm D\_MD}$ is only 0.27 μA under 50% threshold-voltage variation (Gaussian distribution) of n-TFT and p-TFT devices. In order to achieve the low power consumption and small chip area, the referenced current source $I_{\rm D\_M4}$ in the proposed gate-bias voltage-generating circuit with threshold-voltage compensation is realized by M_3 and M_4 devices. Because the voltage $V_{\rm C}$ is dependent on threshold voltages of n-TFT and p-TFT devices, the threshold-voltage variation will cause some variations on the voltage $V_{\rm C}$ and biasing current ($I_{\rm D\_M4}$ and $I_{\rm D\_MC}$) to degrade the performances of the proposed gate-bias voltage-generating circuit with threshold-voltage compensation. The variation of $I_{\rm D\_MD}$ is finally increased from 0.27 to 3.84 μA under 50% threshold voltage variation (Gaussian distribution) of n-TFT and p-TFT devices. In order to reduce the impact of referenced current $I_{\rm D\_M4}$ variation on circuit performance, the M_3 and M_4 referenced current source can be further replaced by the modified n-TFT threshold-voltage referenced current source [11]. The complete circuit of the proposed gate-bias voltage-generating circuit with n-TFT threshold-voltage referenced current source for analog circuit applications in LTPS technology is shown in Fig. 10. When the referenced current source $I_{\rm D\_M4}$ is realized with modified n-TFT threshold-voltage referenced current source, the simulated results show that the variation of $I_{\rm D\_MD}$ is only 0.36 μA under 50% threshold-voltage variation (Gaussian distribution) of n-TFT and p-TFT devices, as shown in Fig. 11. Because the threshold voltages of n-TFT devices have the same variation trend in the local panel location, the biasing current $I_{\rm D\_MD}$ with modified n-TFT threshold-voltage referenced current source can further reduce the variation on performance of the proposed circuit.

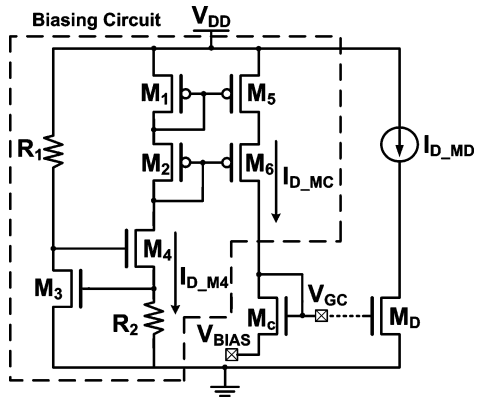

Fig. 10. Complete circuit of the proposed gate-bias voltage-generating circuit with modified n-TFT threshold-voltage referenced current source for analog circuits in LTPS technology.

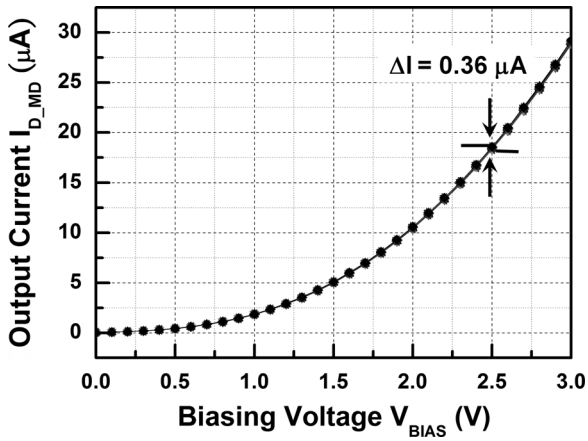

Fig. 11. Simulated drain current $I_{\rm D\_MD}$ of the proposed gate-bias voltage-generating circuit with modified n-TFT threshold-voltage referenced current source under different biasing voltages $V_{\rm BIAS}$ with the 50% threshold voltage variation (Gaussian distribution) of n-TFT and p-TFT devices.

VI. Conclusion

A new gate-bias generating technique with threshold-voltage compensation has been presented to reduce the impact of threshold-voltage variation on analog circuit performance in LTPS technology. The new proposed gate-bias generating circuit with threshold-voltage compensation has been successfully verified in an 8-μm LTPS process. The measured results have confirmed that the impact of threshold-voltage variation on drain current of the n-TFT device can be reduced from 30% to 5% under a biasing voltage of 3 V. The new proposed gate-bias generating technique with threshold-voltage compensation can be applied to realize analog circuits in the LTPS process for SoP or SoG applications.

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