A Novel Nanowire Channel Poly-Si TFT Functioning as Transistor and Nonvolatile SONOS Memory

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***Abstract*—In this letter, a polycrystalline silicon thin–film transistor consisting of silicon–oxide–nitride–oxide–silicon (SONOS) stack gate dielectric and nanowire (NW) channels was investigated for the applications of transistor and nonvolatile memory. The proposed device, which is named as NW SONOS-TFT, has superior electrical characteristics of transistor, including a higher drain current, a smaller threshold voltage ($V_{\rm th}$), and a steeper subthreshold slope. Moreover, the NW SONOS-TFT also can exhibit high program/erase efficiency under adequate bias operation. The duality of both transistor and memory device for the NW SONOS-TFT can be attributed to the trigate structure and channel corner effect.**

***Index Terms*—Nanowire (NW), nonvolatile memory, polysilicon (poly-Si), silicon–oxide–nitride–oxide–silicon (SONOS), thin-film transistor (TFT).**

I. Introduction

POLYSILICON thin-film transistors (poly-Si TFTs) have attracted much attention for use in active-matrix liquid-crystal-displays since they can be integrated with peripheral driving circuits because of their high field effect mobility and driving current [1]. Systems-on-panels (SOP), which are integrated with such functional devices on an LCD panel as a controller [2] and memory [3], have been proposed in the development of display technology development to make displays more compact and reliable and to reduce their cost. Since SOP technology is primarily used for portable electronics, low-power consumption is basically required to ensure long battery life. It is well known that the nonvolatile memory is widely utilized for data storage in portable electronics systems due to its properties of low-power consumption and nonvolatility. Unlike the conventional nonvolatile floating gate memory, silicon–oxide–nitride–oxide–silicon (SONOS)-type memory has become a promising candidate for SOP application because it is fully compatible with poly-Si TFTs process. However, SONOS-type nonvolatile memory still raises several issues concerning performance and reliability, such as insufficient programming/erasing (P/E) efficiency, poor endurance, and short retention time [4]. Recently, various approaches have been proposed for the improvement of the performance and reliability of SONOS using dielectric engineering [5], [6]. In addition, SONOS-type poly-Si TFT, which is fabricated by the sequential lateral solidified (SLS) method, has also been reported to improve the P/E efficiency by field-enhanced tunneling in Si protrusion regions [7]. However, the uniformity of the Si protrusions recrystallized by SLS is still a problem.

Based on our previous study [8], the poly-Si TFT with nanowire (NW) channels can provide good gate control due to its trigate structure. Besides, the nonvolatile nanocrystal memory with a narrow channel width structure has been demonstrated to improve the P/E efficiency [9]. Thus, in this letter, the poly-Si TFT combined with nonvolatile SONOS memory and NW channels, which is named as NW SONOS-TFT, is proposed to obtain superior electrical performance for transistor and higher P/E efficiency for memory device.

II. Experiment

In this letter, the SONOS-TFT with ten strips of 65-nm NW channel was proposed. The standard device with a single channel structure with $W = 1$ μm (STD) was also fabricated for comparison. The detailed fabrication procedures are described as follows. At first, undoped amorphous silicon (a-Si) with thickness of 50 nm was deposited on oxidized silicon wafers by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then, the deposited a-Si layer was recrystallized by solid-phase crystallization at 600 °C for 24 h in a N_2 ambient. After the active region patterning by electron beam lithography, the 25-nm-thick ONO multilayer gate dielectric of the bottom oxide (5 nm) / silicon nitride (10 nm) / top oxide (10 nm) was deposited by LPCVD. Subsequently, a 150-nm-thick *in situ* n^+ doped poly-Si layer was deposited and transferred to a gate electrode. After source/drain (S/D) formation by self-aligned phosphorous implantation, a 200-nm oxide passivation layer was deposited, and contact holes were patterned. Finally, Al

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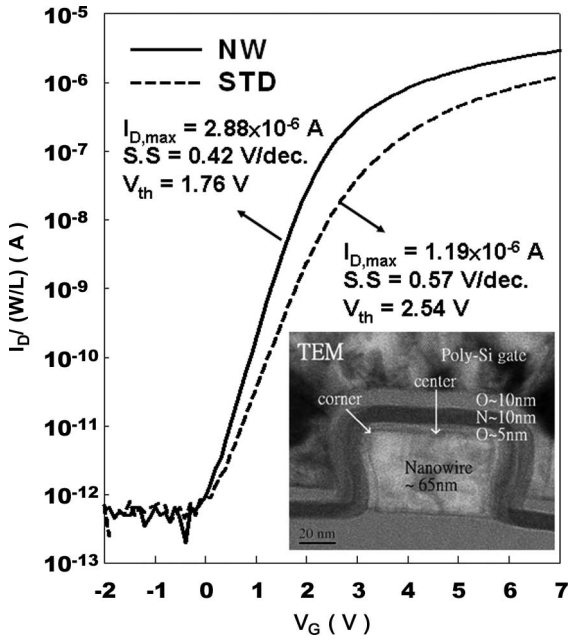

Fig. 1. Comparison of typical I_D–V_G characteristics of the standard and the NW SONOS-TFTs. The inset exhibits the TEM of a single NW channel of NW SONOS-TFT.

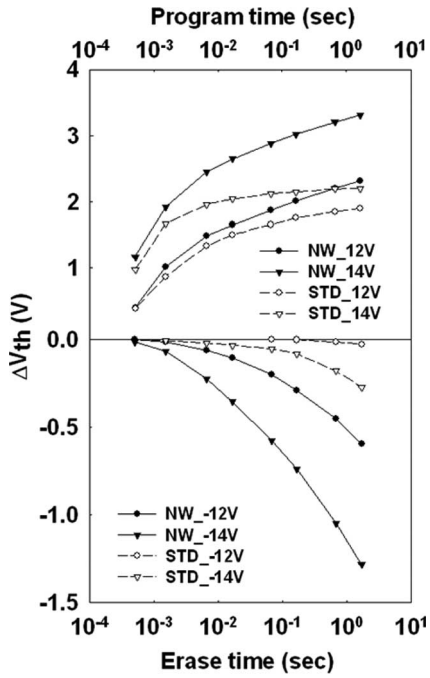

Fig. 2. Programming and erasing characteristics of memory devices for NW and standard structures.

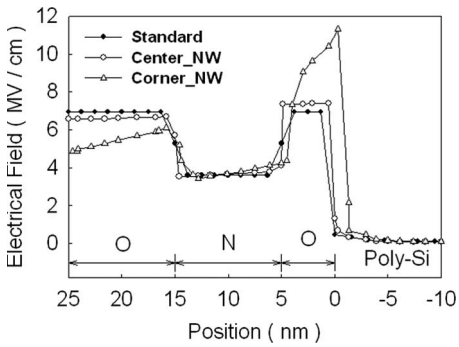

Fig. 3. Simulation results of the electrical fields with a gate bias of 14 V for the standard device and NW device at center and corner regions.

metallization was performed, and the devices were sintered at 400 °C in nitrogen ambient for 30 min.

III. Results and Discussion

Fig. 1 presents the typical normalized I_D–V_G curves of the standard and the proposed NW SONOS-TFTs. The inset shows the transmission electron microscopy (TEM) photography of a single NW channel. It is clearly seen that the NW channel is surrounded by the control gate to form the trigate structure, and the physical channel width of NW SONOS-TFT is confirmed to be 65 nm. The threshold voltage in this letter is determined at $I_D/(W/L) = 10$ nA for $V_D = 0.1$ V. The transfer characteristic reveals that the NW device outperforms the standard device, with higher drain current, smaller threshold voltage $(V_{\rm th})$, and steeper subthreshold swing. Since the effective channel width is increased, and the control of the channel region is enhanced by the trigate structure, the drain current and $V_{\rm th}$ can be improved in NW SONOS-TFT. Furthermore, the current at the corner region turns on earlier than that at the surface of the channel because of the larger electrical field [10], and the additional corner current can increase the drain current as the number of corners increases. Hence, the enhancement in electrical performance of the NW SONOS-TFT can be attributed mainly to the good gate control by the trigate structure and the corner effect.

In addition, the SONOS-TFTs can also be used as nonvolatile memory devices at adequate gate voltage operation. However, the reset state $V_{\rm th}$ of memory differs from the $V_{\rm th}$ for the transistor due to gate injection into the ONO layer during an erasing operation. The reset state $V_{\rm th}$ is determined by the charge balance between the gate injection and the detrapping out of the ONO layer. Thus, the SONOS-TFT is not interchangeable for the two modes at the same time. In this letter, due to the fact that tunneling current is mainly dominated by Fowler–Nordheim (FN) tunneling, as the thickness of tunneling oxide is thicker than 5 nm [11], the SONOS-TFTs are programmed and erased by FN tunneling mechanism. Fig. 2 shows the programming and erasing characteristics of the NW and standard devices. Clearly, the memory device with multiple NW channels has greater P/E efficiency and memory window shift. For the standard device, the results also indicate that the memory windows are saturated as the programming time increases and the threshold voltage shift is very small even at a gate voltage of -14 V.

The distribution of an electrical field across the stacked gate dielectric was numerically simulated at a gate bias of 14 V using an ISE-TCAD simulator for the standard and NW devices to examine the improvement in the memory characteristics. As shown in Fig. 3, at the corners of the NW channel, the electrical field across the tunneling oxide is much larger than that across the blocking oxide. The P/E activity is thus facilitated between the tunneling oxide and channel rather than between the blocking oxide and the gate. Comparatively, electrical fields

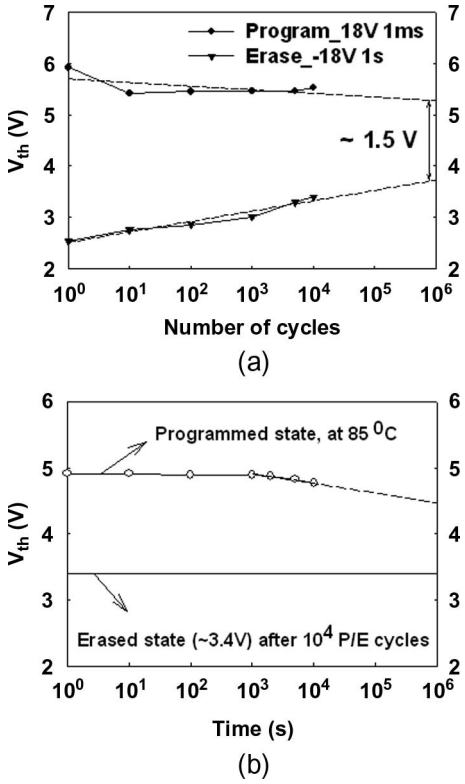

Fig. 4. (a) Endurance and (b) retention characteristic of the NW SONOS-TFT. Memory window remains 1.5 V after 10^4 P/E cycles and 1 V after 10^6 s at 85 °C.

are uniformly across all oxide layers for the standard TFT device. This will lead the threshold voltage shift of the standard device to be easily saturated during the programming operation as soon as the equilibrium of electron flows is achieved through the paths from channel to the storage layer and from the storage layer to gate electrode. The injection of electrons from the gate to the storage layer during the erasing operation causes inefficient erasing and a lower threshold voltage shift in the standard device. Also, the inefficient erasing activity similarly appears at the center region of the NW channel. Therefore, the pronounced enhancement of P/E efficiency for the NW device is attributed to the large number of corners, where large electrical field is induced by the corner effect.

Fig. 4(a) shows the endurance characteristic of the NW device with a programming bias of 18 V for 1 ms and an erasing bias of −18 V for 1 s. Indeed, the memory window is degraded by interface-trap generation and tunneling oxide degradation as the number of P/E cycles increases. However, the NW device can still maintain a 1.5-V memory window after 10^6 P/E cycles. The memory window is sufficiently large for the practical usability. Fig. 4(b) presents the retention characteristic of the NW device. The devices are programmed after 10^4 P/E cycles and then measured at 85 °C. The result indicates that the memory window is still kept about 1 V after 10^6 s at 85 °C.

IV. Conclusion

This letter demonstrates the feasibility of a novel poly-Si TFT that functions as both transistor and nonvolatile SONOS memory. The experimental results show that the NW SONOS-TFT has the better electrical characteristics because of its trigate structure and additional corner current that is induced by corner effect. In addition, the proposed device exhibits memory characteristics as an adequate gate bias is applied. The simulation of electrical field results verified that the enhancement in P/E efficiency of the NW SONOS-TFT is attributable mostly to the large number of corners and the corner effect. In addition, good endurance and retention are also obtained in this device. The fabrication of SONOS-TFTs with NW channels is quite easy and involves no additional processes. Such a SONOS-TFT is thereby very promising for use in the future SOP display applications.

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