Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed nMOSFETs

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***Abstract*—We measure the conduction-band electron direct tunneling current through the 1.27-nm gate oxide of nMOSFETs transistors that undergo longitudinal stress via a layout technique. With known process parameters and published deformation potential constants as input, fitting of the measured direct tunneling current versus gate voltage leads to the channel stress of around 0, −100, and −300 MPa for a gate-to-trench isolation spacing of 2.4, 0.495, and 0.21 μm, respectively. To examine the accuracy of the method, a link with the mobility and threshold voltage measurements on the same device is conducted. The resulting piezoresistance coefficient and band offset are in good agreement with the literature values. The layout technique used is validated as well.**

***Index Terms*—Mechanical stress, MOSFET, piezoresistance, shallow trench isolation (STI), strain, tunneling.**

I. Introduction

IT IS WELL recognized that the mechanical stress in MOSFETs can significantly affect many electrical properties such as mobility [1]–[3], hot carrier immunity [4], threshold voltage [5], and gate direct tunneling current [6]–[8]. Thus, the ability to quantitatively determine the magnitude of the underlying mechanical stress as well as its status (compressive or tensile) is essential. Three fundamentally different methods have been introduced in this direction: 1) wafer bending jig [9]; 2) sophisticated stress simulation [10]; and 3) Raman spectroscopy [11]. Obviously, the *electrical* approach to mechanical stress was lacking to date. However, it is noteworthy that the gate direct tunneling current has been well studied under externally applied mechanical stress [6]–[8]. Particularly in [8], the deformation potential constants [12]–[14] have been experimentally determined and have been found to be consistent with theoretical works [15]. Therefore, with known deformation potential constants, it is plausible to measure mechanical stress by means of the gate direct tunneling current.

In this letter, we show how to transform the gate direct tunneling current in stressed devices into the value of stress achieved without adjusting any parameter. Confirmative evidence is presented in terms of piezoresistance coefficient and band offset, which are both electrically created on the *same* device.

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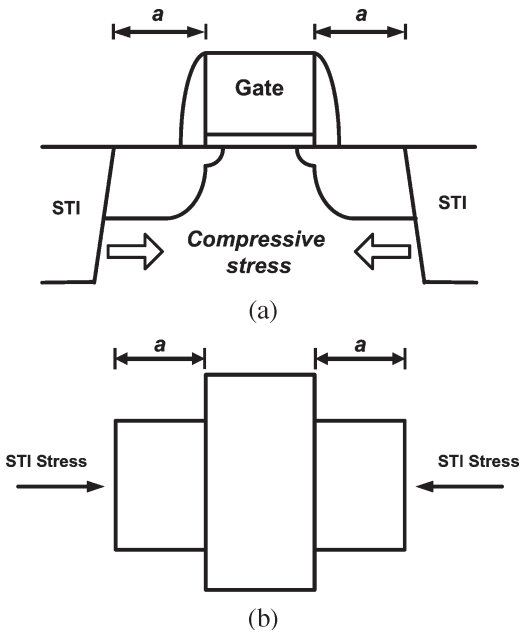

Fig. 1. (a) Schematic cross section and (b) topside view of the device under study. The gate edge to STI sidewall, i.e., a, is highlighted. The stress condition is compressive due to the lower thermal expansion rate of STI oxide compared to silicon.

II. Experiment

The n^+ poly-silicon gate nMOSFETs were fabricated in a state-of-the-art manufacturing process. Three key process parameters were obtained by capacitance–voltage (C–V) fitting: n^+ poly-silicon doping concentration $= 1 \times 10^{20}$ cm^{-3}, gate oxide thickness $= 1.27$ nm, and substrate doping concentration $= 4 \times 10^{17}$ cm^{-3}. In this process, shallow trench isolation (STI)-induced compressive stress was applied. The gate length along the $\langle 110 \rangle$ direction was 1 μm, whereas the gate width was 10 μm, which is large enough that the transverse strain is relatively insignificant. The layout technique was utilized in terms of gate edge to STI sidewall spacing, which is designated as a, with three values of 2.4, 0.495, and 0.21 μm. A decrease in a means increased magnitude of longitudinal stress. The schematic cross section and topside view of the test device are depicted in Fig. 1.

The gate direct tunneling current was measured in inversion conditions with the source, drain, and substrate all tied to ground. The simultaneously measured valence-band electron tunneling counterpart or equivalently the substrate hole current was found to be unchanged regardless of stress. This indicates that the gate oxide thickness under study remains constant. Also

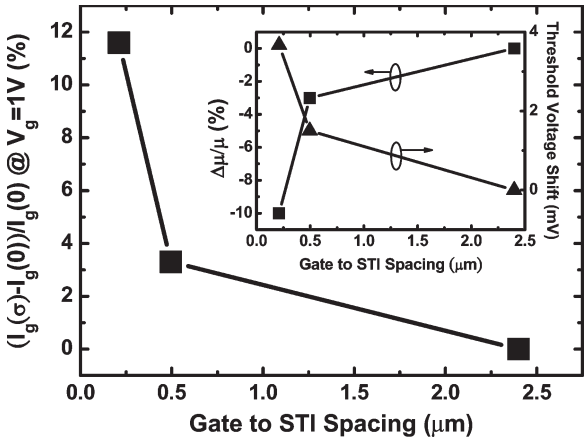

Fig. 2. Relative change of the gate direct tunneling current at $V_g = 1$ V versus gate-to-STI spacing. The inset shows the mobility variations and the threshold voltage shift both versus the gate-to-STI spacing.

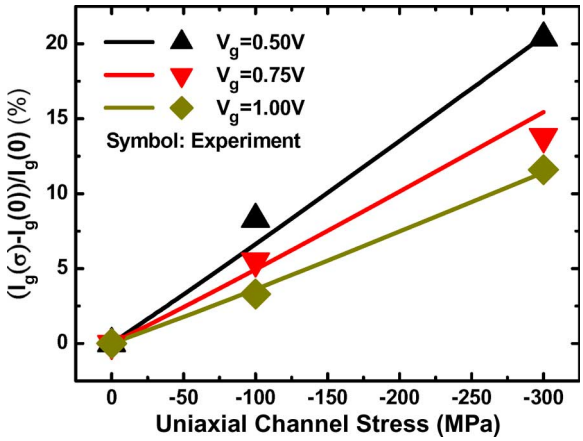

Fig. 3. Relative change of the gate direct tunneling current versus extracted uniaxial compressive channel stress for $V_g = 0.5$, 0.75, and 1 V. The symbols are experimental data. The fitting line is drawn only for accommodating the trend.

characterized were the threshold voltage and mobility on the same device at $V_d = 25$ mV. The change of the conduction-band electron direct tunneling current at $V_g = 1$ V, the mobility at $V_g = 0.5$ V, and the threshold voltage shift, all with respect to $a = 2.4$ μm, are plotted in Fig. 2 versus gate-to-STI spacing. It can be seen that a decrease in the gate-to-STI spacing can produce an increase in both gate current and threshold voltage while degrading mobility.

III. Stress Extraction

Existing direct tunneling models [16], [17] on the basis of the triangular potential approximation [18] in the channel, which takes into account the poly-silicon depletion, can be readily applied with some slight modifications such as incorporating stress dependencies of the subbands. The electrons in inversion primarily populate the two lowest subbands [8]: one of the twofold valley Δ_2 and one of the fourfold valley Δ_4. The corresponding stress dependencies are well defined in the literature [8], [12]–[14]

$$E_{\Delta 2}(\sigma) = \left(\frac{9hqE_{\text{eff},\Delta 2}}{16\sqrt{2m^*_{\Delta 2}}}\right)^{\frac{2}{3}} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11}+2S_{12})\sigma + \left(\frac{\Xi_u}{3}\right)(S_{12}-S_{11})\sigma \quad (1)$$

$$E_{\Delta 4}(\sigma) = \left(\frac{9hqE_{\text{eff},\Delta 4}}{16\sqrt{2m^*_{\Delta 4}}}\right)^{\frac{2}{3}} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11}+2S_{12})\sigma - \left(\frac{\Xi_u}{6}\right)(S_{12}-S_{11})\sigma \quad (2)$$

where the quantization effective masses are $m^*_{\Delta 2} = 0.92\ m_0$ and $m^*_{\Delta 4} = 0.19\ m_0$, and the elastic compliance constants are $S_{11} = 7.68 \times 10^{-12}$ m^2/N and $S_{12} = -2.14 \times 10^{-12}$ m^2/N. The hydrostatic and shear deformation potential constants $\Xi_d = 1.13$ eV and $\Xi_u = 9.16$ eV [5], which are close to those in [8], were cited here. One of the expressions for the effective electric field E_{eff} can be found elsewhere [8]. With the aforementioned process parameters as input, the two lowest subband levels with respect to the Fermi level E_f can be determined. The stress dependencies of the lowest subbands under different gate voltages were found to be consistent with those in earlier works [8]. The inversion-layer carrier density per unit area can further be calculated by $N_i = (k_BT/\pi\hbar^2)g_i m_{di} \ln(1 + \exp((E_f - E_i)/k_BT))$ [16]–[18], where the subscript i denotes Δ_2 or Δ_4, k_BT is the thermal energy, g_i is the degeneracy of the valley, and m_{di} is the density of state effective mass. It is then a straightforward task to calculate the Wentzel–Kramers–Brillouin tunneling probability, taking into account the corrections for reflections from the potential discontinuities [19]. Here, the electron effective mass in the oxide for the parabolic-type dispersion relationship was used with $m_{\text{ox}} \sim 0.50\ m_0$, which is equivalent to $m_{\text{ox}} = 0.61\ m_0$ for the tunneling electrons in the oxide using the Franz-type dispersion relationship [20]. The SiO_2/Si interface barrier height in the absence of stress is 3.15 eV. Consequently, without adjusting any parameter, the conduction-band electron direct tunneling current density can be calculated as a function of stress σ [8] as

$$I_g(\sigma) = \frac{qN_{\Delta 2}(\sigma)}{\tau_{\Delta 2}(\sigma)} + \frac{qN_{\Delta 4}(\sigma)}{\tau_{\Delta 4}(\sigma)}. \quad (3)$$

The tunneling lifetime in (3) can be related to the transmission probability T as $\tau_{\Delta 2}(\sigma) = \pi\hbar/(T_{\Delta 2}(\sigma)E_{\Delta 2}(\sigma))$ and $\tau_{\Delta 4}(\sigma) = \pi\hbar/(T_{\Delta 4}(\sigma)E_{\Delta 4}(\sigma))$.

With the above approach, we found that the uniaxial channel stress of around 0, -100, and -300 MPa for a gate-to-STI spacing of 2.4, 0.495, and 0.21 μm, respectively, can reproduce gate direct tunneling current versus gate voltage characteristics. The corresponding gate current change is plotted in Fig. 3 versus the extracted channel stress with gate voltage as a parameter. It can be seen that the magnitude of the gate current change increases linearly with the stress, which is consistent with those published elsewhere [8]. Again, in agreement with the citation [8], the slope of the straight line in Fig. 3 increases with decreasing gate voltage. This trend clearly points out that the accuracy of the proposed method can be enhanced by lowering gate voltages.

IV. Confirmative Evidence

The measured mobility change percentage versus extracted stress is shown in Fig. 4. The straight line through the data

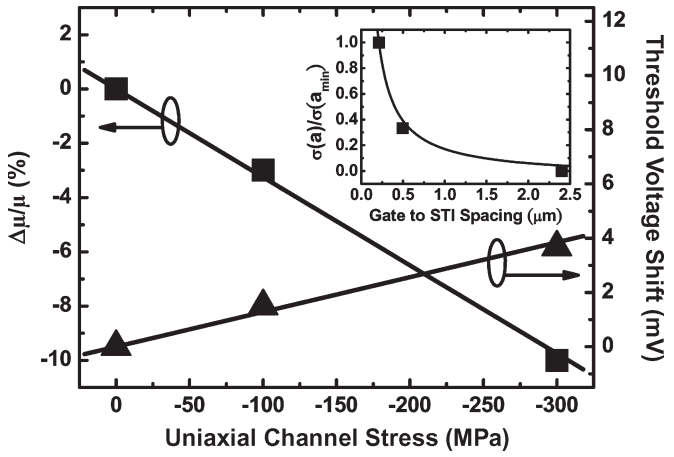

Fig. 4. Measured mobility change and threshold voltage shift versus extracted stress. The inset shows the extracted stress divided by that of the minimum a versus the gate-to-STI spacing along with a fitting curve from (4).

points yields the slope or piezoresistance coefficient of 32.5×10^{-12} dyn^{-1} cm^2, which is close to that (31.5×10^{-12} dyn^{-1} cm^2) in the literature [21]. Also plotted is the threshold voltage shift $\Delta V_{\rm th}$, which produces a straight line of its own. This line can be related to the body-effect coefficient m and the band offset ΔE_g [5]: $q\Delta V_{\rm th}(\sigma) \approx (m-1)\Delta E_g(\sigma)$. The band offset term can further be linked to the strain ε [5]: $\Delta E_g = -6.19\varepsilon = -3.66 \times 10^{-11}\sigma$ eV. The slope of the line in Fig. 4 furnishes $m = 1.35$, which exactly falls within the cited range of 1.3–1.4 [5].

To testify to the layout technique mentioned above, we quote the existing relationship between the effective channel stress and the gate-to-STI spacing, which was derived from the stress simulation [10]

$$\sigma(a) = \sigma(a_{\rm min})\left(1 + V_{m\sigma}\frac{a - a_{\rm min}}{a}\right) \tag{4}$$

where $a_{\rm min}$ represents a minimum gate-to-STI spacing, and $V_{m\sigma}$ is the maximum $\sigma(a)$ variations (i.e., when $a \to \infty$) with respect to $\sigma(a_{\rm min})$. The extracted stress can be adequately described by (4) with $V_{m\sigma} = -1.05$, as inserted in Fig. 4. Indeed, the projected stress for $a = 2.4$ μm, i.e., the reference point mentioned above, approaches zero. Therefore, the layout technique holds true in this letter.

Finally, the electrical method accompanied with the layout technique was also applied to other devices (with a sample size of 10) on the same wafer. The corresponding stress-induced variations in gate direct tunneling current were found to be comparable with those in Fig. 3.

V. Conclusion

With known process parameters and published deformation potential constants as input, fitting of the gate direct tunneling current versus gate voltage data has led to the value of the underlying channel stress. A link with the mobility and threshold voltage measurements on the same device has been conducted. The resulting piezoresistance coefficient and band offset have been in good agreement with the literature values. The layout technique has also been validated.

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