A Monolithic Current-Mode Buck Converter With Advanced Control and Protection Circuits

Feng-Fei Ma, Wei-Zen Chen, and Jiin-Chuan Wu

***Abstract*—A monolithic current-mode pulse width modulation (PWM) step-down dc–dc converter with 96.7% peak efficiency and advanced control and protection circuits is presented in this paper. The high efficiency is achieved by "dynamic partial shutdown strategy" which enhances circuit speed with less power consumption. Automatic PWM and "pulse frequency modulation" switching boosts conversion efficiency during light load operation. The modified current sensing circuit and slope compensation circuit simplify the current-mode control circuit and enhance the response speed. A simple high-speed over-current protection circuit is proposed with the modified current sensing circuit. The new on-chip soft-start circuit prevents the power on inrush current without additional off-chip components. The dc–dc converter has been fabricated with a 0.6 μm CMOS process and measured 1.35 mm^2 with the controller measured 0.27 mm^2. Experimental results show that the novel on-chip soft-start circuit with longer than 1.5 ms soft-start time suppresses the power-on inrush current. This converter can operate at 1.1 MHz with supply voltage from 2.2 to 6.0 V. Measured power efficiency is 88.5–96.7% for 0.9 to 800 mA output current and over 85.5% for 1000 mA output current.**

***Index Terms*—Compensation ramp, current sensing, current-mode control, over-current protection, power management, pulse frequency modulation (PFM), pulse width modulation (PWM), soft-start, switching dc–dc converter.**

I. Introduction

PORTABLE battery-operated devices are more and more popular today. For these devices, small size, light weight, and long battery run-time are the main demands. The batteries had become a main portion in space and weight of these portable devices. As a result, enhancing the efficiency of power supply and management is very important to minimize the size and weight and to extend the battery run-time. The well-known power management strategy, sleep mode, shuts down the unused partial circuit to effectively reduce the power consumption [1]. Although sleep mode can save the power effectively in standby mode, there is no power saving in active mode because it operates with full current. The way of saving the power is to reduce the operating current but this usually reduces the circuit performance such as speed and noise immunity.

We focused on increasing the power efficiency and reducing die size without sacrificing high speed operation. Besides, safety operation is also an important consideration in power supply design. In this paper, we propose the dynamic partial shutdown strategy (DPSS), current sensing, over-current protection, soft-start and pulsewidth modulation–pulse frequency modulation (PWM-PFM) operation to achieve our goal.

The DPSS manages the power consumption at active mode to enhance the circuit performance per power consumption. Improvement was obvious, especially in lighter load with the PFM mode control [2].

Moreover, we modified the current sensing and slope compensation circuits in current-mode control [3]–[11] to simplify the design flows of various specifications. In current sensing circuit, a simple over-current protect comparator is developed. Its response speed is faster than the conventional comparator [10], [12], [13]. But it consumes no additional quiescent power. With this circuit, the over-current protection, which is essential to voltage regulator, can be designed easily.

Most portable electronic devices have more than one power supply modules. Anyone of them may be shut down when the circuit supplied by it is unused. However, if we turn on the power supply module and don't handle the load current demand from next stage properly, the inrush current demand to previous stage will result in impulse voltage drop and affect the circuit operation or shorten the life-time of batteries. On the other hand, inrush current can also cause the output to overshoot [14]. To overcome the induced effects, a soft-start time, usually $1 \sim 10$ ms for portable electronic devices, is required at the beginning of the turn-on stage for voltage regulators. During soft-start time, the corresponding voltage regulator charges the output capacitor slowly, and then no inrush current is generated to affect the pre-stage circuit or to cause output overshoot. The conventional method of generating the soft-start time is costly in area [12], [15], [16] or need the extra pin-out and discrete capacitor [14], [17]–[20]. This method results in the increase in cost, size and weight. This paper also presents a simple and area-effective circuit to generate soft-start time without the extra pin-out and discrete capacitor. This circuit has the soft-start time proportional to the square of silicon area and is suitable for even longer soft-start time (>10 ms) applications.

Structure of current-mode PWM and PFM control are introduced in Section II, [2], [21]. Circuit implementations of the controller are discussed in Section III.

All the circuits mentioned above are integrated in a monolithic buck converter and implemented in a 0.6 μm CMOS process. It can operate in a wide input range from 2.2 to 6.0 V. Measurement results are shown in Section IV and conclusion is in Section V.

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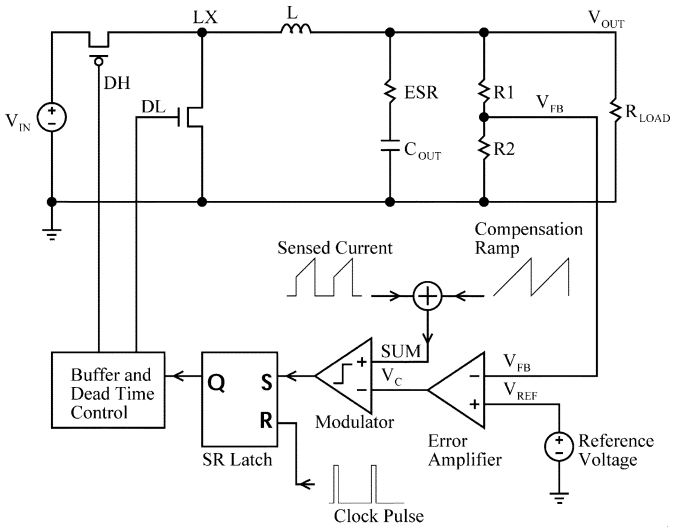


Fig. 1. Simplified structure of current-mode PWM control.

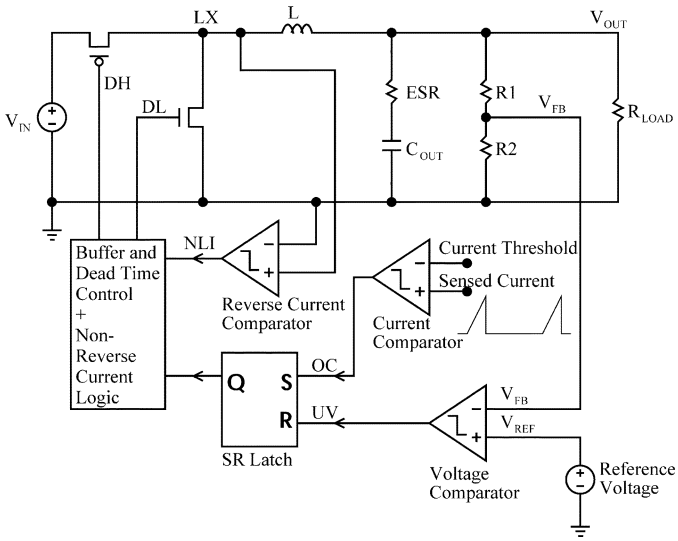


Fig. 2. Simplified structure of PFM control.

II. Structure of the Monolithic Buck Converter

In this section, we will briefly introduce the structure of current-mode PWM and PFM operation in the developed monolithic buck converter [2], [21].

A. PWM

At moderate to heavy loads, the converter operates in PWM mode. The block diagram of a simplified current-mode PWM buck converter is illustrated in Fig. 1. A clock pulse at the R (reset) input of SR Latch initiates the switching period, causing the latch output Q to be low. The latch output Q goes through Buffer and Dead Time Control to produce both DH and DL low to turn on the high side PMOS transistor and turn off the low side NMOS transistor. While the high side transistor conducts, its current is equal to the inductor current. This current increases in a certain positive slope according to the inductor value and converter voltages. We sense the high side transistor current and compare it with the control voltage V_C. When the sensed current signal becomes higher than control voltage V_C, the modulator output will be high to set the SR Latch output Q high. Again the latch output Q goes through Buffer and Dead Time Control to produce both DH and DL high to turn off the high side PMOS transistor and turn on the low side NMOS transistor until next clock pulse. We see the current controlled through the control voltage V_C and thus is named current-mode control. On the other hand, a compensation ramp is added to the sensed current signal to suppress sub-harmonic oscillation at duty ratio $>50\%$ [3].

B. PFM

With decreasing load current, the converter automatically switches into PFM mode in which the power stage operates intermittently, based on load demand. Due to reduced switching activity at power stage, the switching losses are minimized, and the device runs with a minimum quiescent current and maintains high efficiency. The block diagram of a simplified PFM mode buck converter is illustrated in Fig. 2. The output voltage is monitored with a voltage comparator. As soon as the output voltage falls below the nominal value, the output of the voltage comparator resets the SR Latch. Through Buffer and Dead Time Control the high side PMOS transistor is turned on and the inductor current ramps up. When a current comparator detects that the inductor current reaches the preset peak current, its output sets the SR Latch and turn off the high side PMOS transistor and turn on the low side NMOS transistor. As the inductor current ramps down, a reverse current comparator detects if the inductor current begins to flow in reverse direction. When this is the case, the Reverse Current Comparator turns off the low side NMOS transistor to prevent drawing energy from output capacitor back to ground. When the output voltage falls below the nominal voltage again, the next cycle is started. As the load current decreases, the time interval between two successive pulses will become larger and vice versa.

C. Automatic PWM/PFM Mode Switching

There are many algorithms of switching between PWM and PFM. In this paper, we use a hysteresis switching algorithm to prevent repeatedly switching between two modes during steady state operation. The algorithm can be described as follows.

1) In PWM mode, as the load current decreases, the inductor current may ramp to zero before the end of each clock cycle. In order to increase the efficiency, the low side NMOS will be turned off when the inductor current ramps to zero. This action prevents the current flowing in reverse direction from output capacitor to ground through inductor and low side NMOS. Thus, the converter enters discontinuous conduction mode (DCM). When the converter operates in DCM, it means that the load current is small and we don't need continuous full-cycle-pulses to sustain it. If the converter operates in DCM for about 20 μs, it will automatically switch to PFM mode.
2) In PFM mode, the peak current of each pulse is preset to a constant value as described above. We monitor the output voltage to determine when the next pulse should be issue. The next pulse will be issue if the output voltage falls below the nominal value. When the load current increases, the

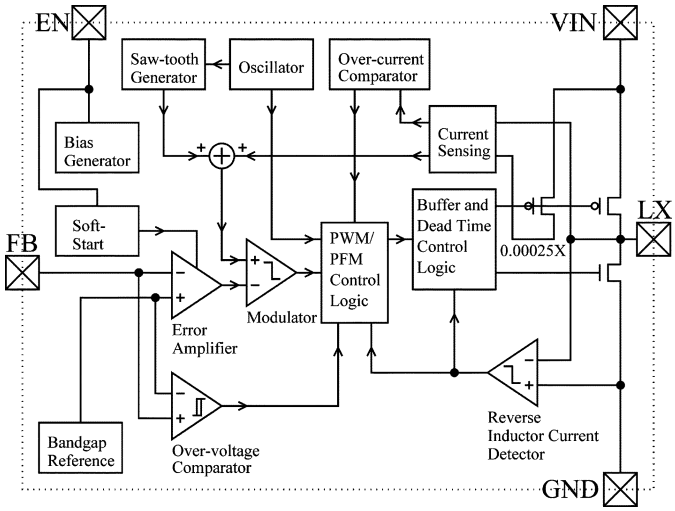


Fig. 3. Functional block diagram of the developed monolithic buck converter.

output voltage falls faster and the two pulses in succession will become closer. If the output voltage falls below the nominal value after the peak current is reached and before the current ramps back to zero, it means that we need to issue the next pulse even before the present pulse is completed. In this condition, the load current is large and the output voltage cannot be sustained with this preset current pulse. Thus the converter will enter PWM mode again.

D. Proposed Converter

Fig. 3 shows the simplified block diagram of the developed converter chip. It uses PWM and PFM control as described above. Key elements such as on-chip soft-start, DPSS, current sensing, modulator, and over-current comparator will be described in the next section.

III. Design Considerations and Circuit Implementations

A. On-Chip Soft-Start Circuit

There are mainly two kinds of conventional soft-start circuits. One is the clock-based soft-start circuit which raises the reference voltage or maximum output current or duty cycle slowly [12], [15], [16]. In this method, the way to achieve the longer soft-start time (>1 ms) is to reduce the clock frequency or increase the bit-length of counter. The former one fails to reach the goal of raising the switching frequency to minimize the energy storage elements (such as inductors and capacitors) and to enhance the response speed in switching regulator design. A separate clock can be used for soft-start, but it requires extra die area and power. The latter one, however, consumes large silicon area. Moreover, the clock-based soft-start needs time-to-voltage or time-to-current-limit circuits.

The other soft-start method charges the capacitor with a constant current to generate a steadily rising voltage. This steadily rising voltage can be used as reference voltage during startup or to limit the duty ratio or output current during startup [14], [17]–[20]. The soft-start time can be calculated as

$$t_{\text{soft-start}} = V_{\text{REF}} \times C/I. \tag{1}$$

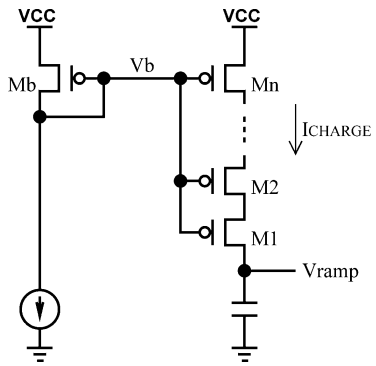


Fig. 4. Soft-start ramp generator.

Note that V_{REF} is the reference voltage or a threshold voltage which determines the end of startup, C is the capacitor value and I is the charging current.

In previous works [14], [17]–[20], extra pin-out and discrete capacitor were needed to reach longer soft-start time (>1 ms). For example, if V_{REF} equals 0.6 V and 1 ms soft-start time is needed with 1 μA charging current, a 1.67 nF capacitor is needed. Our goal is to minimize the capacitor using small charging current. For integration of capacitor on die, the order of capacitor is picofarad. Correspondingly, the charging current is in the order of nanoampere. In [22]–[25], complex bias circuit is needed to generate the bias current in nanoampere order. In addition, transistors must operate in deep subthreshold region. The I–V characteristic of MOS transistor operates in the deep subthreshold region is [26]

$$I_D = k_x \frac{W}{L} e^{\frac{V_{\text{GS}}}{nV_t}} \left(1 - e^{-\frac{V_{\text{DS}}}{V_t}}\right) \tag{2}$$

where k_x depends on process, $n \approx 1.5$ and V_t is the threshold voltage of the transistor. The effectiveness of gate drive voltage (V_{GS}) to drain current (I_D) is exponential. Noise on the gate drive voltage will greatly affect the drain current. So that deep subthreshold bias is not suitable for a noisy environment like switch-mode power supply with integrated power switches.

In this paper, a simple circuit is proposed as shown in Fig. 4. Note that, V_b can be generated by a simple bias circuit or the existing bias voltage in the system. In Fig. 4, for a general bias circuit

$$|V_b - VCC| = |V_{\text{GS}(M_b)}| > |V_{t(M_b)}|. \tag{3}$$

The transistor M_b operates in saturation region. We can use simple MOS transistor equations in [26]:

Saturation region $(V_{\text{GS}} > V_t, V_{\text{DS}} > V_{\text{GS}} - V_t)$

$$I_D = \frac{1}{2}\mu \cdot C_{\text{OX}} \frac{W}{L}(V_{\text{GS}} - V_t)^2. \tag{4}$$

Triode region $(V_{\text{GS}} > V_t, V_{\text{DS}} < V_{\text{GS}} - V_t)$

$$I_D = \mu \cdot C_{\text{OX}} \frac{W}{L}\left[(V_{\text{GS}} - V_t) \cdot V_{\text{DS}} - \frac{1}{2}V_{\text{DS}}^2\right] \tag{5}$$

where μ is mobility and C_{OX} is oxide capacitance. When V_{ramp} is well below *VCC*, transistor M_1 operates in saturation region. Other series transistors $M_2 \sim M_n$ operate in triode region. Therefore, $M_2 \sim M_n$ are like the $(n-1)$ linear resistances

whose total voltage drop is slightly smaller than $(V_{\rm GS} - V_t)$. For small $V_{\rm DS}$, we approximate (5) to

$$R_{\rm DS} = \left[\mu \cdot C_{\rm OX}\frac{W}{L}(V_{\rm GS} - V_t)\right]^{-1}. \quad (6)$$

Then, according to Ohm's law, we have

$$I_{\rm CHARGE} = I_{D(M_1)} = I_{D(M_2 \sim M_n)} = \frac{VCC - V_{D(M_2)}}{R_{{\rm DS}(M_2)} + \cdots + R_{{\rm DS}(M_n)}}. \quad (7)$$

As a result, the nanoampere order charging current can be achieved easily in today's technology. For example, if $V_{\rm REF}$ equals to 0.6 V, 1 ms soft soft-start time is available with a 1-nA current to charge the 1.67-pF capacitor. In our design, the soft-start circuit occupies only 56.1×65.4 μm^2 and reaches longer than 1.5 ms soft-start time.

Another advantage of this circuit is that the soft-start time is proportional to the square of the silicon area. According to (1), for a fixed reference voltage, the soft-start time is proportional to the capacitor value and reverse proportional to the charging current. In (7), the charging current is reverse proportional to the summation of $R_{\rm DS}$ of transistors. Thus we have the soft-start time proportional to the series number of PMOS. If we increase both the capacitor value and the series number of PMOS with the same ratio, the soft-start time is proportional to the square of the silicon area. The proposed method can reduce the silicon area dramatically and this circuit does not need extra pin-out and discrete capacitor.

B. Dynamic Partial Shutdown Strategy

For extension of battery run time of portable devices, dynamic power management uses sleep mode which shuts down unused circuits to save power during standby mode [1]. However, in active mode, it cannot save the power consumption because of the full operating current. In this paper, the dynamic partial shutdown strategy (DPSS) controlling the turn off of partial circuits is proposed to save the power consumption, especially in active mode. During active mode, only the essential parts will be turned on in specific operating situation under DPSS. As a result, the power consumption is minimized and battery run time is extended.

In a switch-mode power supply, the decision of when to turn on or turn off switches was made according to the output voltage and current condition in each switching cycle. When the switch is on, we need to decide when to turn it off; when the switch is off, we need to decide when to turn it on again. According to this characteristic of switch-mode power supply, we can turn off partial circuits which are not needed to decide when the switch should be turned off during "ON" state and vice versa. Since there are digital signals indicating the ON and OFF states of the power switches in the converter, we can use these digital signals to turn on and turn off the partial circuits which are not needed in each state.

Take the proposed converter as an example. In Figs. 5 and 6, we use horizontal, vertical, and oblique lines to indicate shut down parts. Blocks with horizontal lines are shut down when high side PMOS is turned on. Blocks with vertical lines are shut down when low side NMOS is turned on. Blocks with oblique lines are shut down when both power transistors are turned off. Fig. 5 shows circuits operate in PWM mode; and Fig. 6 in PFM mode. Note that the soft-start time has been completed and the Soft-Start in Figs. 5 and 6 is always shut down.

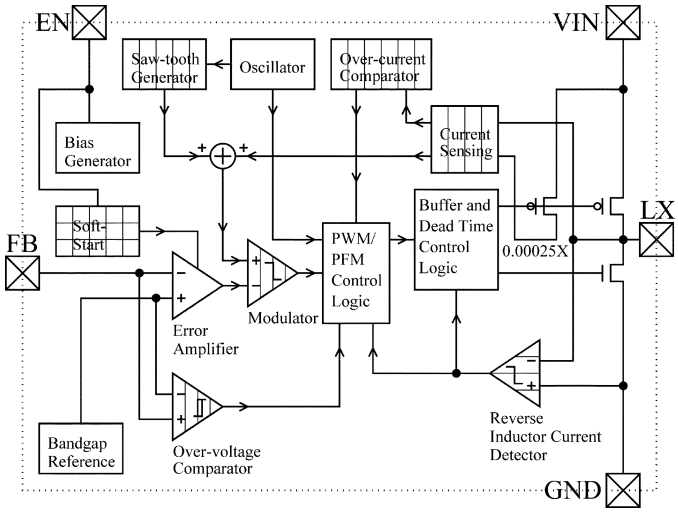


Fig. 5. DPSS in PWM mode. Blocks with horizontal lines are shut down when high side PMOS is turned on. Blocks with vertical lines are shut down when low side NMOS is turned on.

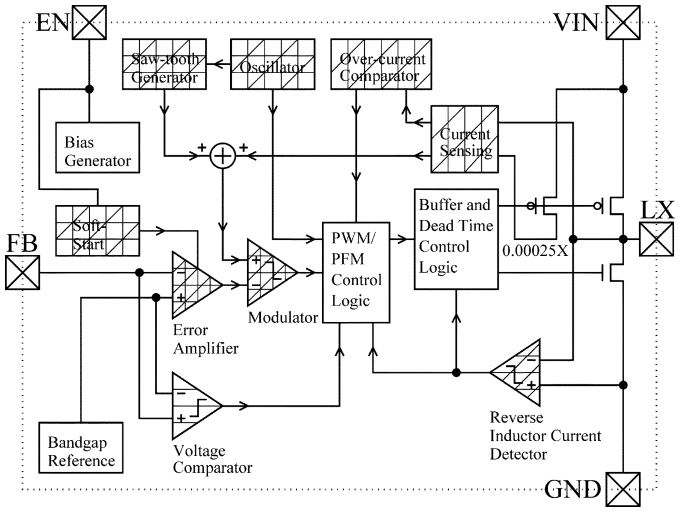


Fig. 6. DPSS in PFM mode. Blocks with horizontal lines are shut down when high side PMOS is turned on. Blocks with vertical lines are shut down when low side NMOS is turned on. Blocks with oblique lines are shut down when both power transistors are turned off.

In PWM mode, when high side PMOS is turned on, the slope of inductor current is positive. So we don't need to detect reverse inductor current and the Reverse Inductor Current Detector can be turned off. When low side NMOS is turned on and that the slope of inductor current is negative, there is no need to detect the over-current and the Current Sensing and Over-current Comparator can be shut down. Since the slope of inductor current is negative, the Over-voltage Comparator cannot do anything more to prevent output voltage from going too high. Thus the Over-voltage Comparator can be shut down. Besides, the next turning on of high side PMOS is decided by clock pulse in constant frequency leading edge modulation [27].

The Saw-tooth Generator, Analog Adder, and Modulator can also be shut down.

In PFM mode, the Error Amplifier, Oscillator, Saw-tooth Generator, Analog Adder, and Modulator all can be shut down. When high side PMOS is turned on, only the peak inductor current decides when to turn it off. As a result, the Voltage Comparator and Reverse Inductor Current Detector can be shut down. When low side NMOS is turned on, the Current Sensing and Over-current Comparator can be shut down. When both high side PMOS and low side NMOS are turned off, only the Voltage Comparator is active to decide when the high side PMOS should be turned on again.

When using DPSS, care must be taken as dealing with analog signal level between ON and OFF states. For example, if the analog signal level of the Current Sensing is not preset correctly when the Current Sensing is turned off, the Current Sensing may give wrong information about the inductor current at the beginning of next cycle. This wrong information may result in unstable operation. On the other hand, timing of digital signal is also an important issue. For example, if the Over-voltage Comparator is not turned on slightly before the next cycle, the next pulse may cause the output voltage goes even higher during transient conditions. This high voltage may damage the circuits in load stage.

Simulation results show that in PWM mode, operating current can be reduced from 500 μA to 250 $\sim$300 μA, depending on the duty ratio. In PFM mode, operating current can be reduced from 200 μA to 50 μA. The reduced operating current can effectively boost conversion efficiency especially in light load operation. For example, when $V_{\rm IN} = 3.6$ V, $V_{\rm OUT} = 2.5$ V and $I_{\rm LOAD} = 1$ mA, the conversion efficiency is 89% and 75% with and without DPSS, respectively. Higher input voltage and lower load current will increase the difference. When $V_{\rm IN} =$ 4.2 V, $V_{\rm OUT} = 2.5$ V and $I_{\rm LOAD} = 1$ mA, the results are 88% and 72% with and without DPSS, respectively. When $V_{\rm IN} =$ 3.6 V, $V_{\rm OUT} = 2.5$ V and $I_{\rm LOAD} = 0.5$ mA, the results are 84% and 62% with and without DPSS, respectively.

C. Current Sensing and Slope Compensation

The current sensing circuit is one of the most important building blocks in current-mode control. There are many current sensing circuits available [4]–[11]. Among them we choose the current-conveyor-based sense-FET current sensing [5]–[10], [28] because it has some good features as follows.

1) It dose not need the extra pin-out and external component.
2) Its quasi-lossless characteristic could enhance the efficiency [9].
3) Matching devices, instead of $R_{\rm DS(ON)}$ of MOSFET or passive component such as resistors, are used to improve accuracy (reported higher than 94% accuracy [5], [6]).
4) It can operate in low voltage [6] and has improved noise immunity [10].
5) It can be easily compensated [10] and has high speed response [10].

The current sensing circuit is shown in Fig. 7. The second generation negative current conveyor (CCII-) [28] is enclosed in the dashed box. In our current sensing circuit design, we use the second generation current conveyor (CCII-) instead of the

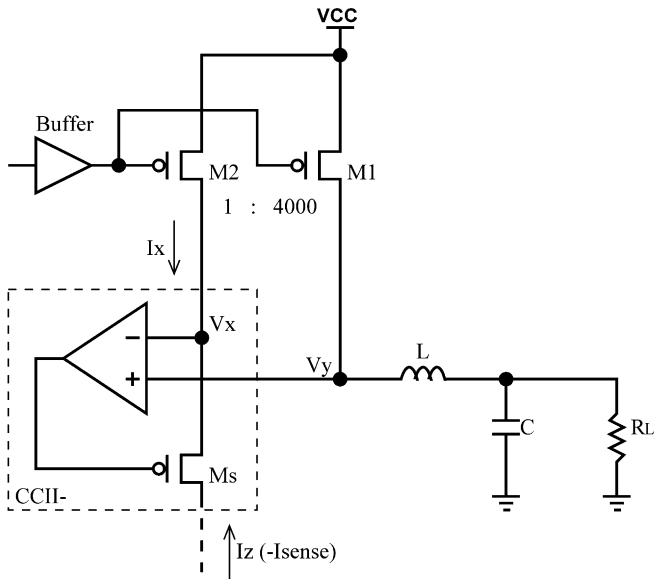


Fig. 7. Current-conveyor-based sense-FET current sensing.

first generation current convey (CCI) used in [5]–[8]. The CCII has no current flow in terminal Y, thus eliminates the unused power dissipation and extra circuits. According to the principles of CCII-[28], (8) and (9) were shown as follows:

$$V_X = V_Y \tag{8}$$

$$I_Z = -I_X. \tag{9}$$

According to (4) and (5), when $V_{\rm DS(M2)} = V_{\rm DS(M1)}$ and $V_{\rm GS(M2)} = V_{\rm GS(M1)}$, we obtained

$$I_{D(M_2)} : I_{D(M_1)} = \left(\frac{W}{L}\right)_{(M_2)} : \left(\frac{W}{L}\right)_{(M_1)}. \tag{10}$$

From (9) and (10)

$$I_{\rm sense} = I_Z = -I_X = I_{D(M_2)} = \left(\frac{W_{(M_2)} \cdot L_{(M_1)}}{W_{(M_1)} \cdot L_{(M_2)}}\right) \cdot I_{D(M_1)}. \tag{11}$$

And the relationship of the sensed current and the inductor current can be determined by the aspect ratio of M_1 and M_2. As a result, accurate current information is obtained for the control loop of the current-mode control.

When dealing with current-mode control, there is a well known instability problem for duty ratio greater than 50% [3]. An artificial ramp acts as slope compensation must be added to the sensed current signal to suppress the sub-harmonic oscillation of the converter. How to generate a compensation ramp and add it to the sensed current signal is another issue. Conventionally, both the output of current sensing and the compensation ramp are expressed in "voltage" form [4]–[11]. We need a summing amplifier to add the compensation ramp ($V_{\rm ramp}$) to the sensed current signal ($V_{\rm isense}$) as shown in Fig. 8(a) [4]. Another solution is to convert the current information ($V_{\rm isense}$) and compensation ramp ($V_{\rm ramp}$) to "current" form by V-to-I converters, respectively. Then we add these two current together and get the summing voltage through a single resistor as shown in Fig. 8(b), [5], [6]. These methods

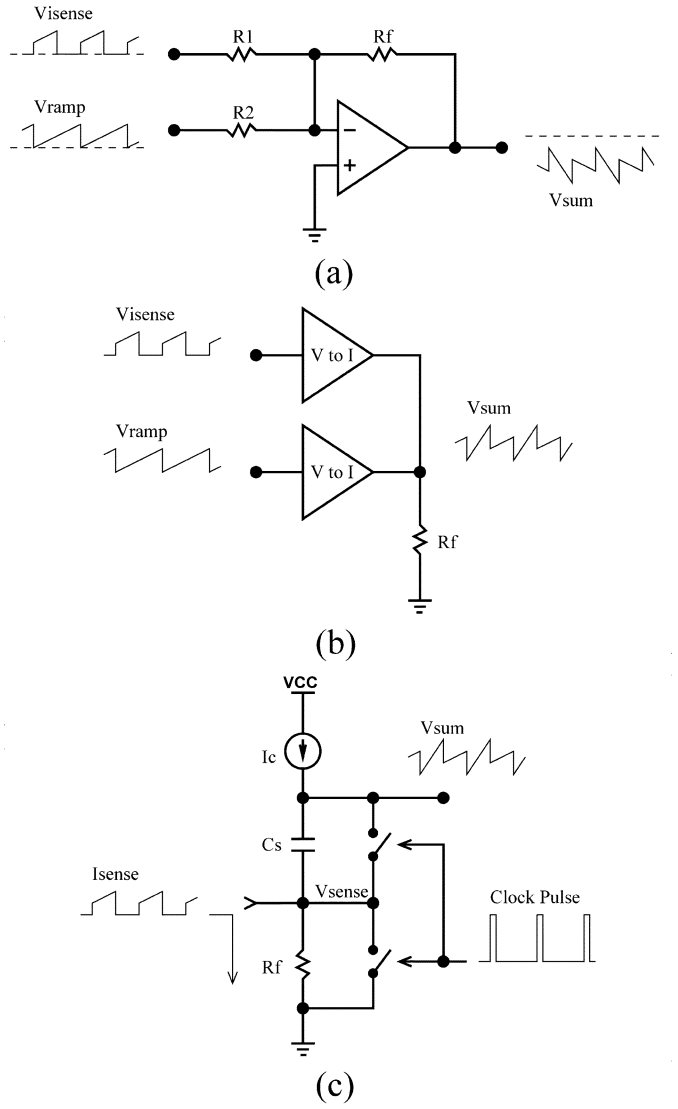


Fig. 8. Different methods of adding compensation ramp to sensed inductor current signal. (a) Summing amplifier. (b) Use two V-to-I converters and adding the current signals by a resistor. (c) Proposed summing circuit.

need multiconverts with complex circuits, and correspondingly, inducing more distortion to the desired signal.

To solve the above problem, we propose a simple and effective circuit as shown in Fig. 8(c). Because the output signal $I_{\rm sense}$ of the current-conveyor-based sense-FET current sensing mentioned above is in current form, it does not need a V-to-I converter. On the other hand, the compensation ramp can be generated by charging a capacitor with a constant current and discharging it with clock pulses. In Fig. 8(c), we leave out another V-to-I converter and directly connect the capacitor C_S to a resistor R_f. One end of the resistor R_f is grounded. $I_{\rm sense}$ and a constant current I_C flow into the top of C_S and R_f, respectively. The capacitor C_S and resistor R_f were grounded periodically by clock pulses. And we have the summing voltage $V_{\rm sum}$ at the top of Cs. We can calculate the $V_{\rm sense}$ and $V_{\rm sum}$ as follows:

$$V_{\rm sense} = (I_{\rm sense} + I_C) \cdot R_f \tag{12}$$

$$V_{\rm sum} = (I_{\rm sense} + I_C) \cdot R_f + \int_0^t \frac{I_C}{C_S} \tag{13}$$

where t is the time elapsed from the end of clock pulse in each cycle. Except the desired sum of current information and compensation ramp, here we have an extra term "$I_c \times R_f$" in $V_{\rm sum}$. This extra term is a constant value and can be used as a dc bias to avoid $V_{\rm sum}$ falling into the nonlinear region of error amplifier output [11]. For different applications of converter design, we can simply adjust the values of C_S and R_f to change the compensation slope or current gain to have the desired result.

D. Over-Current Protection

Over-current protection is very important in power supply design for safety reason. One of the benefits of current-mode control is cycle-by-cycle current limitation. However, because of the minimization of the inductor and the higher slope of current ramp, the switching frequency goes higher. As a result, the over-current protection needs higher speed in response to ensure safety.

The conventional over-current protection compares the sensed current signal (in voltage) with a reference voltage [10], [12]. If the sensed signal is higher than the threshold, it turns off the main switch (In our case the main switch is the high side PMOS) with an over-current signal as shown in Fig. 9(a). The comparator delay was undesirable. In traditional voltage comparator design, for most circuit topology, the basic way to increase response speed is to increase operating current [13]. However, it is at the expense of power consumption and also conversion efficiency. Moreover, when the operating current goes higher, the speed of traditional voltage comparator will saturate due to the increase of parasitic capacitance and even larger operating current cannot help either.

To solve this problem, we propose a new over-current protection circuit as shown in Fig. 9(b). As mentioned in the preceding section, the $I_{\rm sense}$ is in current form. We utilize this characteristic of current sensing circuit and use a single transistor to achieve over-current protection. Note that the bias circuit located in left-down of Fig. 9(b) can be any simple bias circuit used by other circuits in the converter to generate a bias voltage V_b. From (4) and (5), we know that when

$$I_{\rm sense} > I_{D({\rm sat.})(M_1)} = \frac{1}{2}\mu \cdot C_{\rm OX}\frac{W}{L}(V_{\rm GS} - V_t)^2 \tag{14}$$

the drain voltage increases dramatically and the speed is determined by the excess current and parasitic capacitance at drain node. Inherently, it operates faster than the conventional voltage comparator. Moreover, because the current sensing and bias circuits are not newly created parts in the circuit, the quiescent current of the over-current protection circuit is zero. As a result, the simple circuit deals with the comparator response speed and power consumption at the same time.

This circuit can be easily adjusted to fit various applications. As we know the value of $I_{\rm bias}$ and the aspect ratio of M_b, we can easily adjust the aspect ratio of M_1 to reach the desired current limit. Note that the $V_{\rm DS(sat)}$ (equals to $(V_{\rm GS} - V_t)$) must be smaller than the logic threshold to avoid M_1 operating in triode region, or the current limit will be smaller than the expected value and cannot be well defined.

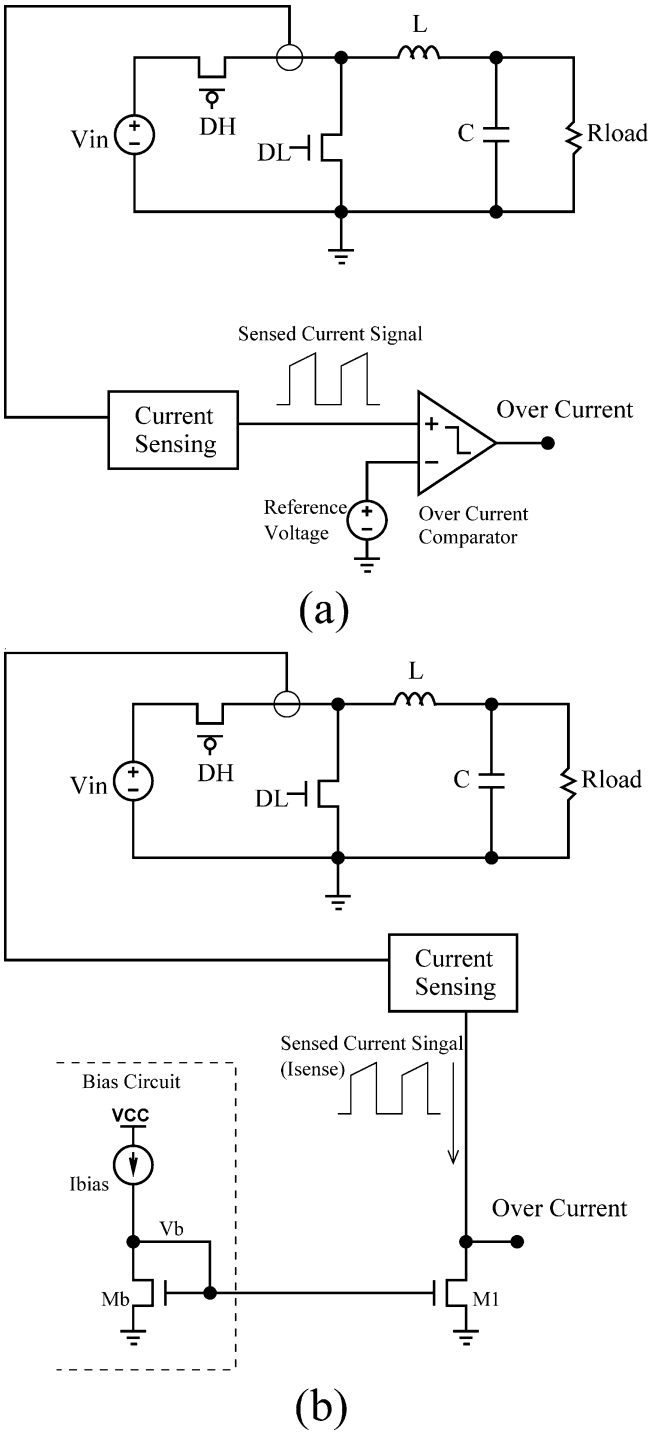


Fig. 9. Over-current protection circuit. (a) Conventional over-current protection circuit. (b) Proposed over-current protection circuit.

IV. Experimental Results

All circuits described above are integrated in a monolithic current-mode buck converter and realized using a 0.6-μm 1P2M logic CMOS process. Fig. 10 shows the microphotograph of the silicon chip. The whole chip area is 1.35 mm^2 including the power MOSFETs and voltage reference circuit. The controller is measured 0.27 mm^2 including frequency compensator and on-chip oscillator. It doesn't need any pin-out and off-chip component for frequency compensation, voltage reference and clock generator. The experimental setup is shown in Fig. 11. There are only six off-chip components needed, including bypass capacitor $(C_{\rm IN})$ for $V_{\rm IN}$, filtering inductor $(L_{\rm OUT})$ and capacitor $(C_{\rm OUT})$, resistors (R_1 and R_2) for setting the output voltage and a small capacitor $(C_{\rm FB})$ for compensation of the parasitic capacitance at $V_{\rm FB}$. The total PCB area was minimized. A typical set of component values is listed in Table I. Unless otherwise specified, the following results are measured using the component values listed in Table I.

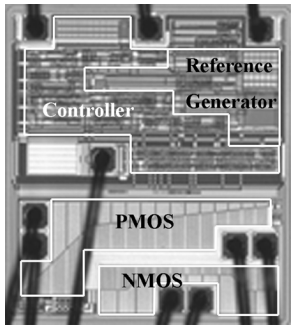


Fig. 10. Chip microphotograph.

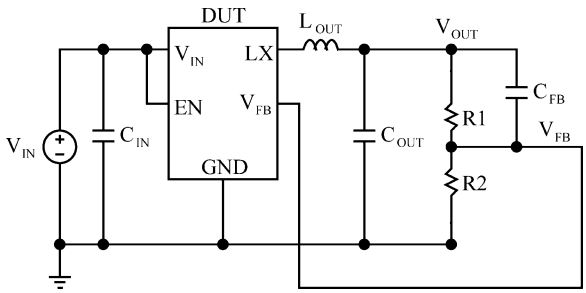


Fig. 11. Experimental setup of the monolithic buck converter.

TABLE I
List of Component Values Used in Test Setup

C_{IN}	10 μF
L_{OUT}	4.7 μH
C_{OUT}	10 μF
R_1	1000 kΩ
R_2	316 kΩ
C_{FB}	22 pF
V_{IN}	3.6 V
V_{OUT}	2.5 V

A. Soft-Start

The soft-start function has been tested. Fig. 12 shows the simulated input current and output voltage waveforms for 2.5 Ω (≈ 1000 mA) load at startup. Fig. 13 shows the measured input current and output voltage waveforms at startup. We can see the experimental results match the simulation prediction. The soft-start function with soft-start time longer than 1.5 ms effectively suppresses the inrush current and overshooting of output voltage during startup. The measured soft-start time doesn't change for various input voltage, output voltage and load current. It can be seen that both the input current and the output voltage follow the internal soft-start ramp until they reach the steady-state values.

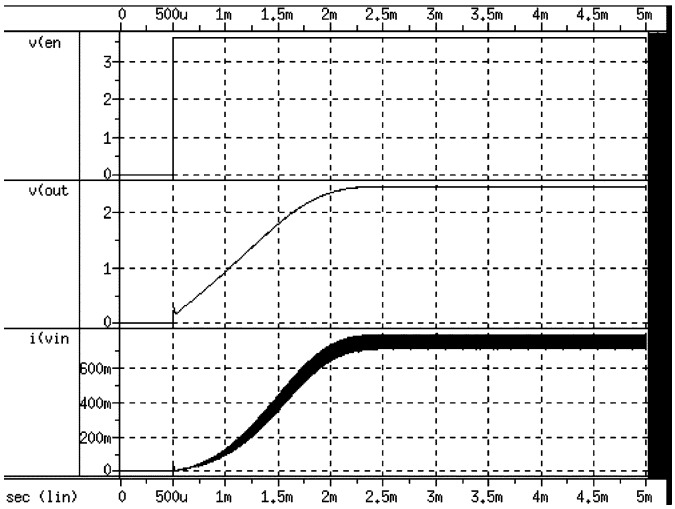


Fig. 12. Simulated waveforms of input current and output voltage during startup with 2.5 Ω load (≈1000 mA at steady-state).

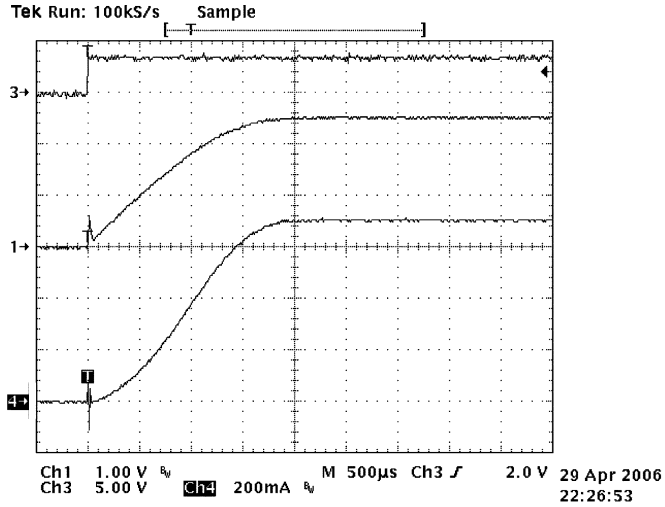


Fig. 13. Measured input current and output voltage during startup with 2.5 Ω load (≈1000 mA at steady-state). From top to bottom: Channel 3 is chip enable, Channel 1 is output voltage, and Channel 4 is input current.

B. Efficiency

The proposed converter incorporated with DPSS in both PWM and PFM mode gives very high conversion efficiency (>88.5%) in a wide load range from 0.9 to 800 mA. The measured efficiency is greater than 85.5% even at 1000 mA load. The results are shown in Fig. 14(a). Since we use a hysteresis switching algorithm for automatic PWM/PFM mode switching, the efficiency curves of PWM and PFM mode are overlapped over certain load range in Fig. 14. The maximum efficiency is over 96% at 60–200 mA load and peaks over 96.7% at 100 mA load under PWM mode. In PFM mode, the maximum efficiency is over 95% at 100–200 mA load.

Fig. 14(b) shows the measured conversion efficiency for $V_{\rm IN} = 4.2$ V. The efficiency still peaks over 96% for 120–200 mA load and is greater than 86% for 0.8–1000 mA load.

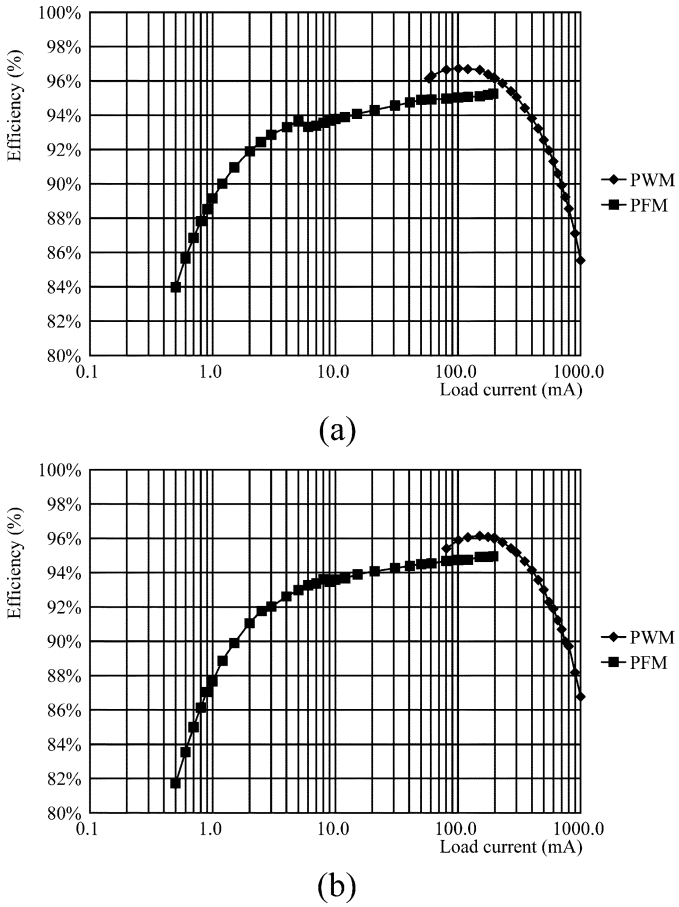


Fig. 14. Measured conversion efficiency. (a) $V_{\rm IN} = 3.6$ V and $V_{\rm OUT} = 2.5$ V. (b) $V_{\rm IN} = 4.2$ V and $V_{\rm OUT} = 2.5$ V.

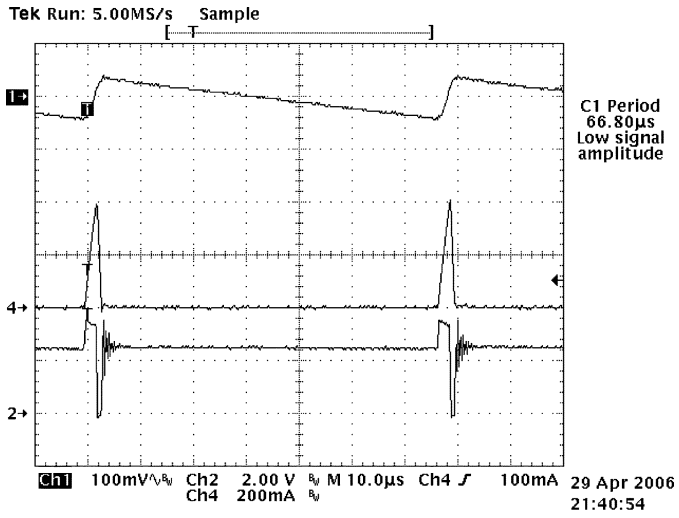
C. Steady-State and Transient Response

In PFM mode, the measured quiescent current is 48.6 μA with DPSS. The waveforms of PFM operation are shown in Fig. 15. The interval between two switching pulses is defined by load current. For heavier load, the switching pulses will get closer, and vise versa.

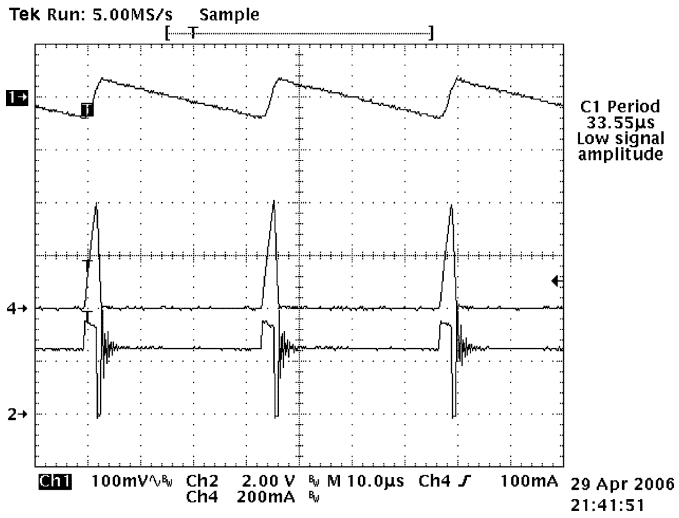
Fig. 16 shows the steady-state waveforms in PWM mode. It can be seen that the converter is stable without sub-harmonic oscillation in both duty ratio greater and smaller than 50%. Ripples on output voltage are less than 3 mV. Measured line and load regulation are 0.07%/V and 0.08%/A, respectively. Transient response is shown in Fig. 17. The recovery time for a 500 mA step load-transient is less than 20 μs for 1% (25mV) tolerance of the final settling value. The output voltage drops and peaks less than 80 mV (≈3.2% of the nominal value of output voltage 2.5 V) during the 500 mA load step-up and step-down transient, respectively.

D. Over-Current Protection

Fig. 18(a) shows the waveforms of output voltage and inductor current at 2.5 Ω (≈1000 mA) load (normal operation). Fig. 18(b) shows the waveform of inductor current when overloaded ($R_{\rm LOAD} = 1\ \Omega$). The proposed over-current protection circuit successfully limits the output current when overloaded. The cycle-by-cycle peak inductor current is limited to 1.28 A.

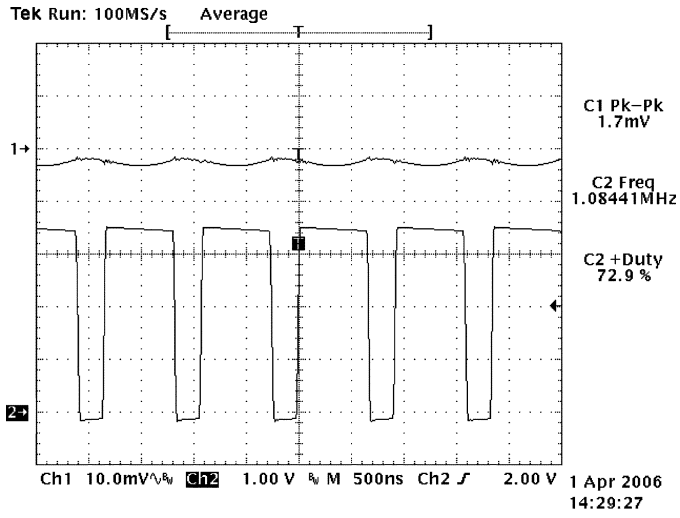


(a)

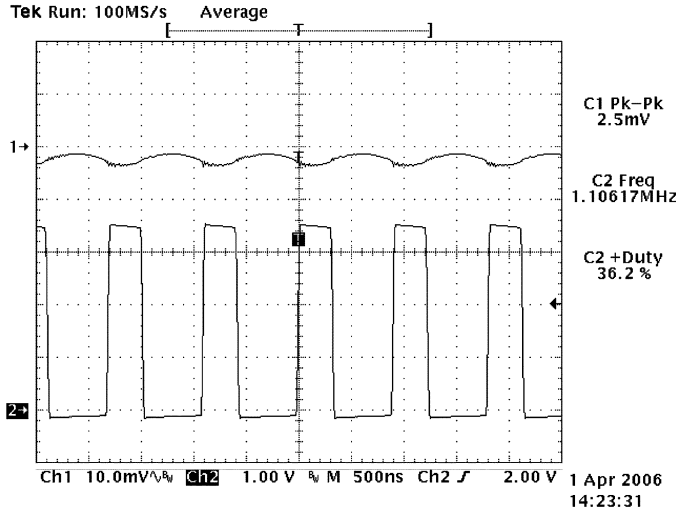


(b)

Fig. 15. Steady-state waveforms of PFM mode operation. From top to bottom: Channel 1 is output ripple voltage (ac coupled), Channel 4 is inductor current and Channel 2 is switch node LX: (a) 10 mA load and (b) 20 mA load.



(a)



(b)

Fig. 16. Steady-state waveforms of the output ripple voltage (Channel 1, ac coupled) and the switch node *LX* (Channel 2) in PWM mode. (a) Duty cycle $>50\%$. (b) Duty cycle $<50\%$.

E. Comparison

Table II summarizes the measured performance of the proposed converter. Table III shows a comparison with previously reported works [5], [29]–[32]. Incorporates with all the advancements described above, our design features the smaller die size and controller size with fewer off-chip components, higher conversion efficiency and wider operating range. Small output ripple voltage and fast transient response are also included. Besides, on-chip soft-start and over-current protection functions ensured safety. All these features are realized in a low cost 0.6 μm 1P2M logic CMOS process.

V. Conclusion

A compact high efficiency monolithic current-mode buck converter is presented in this paper. Novel features including on-chip soft-start, dynamic partial shutdown strategy, slope compensation and over-current protection circuits are demonstrated. These techniques reduce pin-outs and external components, upgrade efficiency, reduce circuit complexity and silicon

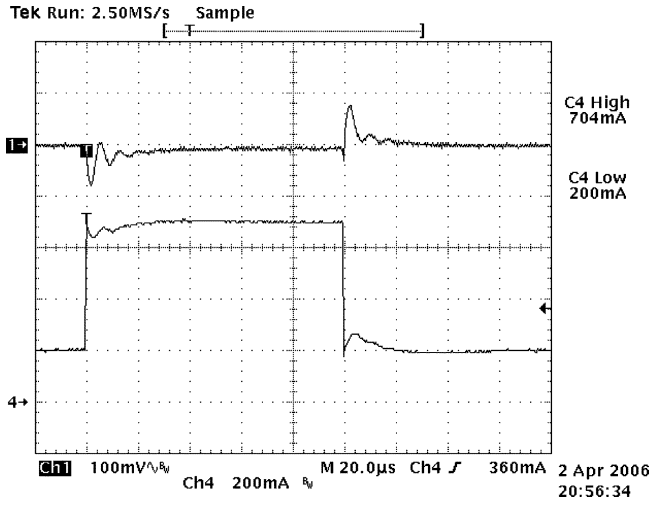
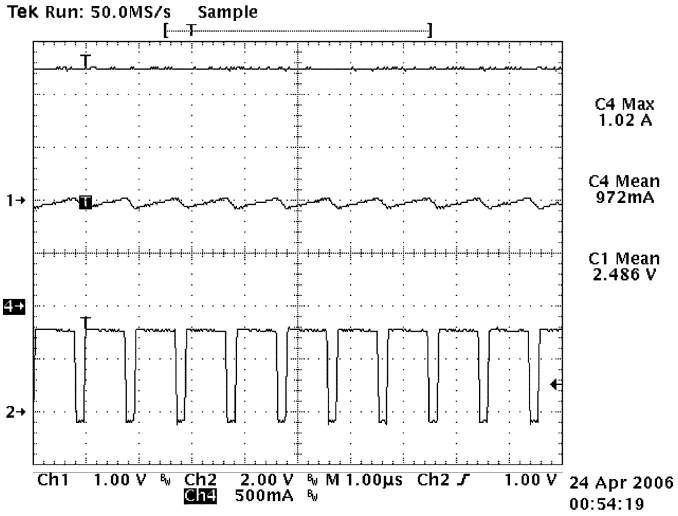
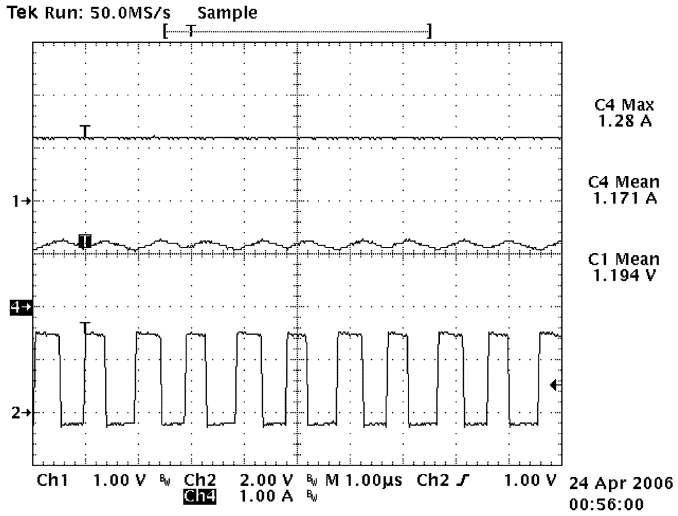


Fig. 17. 500 mA step load-transient response. Channel 1 is output voltage (ac coupled) and Channel 2 is output current (step from 200 to 700 mA and from 700 mA to 200 mA).



(a)



(b)

Fig. 18. Over-current protection test. From top to bottom: Channel 1 is output voltage (dc coupled), Channel 4 is inductor current and Channel 2 is switch node *LX*. (a) Normal operation with 2.5 Ω (≈1000 mA) load. ($V_{\rm OUT} = 2.5$ V). (b) The converter is overloaded ($R_{\rm LOAD} = 1\ \Omega$). The peak inductor current is limited to 1.28 A and the output voltage falls from 2.5 V to ≈1.2 V.

TABLE II
SUMMARY OF PERFORMANCE

Process	0.6 μm, 1P2M logic CMOS
Total die area	1.1 mm x 1.23 mm
Controller size	0.27 mm^2
Efficiency	88.5 ~ 96.7% @ 0.9 ~ 800 mA; 85.5% @ 1000 mA (V_{IN} = 3.6 V, V_{OUT} = 2.5 V)
Input voltage range	2.2 ~ 6 V
Output voltage range	0.6 V ~ (Input voltage – 0.2 V)
Max. output current	1000 mA
Soft-start	> 1.5 ms
Quiescent current	48.6 μA (PFM Mode, No Switching)
Switching frequency	1.1 MHz
Inductor	4.7 μH
Capacitor	10 μF
Output ripple voltage	< 3 mV
Line regulation	0.07%/V (Load current = 200 mA)
Load regulation	0.08%/A (Load current from 200 mA to 1000 mA)
Transient recovery time (99%)	< 20 μs @ 500 mA load step

area, ease design effort, ensure safety and can be applied to a wide operating range. The experimental results show that these novel features work well and the converter achieves very good performance at many aspects. The proposed converter is suitable especially for mobile devices that require high efficiency, small size, and safety operation.

TABLE III
PERFORMANCE COMPARISON

	[5]	[29]	[30]	[31]	[32]	This work
Technology	0.6 μm	0.25 μm	0.5 μm, 1P3M	0.25 μm	0.6 μm, 2P3M	0.6 μm, 1P2M
Die size	2.87 mm^2 (*)	1.43 mm^2	2.31 mm^2 (*)	4.16 mm^2 (*)	3.78 mm^2 (*)	1.35 mm^2
Controller size	0.2575 mm^2	0.35 mm^2	0.54 mm^2	2 mm^2	0.78 mm^2	0.27 mm^2
Max. efficiency	89.5%	95%	93.7%	92%	92%	96.7%
Input voltage range	3.0 ~ 5.2 V	2.5 V	3.3 V	2.8 ~ 5.5 V	3.3 V	2.2 ~ 6 V
Output voltage range	< Input voltage - 0.2 V	1.5 V	0.9 ~ 2.5 V	1.0 ~ 1.8 V	0.2 ~ 3.0 V	0.6V ~ (Input voltage - 0.2 V)
Max. Output current	450 mA	N/A	180 mA	400 mA	250 mA	1000 mA
Switching Frequency	0.3 ~ 1 MHz	0.46 ~ 0.86 MHz	> 1 MHz	0.5 ~ 1.5 MHz	1 MHz	1.1 MHz
Inductor	4.7 μH	15.2 μH	N/A	10 μH	2.2 μH	4.7 μH
Capacitor	10 μF	21.6 μF	N/A	47 μF	47 μF	10 μF
Output ripple voltage	20 mV	< 15 mV	< 10 mV	2 mV	< 15 mV	< 3 mV
Transient recovery time (99%)	N/A	< 10 μs @ 80mA load step	> 50 μs @ 90mA load step	N/A	50 μs @ 100mA load step	< 20 μs @ 500mA load step

(*) Reference voltage generator is not included in the chip.

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