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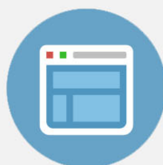
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Effective density-of-states distribution of polycrystalline silicon thin-film transistors under hot-carrier degradation

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In this work, quantitative information for nonuniform hot-carrier degradation, especially under mild stressing condition, is investigated. A test structure capable of revealing hot-carrier degradations of polycrystalline silicon (poly-Si) thin-film transistors in specific portions of the channel is employed. Effective density-of-states (DOS) distributions at the damaged sites can be extracted using field-effect conductance method, thus providing an effective tool to evaluate the impact of hot-carrier degradations. By measuring along individual sections of the channel, it becomes possible to extract the DOS for the device as a whole. The combination of the proposed test structure and DOS extraction technique also provides a powerful tool for modeling and simulating current-voltage characteristics of thin-film transistors under hot-carrier stressing. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2777804]

INTRODUCTION

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have been extensively used in many applications, especially for active-matrix liquid-crystal displays (AMLCDs).[1–4] Because of their better crystallinity, compared with the amorphous counterparts, significant improvement in device performance in terms of carrier mobility and drive current can be realized in poly-Si TFTs. Along with these improvements, the stability and reliability of the poly-Si TFTs now become a major issue. Hot-carrier degradation remains as one of the most critical concerns for practical applications.[5,6] Hot carriers are induced by high electric fields in the channel. By releasing their energy, these hot carriers could generate defects and cause device degradation.[7] Since the electric field along the channel is not uniformly distributed, hot-carrier-induced damage is location dependent along the channel. Because of the lack of substrate contacts, coupled with the presence of numerous inter-/intragrain defects,[8] the whole picture is much more complicated for poly-Si TFTs, compared with bulk metal-oxide-semiconductor field-effect transistors (MOSFETs). The damage scenarios of hot-carrier degradations have been characterized in the literature by a number of techniques, including reversed source/drain measurement,[9] capacitance-voltage (C-V) measurement,[10] device simulation,[11,12] asymmetric drain/source structure,[9] and picosecond time-resolved emission microscope.[13] However, none of the above methods is capable of directly and unambiguously pinpointing the damage location.

Modeling hot-carrier degradations is a challenging task. Trap states associated with grain boundaries, intragranular defects, and hot-carrier induced defects can be taken into account through the use of the effective density-of-states (DOS) distribution within the band gap.[14–17] However, realistic DOS distribution is very difficult to obtain owing to the nonuniform distribution of induced defects by the hot-carrier stressing. Recently, a test structure capable of spatially resolving the damage along the channel of the stressed transistor has been proposed by our group.[18] With the proposed structure, analysis of hot-carrier degradation along the stressed channel becomes feasible. In this work, modeling of the location-dependent hot-carrier degradation is investigated in detail using the proposed structure. We show that, by measuring along individual sections of the channel, it becomes feasible to extract the DOS for the device as a whole.

DEVICE EXPERIMENTAL AND SIMULATION

The test structure was originally designed to spatially detect and reveal the location of damage sites during hot-carrier stressing. The top view of the test structure is illustrated in Fig. 1(a). One test transistor along the x direction, denoted as TT, is designed to receive the hot-carrier stressing. Three monitor transistors (MTs) along the y direction, denoted as S-MT, C-MT, and D-MT, respectively, can be characterized independently before and after the stressing. In this way, damage induced at different portions of the channel can be directly resolved. Figures 1(b) and 1(c) illustrate the schematics of the test transistor and monitor transistors, respectively.

Because the proposed test structure requires only modifications in layout, the processing steps are identical to those of conventional TFTs. No extra masks or lithography steps are needed when employing the test structure. TFTs in this work were prepared on oxidized Si wafers with a 50-nm-thick polycrystalline silicon layer to serve as the active device region. The polycrystalline silicon layer was formed by depositing an amorphous silicon layer and then

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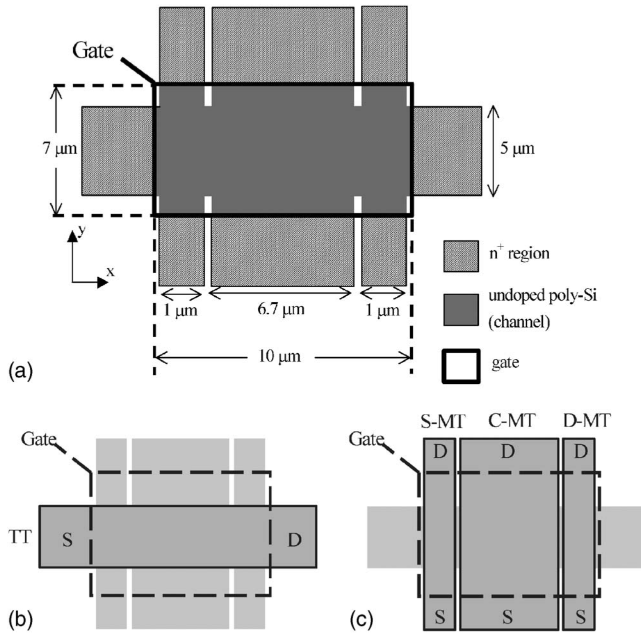

FIG. 1. Schematic and operating configurations of the test structure.

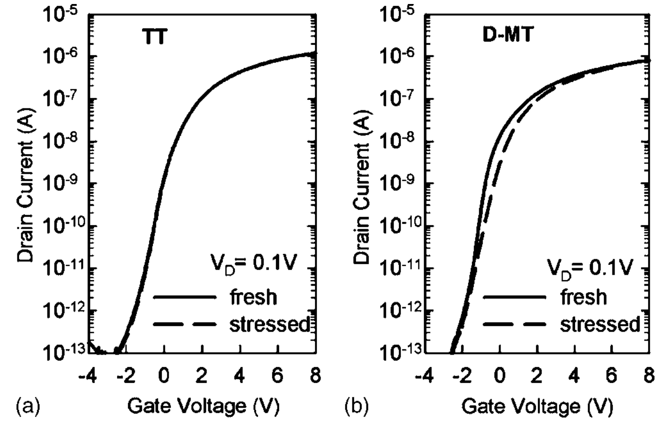

FIG. 2. Subthreshold characteristics of (a) TT and (b) *D*-MT, before and after hot-carrier stressing under V_G/V_D=6.5 V/13 V for 1000 s.

crystallizing it at 600 °C in N_2 for 24 h. Afterwards, a 35-nm-thick tetra-ethyl-ortho-silicate (TEOS) and 200-nm-thick n^+ poly-Si were deposited and patterned to form the gate dielectric and gate electrode, respectively. Standard processing for source/drain formation, passivation, and metallization were then performed, followed by a plasma treatment in NH_3 ambient at 300 °C for 1 h.

The effective DOS distribution in the device channel was extracted from the subthreshold current-voltage (*I-V*) characteristics using the field-effect conductance (FEC) method.[19] The method was originally proposed by Suzuki *et al.* for amorphous silicon films.[20] Later Fortunato and Migliorato applied the method to poly-Si films.[21] This method assumes that spatial distribution of the defect states along the channel is uniform, which is acceptable when the grain size of poly-Si film is small. The DOS at a given energy level inside the band gap can be expressed as

$$\mathrm{DOS}(E_F+\psi_s)=\frac{\varepsilon_{\mathrm{Si}}}{2q}\frac{\partial^2}{\partial\psi_s^2}\left(\left.\frac{d\psi}{dx}\right|_{x=0}\right)^2. \qquad (1)$$

In Eq. (1), E_F, ψ_s, and $\varepsilon_{\mathrm{Si}}$ represent Fermi energy, surface band bending at the channel/gate-oxide interface, and dielectric constant of the silicon, respectively. In this work, incremental method[22] is employed to construct the relationship between the measured current-voltage characteristics and the surface band bending. The relationship can be obtained by the following equation:

$$\psi_{s,i+1}=\psi_{s,i}+\frac{I_{D,i+1}-I_{D,i}}{I_{D,\mathrm{flatband}}}\frac{d}{t_{0x}}\frac{\varepsilon_{0x}}{\varepsilon_{\mathrm{Si}}}\frac{V_{G,i}-V_{FB}-\psi_{S,i}}{\exp(q\psi_{\mathrm{Si}}/KT)-1}, \qquad (2)$$

where d represents the thickness of the poly-Si channel. Using the initial condition (i.e., $\psi_{S,i=0}=0$) and the known current-voltage ($I_{D,i}$ and $V_{G,i}$) relationship, we can calculate the corresponding $\psi_{S,i}$ for a specific $V_{G,i}$. The DOS at a given energy level can then be calculated using Eq. (1). Note that only DOS distribution of the energy level above the Fermi energy ($E > E_F$) can be extracted because *n*-type TFTs are used in this work.

RESULTS AND DISCUSSION

Owing to the nature that hot-carrier degradation is usually occurred at some portions of channel, it is very difficult to observe the degradation in subthreshold characteristics when the stress condition is moderate. Figure 2(a) shows subthreshold characteristics of a test transistor measured at drain voltage (V_D) of 0.1 V, before and after a moderate hot-carrier stressing, under gate voltage (V_G) of 6.5 V and V_D of 13 V for 1000 s. In this case, hot-carrier degradation cannot be observed by the subthreshold characteristics because the damaged region is very small compared with the whole channel. In our previous work,[23] the damaged region under such stress condition was found to be located near the drain side. As shown in Fig. 2(b), visibly retarded *I-V* characteristics of the monitor transistor near the drain (*D*-MT) directly and clearly reveal the existence of the damaged area near the drain side. The information from the *D*-MT can provide excellent sensitivity in characterizing the hot-carrier degradation.

For traditional testers, trying to resolve the difference in effective DOS distribution during hot-carrier degradation is more arduous, especially when the device is stressed under moderate or mild conditions. For example, Fig. 3 shows and compares the effective DOS distributions of the test transistor characterized in Fig. 2(a) before and after a moderate hot-carrier stressing of V_G/V_D=6.5 V/13 V for 1000 s. As can be seen in the figure, it is very difficult to distinguish the difference of effective DOS induced by the hot-carrier degradation. This is because only a small portion of the channel is damaged; the increased DOS will be averaged out during the extraction owing to the assumption that spatial distribution of defect states along the channel is uniform.

In contrast, since the hot-carrier degradation occurs near the drain side, the generated states can be treated as more uniformly distributed inside the *D*-MT. The DOS distributions calculated from the subthreshold characteristics of the *D*-MT shown in Fig. 2(b) before and after the hot-carrier stressing are shown in Figs. 4(a) and 4(b), respectively. It can

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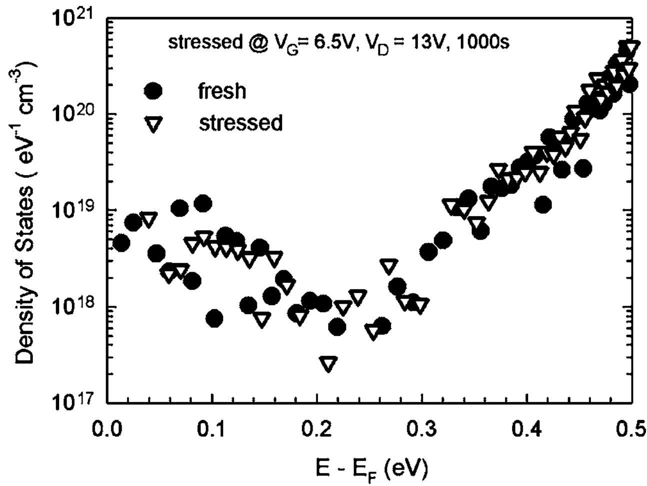
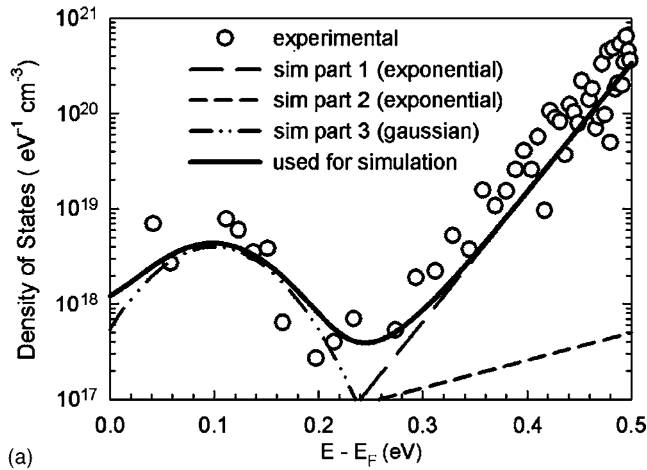


FIG. 3. Effective density-of-states distributions of TT before and after hot-carrier stressing under V_G/V_D=6.5 V/13 V for 1000 s.

be clearly and easily seen that the DOS increases after the stressing, especially in the range between 0.15 and 0.3 eV above the Fermi level.

This finding is very similar to the "type 2 of stress-created defects" proposed by Hack *et al.*[24] They proposed that two types of defect are generated during the hot-carrier stressing. "type 1" defects are generated when devices are stressed under linear conditions ($V_G > V_D$) and can be modeled as an increase in DOS near the midgap. Type 2 defects, which are similar to what we found in this study, are generated when devices are stressed in saturation ($V_G < V_D$) and can be modeled as an increase in DOS located 0.2–0.3 eV above the Fermi level. They found that by adding type 2 defects in the region within 1 μm of the drain, the simulated subthreshold characteristics can match well with their experimental results. However, their conclusion is based on the simulated results which assume specific location of generated defects. In contrast, we provide a direct evidence for the corresponding position within the band gap and the spatial location of such type of defect.



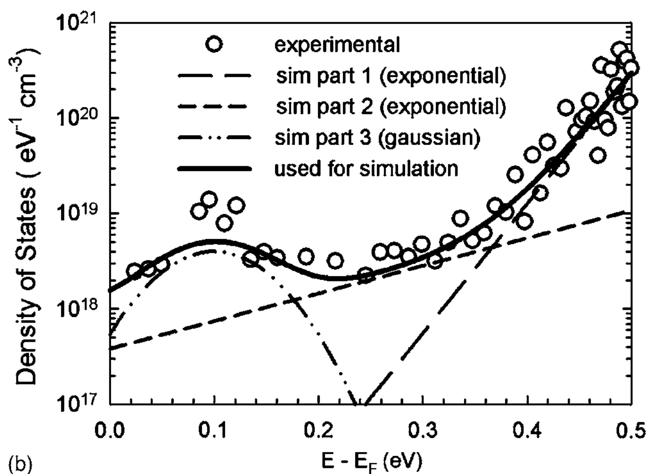


FIG. 4. Effective density-of-states distributions of *D*-MT (a) before and (b) after hot-carrier stressing under V_G/V_D=6.5 V/13 V for 1000 s.

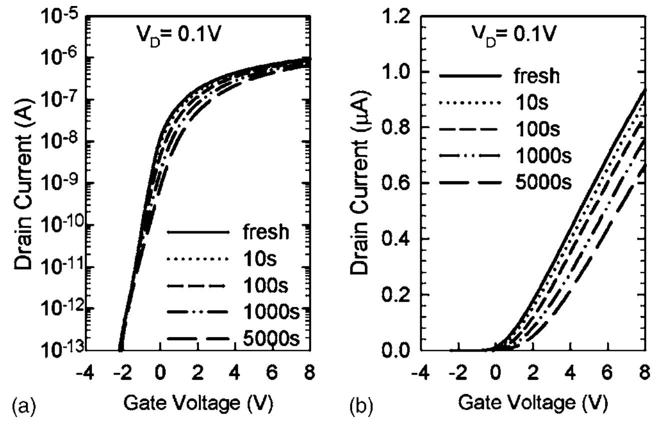


FIG. 5. Evolutions of subthreshold characteristics of *D*-MT in (a) logarithmic and (b) linear scales during hot-carrier stressing under V_G/V_D=6.5 V/13 V.

Temporal evolution of hot-carrier degradation at specific locations of the channel can also be addressed. Figure 5 depicts the evolution of subthreshold characteristics of *D*-MT during the hot-carrier stress of V_G=6.5 V and V_D=13 V. The evolution of subthreshold characteristics in both logarithmic and linear scales are in agreement with the simulated results reported by Dimitriadis *et al.*,[25] which suggest that this type of evolution is contributed by an increase in deep states. The evolution of extracted shift in subthreshold swing (ΔSS) for

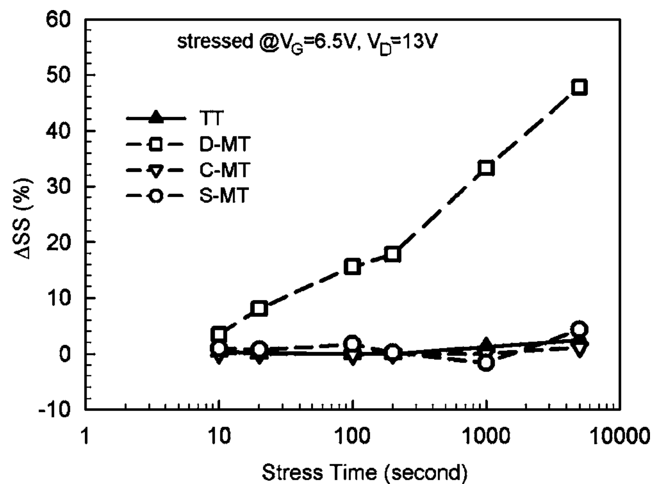


FIG. 6. Evolutions of degradation in subthreshold swing of the test structure during hot-carrier stressing under V_G/V_D=6.5 V/13 V.

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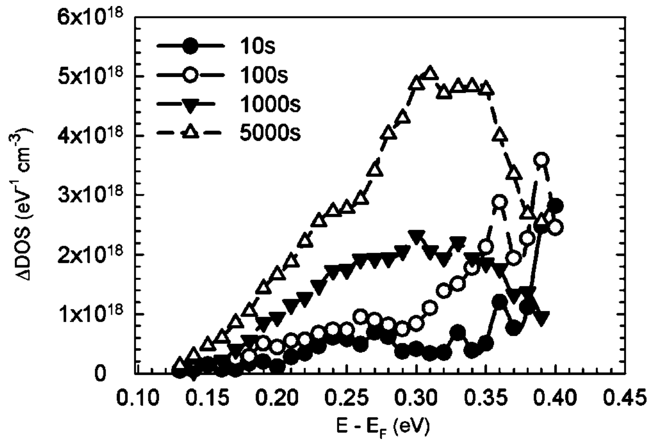

FIG. 7. Increase in density-of-states distributions of *D*-MT during hot-carrier stressing under V_G/V_D=6.5 V/13 V.

all TT and MTs is shown in Fig. 6. It can be seen that although TT's data show negligible subthreshold shift after the stressing, the *D*-MT shows unambiguous degradation at a very early stage, and the degradation increases monotonically with increasing stress time.

Using the aforementioned technique, the temporal evolution of DOS distribution of the degraded location, i.e., *D*-MT, during the hot-carrier stressing can also be observed. Increase in DOS distributions of *D*-MT during hot-carrier stressing is demonstrated in Fig. 7. It appears that during the hot-carrier stressing, the DOS near the drain side continuously increases, especially for the states located 0.2–0.4 eV above the Fermi level. The result demonstrates the capability of resolving the position of the generated states within the band gap.

Another tester was stressed under V_G/V_D=10 V/20 V for 1000 s. The subthreshold characteristics of all TT and MTs before and after the stressing were carefully measured. As shown in Figs. 8(a)–8(d), the degradation in all transistors can be easily observed. Although the degradation can be observed on TT, MTs' data provide a clearer picture, including not only better sensitivity enhancement but also the spatial location of two different types of degradation which occur simultaneously. The degradation of the test transistor can be expressed as the combination of parallel shift in S-MT and degradations of subthreshold swing and on current in *D*-MT. The mechanism of each phenomenon has been introduced and discussed before.[23]

The DOS distributions for each MTs before and after the stressing are shown in Figs. 9(a)–9(c). The increase of DOS in Fig. 9(c) indicates that many defects are generated near the drain side during the stressing. Compared with the result of devices under minor stress conditions (shown in Fig. 4), it can be clearly seen that in addition to the increase between 0.15 and 0.3 eV above the Fermi level, significant increase

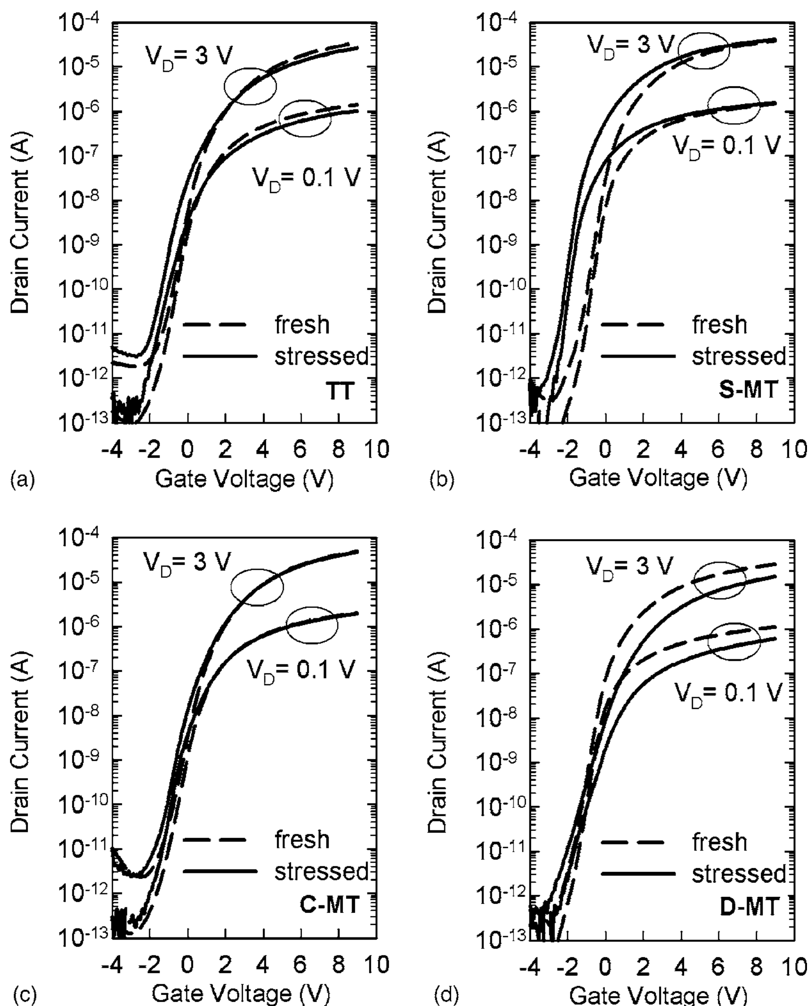

FIG. 8. Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) *D*-MT transistors in the test structure before and after the hot-carrier stressing under V_G/V_D=10 V/20 V for 1000 s.

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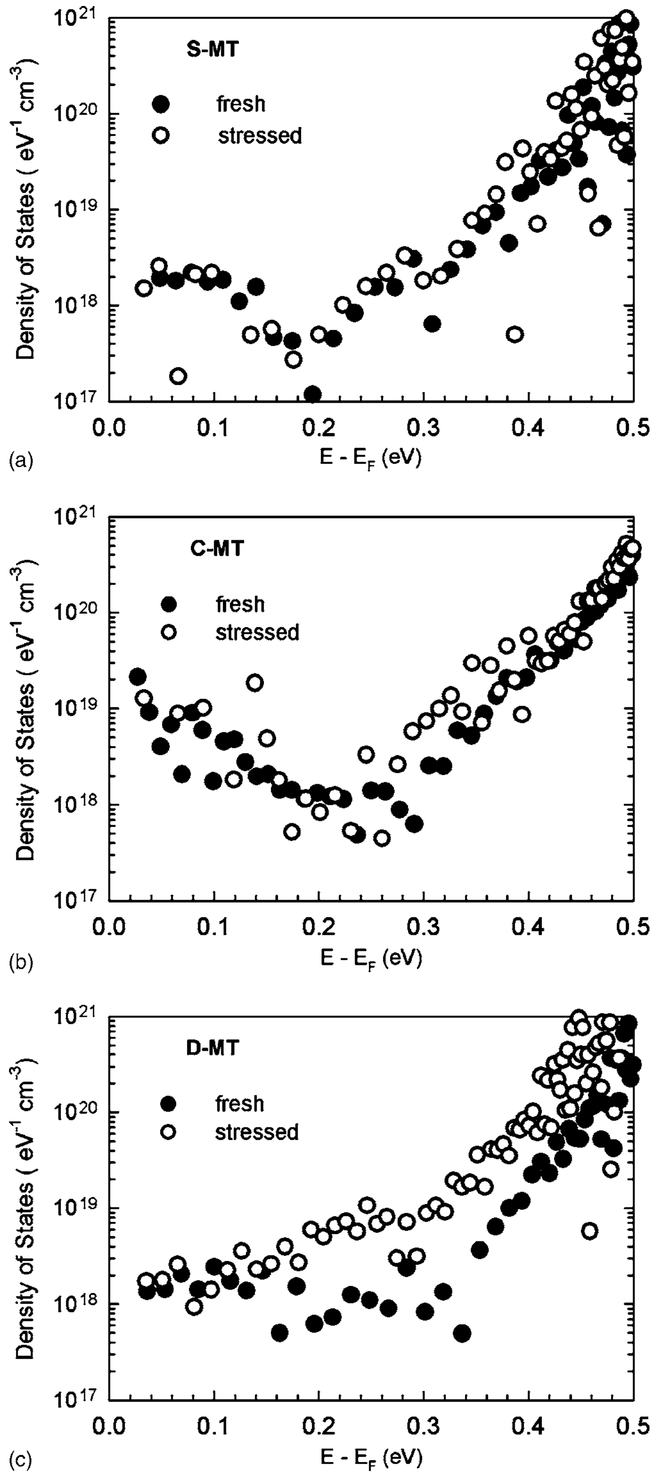

FIG. 9. Density-of-states distributions of (a) S-MT, (b) C-MT, and (c) *D*-MT before and after hot-carrier stressing under V_G/V_D=10 V/20 V for 1000 s.

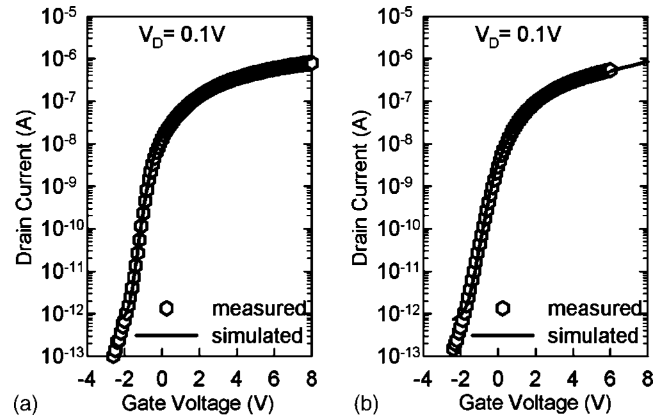

FIG. 10. Simulated subthreshold characteristics of *D*-MT (a) before and (b) after hot-carrier stressing under V_G/V_D=6.5 V/13 V for 1000 s.

of tail states is also observed. It is reasonable since the channel near the drain side is heavily damaged. The result also indicates that different types of defect are generated when the devices is stressed under minor or heavier conditions. In the experiments which employ traditional testers only, extrapolation from the result under heavier stress conditions is often used to predict the hot-carrier degradation under minor conditions. In this case, it appears that the direct observation using the MTs can provide more accurate information than the commonly used extrapolation technique. For the S-MT, because the creation of positive charge located in the oxide[23] affects the flatband voltage only, the DOS distribution in Fig. 9(a) remains unchanged.

The extracted DOS distributions were also used for device simulation to construct the *I*-*V* characteristics and validate the extracted results. One Gaussian and two exponential distributions were given to fit the DOS distribution used for simulation. For example, the extracted DOS distribution which was calculated from *D*-MT is shown by the circles in Fig. 4. Three curves, marked as "sim part (1–3)," represent the corresponding distribution. It can be seen that the summation of these three curves, which is represented by the solid line, matches well with the experimental results.

The DESSIS in ISE TCAD (Ref. 26) was used to obtain the simulated subthreshold characteristics. Figures 10(a) and 10(b) demonstrate the simulated *I*-*V* curves of *D*-MTs with the density-of-states distributions given from Figs. 4(a) and 4(b), respectively. The simulated data fit well with the measurement for both fresh and stressed samples. As mentioned before, the realistic density-of-states distributions after such nonuniform degradations are very difficult to obtain because of the limits of extraction technique. However, because the data extracted from monitor transistors can be employed to represent the localized defect distribution, the realistic distributions along the channel of TT can now be expressed be piecing together all MTs after the stressing. By giving the MTs' data shown in Figs. 9(a)–9(c), the channel of the TT can be split into three parts, as shown in Fig. 1. The DOS distribution of each part is then set using the data collected from the corresponding MT. Simulated subthreshold characteristics of the TT before and after the hot-carrier stressing using data collected from MTs are shown in Figs. 11(a) and 11(b), respectively.

CONCLUSIONS

In this work, a high-sensitivity TFT structure capable of spatially resolving hot-carrier degradation at a very early stage of stressing is employed to investigate the DOS characteristics. The nonuniform degradation along the channel could be clearly detected and characterized even under mild stress conditions. The effective DOS distributions in specific

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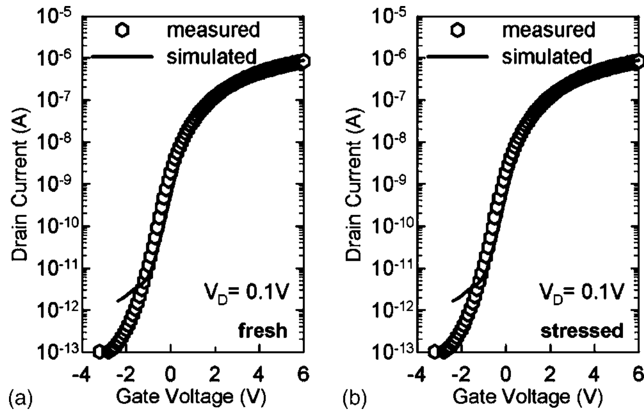

FIG. 11. Simulated subthreshold characteristics using data collected from MTs.

locations are extracted using field-effect conductance method. The effective DOS distributions reveal many useful and meaningful information not possible by traditional *I-V* characteristics. An increase in DOS is observed on certain position within the band gap when the device is stressed under mild conditions. Temporal evolution during the hot-carrier stressing is also characterized, and the monotonic increase in DOS distribution is observed. The extracted DOS distributions for both unstressed and stressed films are used to conduct a simulation for subthreshold characteristics of TFTs. The simulated *I-V* characteristics fitted well with the measured data. We have also simulated the subthreshold characteristics of the TTs before and after hot-carrier stressing using the DOS distributions extracted from all MTs. The combination of the proposed test structure and DOS extraction technique provides a powerful tool for resolving the nonuniform degradation of TFTs after hot-carrier stressing, which is difficult to achieve using traditional testers.

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