Effect of Channel-Width Widening on a Poly-Si Thin-Film Transistor Structure in the Linear Region

Kow-Ming Chang, *Member, IEEE*, and Gin-Ming Lin

***Abstract*—This is the first paper to discuss the ON-state drain–current of a special thin-film transistor structure with a wide channel width and a narrow source/drain width in the linear region. The experimental results indicate that when the channel width is wider than the source/drain width, the side-channel current effect is generated. This effect increases the ON-state drain–current due to the additional current-flow paths existing in the side-channel regions and low channel resistance. As the side-channel width increases, the ON-state drain–current initially increases and then gradually becomes independent of the side-channel width when the side-channel width is larger than the effective side-channel width, which depends on the channel width and is largely independent of the source/drain width. This paper also demonstrates that the ON-state drain–current gain is directly proportional to the channel length and the ratio of the channel length to the source/drain width and dependent on the side-channel width.**

***Index Terms*—Drain–current, poly-Si thin-film transistor (TFT), source/drain width, wide channel width.**

I. Introduction

LOW-TEMPERATURE polycrystalline-silicon thin-film transistors (TFTs) are one of the most promising technologies for the ultimate goal of building large-area electronic systems on glass substrates [1]. In flat-panel liquid-crystal, electroluminescence, and plasma displays, as well as other applications such as high-speed printers and page-width optical scanners, poly-Si TFTs can be utilized to integrate peripheral driver circuits on glass for system integration [2]. To integrate peripheral driving circuits on the same glass substrate, a large current drive and a high drain breakdown voltage are necessary for poly-Si TFT devices. Previous studies reported that use of a thin active-channel film is beneficial in obtaining a high current drive [3], [4]. However, the use of a thin active-channel layer typically results in poor source/drain contact and large parasitic series resistance. A thick source/drain region not only reduces the lateral electric field, thus maintaining the breakdown voltage [5], [6], but also reduces the source/drain series resistance [6]. Therefore, an ideal TFT device structure should consist of a thin active-channel region while maintaining a thick source/drain region.

To achieve this ideal TFT structure, we have proposed a novel four-mask step TFT structure with self-aligned raised source/drain (SARSD) [7]. In the SARSD TFT structure, a special structure was formed, which had a wide channel width and a narrow source/drain width. A high ON-state drain–current was obtained due to low channel resistance and additional current-flow paths existing in the side-channel regions [7]. Several models have been proposed to explain the behavior of the ON-state drain–currents of poly-Si TFTs and to simulate these ON-state drain–current values [8]–[11]. However, the drain–currents of these models were all derived from the assumption that the channel width is identical to the source/drain width. Simulating the ON-state drain–current of an SARSD TFT structure using these models is unreasonable [8]–[11]. Some studies have discussed the case of a narrow channel width [12]–[14]; however, no study has discussed the variations in the ON-state drain–current when the channel width is larger than the source/drain width. Therefore, before new physical models are proposed to elucidate and simulate the ON-state drain–current of a structure with a wide channel width and a narrow source/drain width, such as an SARSD TFT, the relationship among the ON-state drain–current of a structure with a wide channel width and narrow source/drain width, the channel width, the channel length, and the source/drain width must be defined clearly. This task is the aim of this paper, which examines the wide-channel-width effect in poly-Si TFTs. This paper will help us to further understand the behavior of the carrier transport in the channel region when the channel width is larger than the source/drain width and explain the increase of the ON-state current of a wide-channel-width TFT structure such as the SARSD TFT structure.

This paper uses a test structure with a wide channel width and a narrow source/drain width to analyze the influences of the channel width, the channel length, and the source/drain width on ON-state drain–current. Because the kink effect causes an anomalous current increase in the saturation region, this paper only focus on the ON-state drain–current in the linear region.

II. Device Fabrication

The fabrication processes for a tested n-channel poly-Si TFT with a wide channel width and narrow source/drain width were

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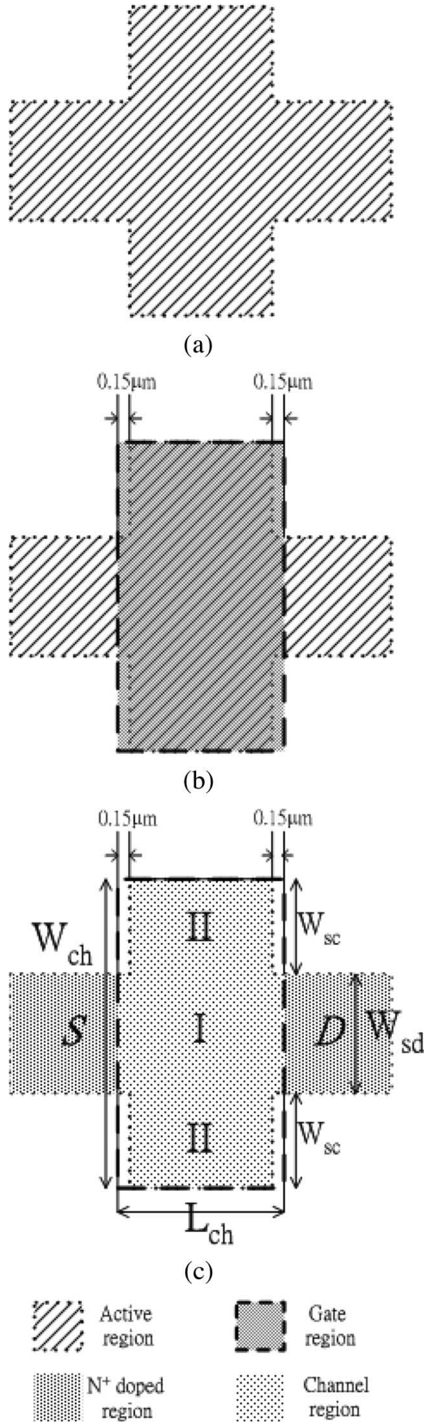


Fig. 1. Schematic top view of the major fabrication steps for the test TFTs.

as follows. A 50-nm-thick α-Si layer for the active region was deposited by a low-pressure chemical-vapor-deposition (LPCVD) system using SiH_4 at 550 °C on 500-nm thermal-oxidized silicon wafers. The active region was patterned by a G-line stepper and formed using reactive-ion etching [Fig. 1(a)]. The deposited α-Si film was then annealed at 600 °C for 24 h to become a poly-Si film. A 50-nm plasma-enhanced CVD (PECVD) gate-oxide layer was deposited at 350 °C. A 300-nm LPCVD poly-Si gate was then deposited. Because the G-line stepper system has a layer-to-layer misalignment of less than 0.15 μm, the gate region [Fig. 1(b)] has two overlapping regions that are 0.15 μm long and ensure that the source/drain width is narrower than the channel width. After the gate-region formation, the gate, source, and drain regions were formed by ion implantation of phosphorous (dose $= 5 \times 10^{15}$ cm^{-2} at 50 keV) and then activated at 600 °C for 24 h [Fig. 1(c)]. Following the source, drain, and gate activation, the 500-nm passivation oxide was deposited by PECVD. Contact holes were opened using wet etching of the passivation oxide layer. A layer of 600-nm-thick aluminum was then deposited by a thermal-coater system. After metal patterning, Al sintering was carried out at 400 °C for 30 min.

The channel region [Fig. 1(c)] is divided into one main-channel region (region I) and two side-channel regions (region II). The channel length and width are represented as $L_{\rm ch}$ and $W_{\rm ch}$, respectively. The channel width $(W_{\rm ch})$ is wider than the source/drain width $(W_{\rm sd})$, and this can be written as

$$W_{\rm ch} = W_{\rm mc} + 2W_{\rm sc} = W_{\rm sd} + 2W_{\rm sc} \tag{1}$$

where $W_{\rm sc}$ is the width of the side-channel region [Fig. 1(c), region II] in the test structure, and $W_{\rm mc}$ is the main-channel width that is equal to the source/drain width $(W_{\rm sd})$.

For comparison, the conventional poly-Si TFTs structure, in which the channel width is identical to the source/drain width, is also fabricated. The physical device parameters of the conventional structure are identical to those of the test structure.

III. Results and Discussion

A. *Simulation Results of the Test Structure* $(W_{\rm ch} > W_{\rm sd})$ *and the Conventional Structure* $(W_{\rm ch} = W_{\rm sd})$

To simulate the current flows of the test and the conventional structures, the 2-D numerical simulator MEDICI was used [15]. Fig. 2(a) shows the simulated current-flow lines of the conventional structure in the ON-state. The channel length and the channel width of the simulated conventional structure are 10 and 5 μm, respectively. Based on the simulation results [Fig. 2(a)], the simulated current-flow lines of the conventional structure are uniformly distributed in the channel region [Fig. 1(c), region I] and the source/drain region. However, for the test structures with a wide channel width [Fig. 2(b)–(d)], there are additional current-flow paths that differ from those of the conventional sample existing in the side-channel regions [Fig. 1(c), region II] of the test structure in the ON-state. Furthermore, comparing the simulation results of Fig. 2(b) with those of Fig. 2(c), the additional current flow is generated in the side-channel regions (region II), and the distribution width of the current-flow lines in the side-channel regions increases as the channel length increases ($L_{\rm ch} = 3$ μm to $L_{\rm ch} = 10$ μm). This finding implies that the current-flow distribution in the side-channel regions depends on the channel length. Comparing the simulation results of Fig. 2(c) with those of Fig. 2(d), the distribution and the effective distribution width of current-flow

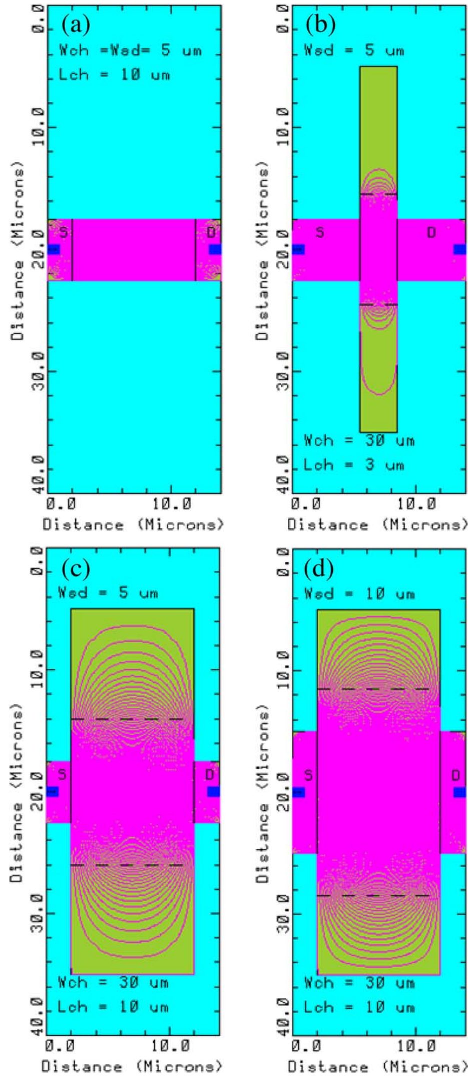


Fig. 2. Current-flow lines simulated by MEDICI in (a) conventional structure with $L_{\mathrm{ch}} = 10\ \mu$m and $W_{\mathrm{ch}} = W_{\mathrm{sd}} = 5\ \mu$m; (b) test structure with $L_{\mathrm{ch}} = 3\ \mu$m, $W_{\mathrm{sd}} = 5\ \mu$m, and $W_{\mathrm{ch}} = 30\ \mu$m; (c) test structure with $L_{\mathrm{ch}} = 10\ \mu$m, $W_{\mathrm{sd}} = 5\ \mu$m, and $W_{\mathrm{ch}} = 30\ \mu$m; (d) test structure with $L_{\mathrm{ch}} = 10\ \mu$m, $W_{\mathrm{sd}} = 10\ \mu$m, and $W_{\mathrm{ch}} = 30\ \mu$m.

lines of $W_{\mathrm{sd}} = 10\ \mu$m in region II are almost identical to those of $W_{\mathrm{sd}} = 5\ \mu$m, even when the source/drain width ($W_{\mathrm{sd}} = 5\ \mu$m to $W_{\mathrm{sd}} = 10\ \mu$m) is increased. This finding indicates that an increase in the source/drain width (or main-channel width) does not significantly alter the distribution of current-flow lines in region II.

B. Equivalent Circuit of the Channel Region of the Test Structure $(W_{\mathrm{ch}} > W_{\mathrm{sd}})$ in the Linear Region

This paper uses an equivalent circuit, as shown in Fig. 3, to further elucidate the additional current-flow paths of the test structure in the side-channel regions. In the side-channel regions (Fig. 3), the resistance of path 2 (R_{sc2}) is larger than that of path 1 (R_{sc1}) because path 2 is longer than path 1. Consequently, the current flow via path 2 must be less than the current flow via path 1. According to this equivalent circuit,

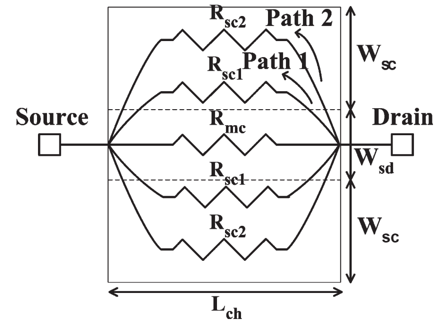


Fig. 3. Equivalent circuit of the channel region of the test structure ($R_{m,c}$ is the main-channel resistance; $R_{s,c}$ is the side-channel resistance).

the total channel resistance (R_{tot}) of the test structure can be written as

$$R_{\mathrm{tot}} = \frac{1}{\frac{1}{R_{\mathrm{mc}}} + \frac{2}{R_{\mathrm{sc1}}} + \frac{2}{R_{\mathrm{sc2}}} + \cdots} < R_{\mathrm{mc}} \tag{2}$$

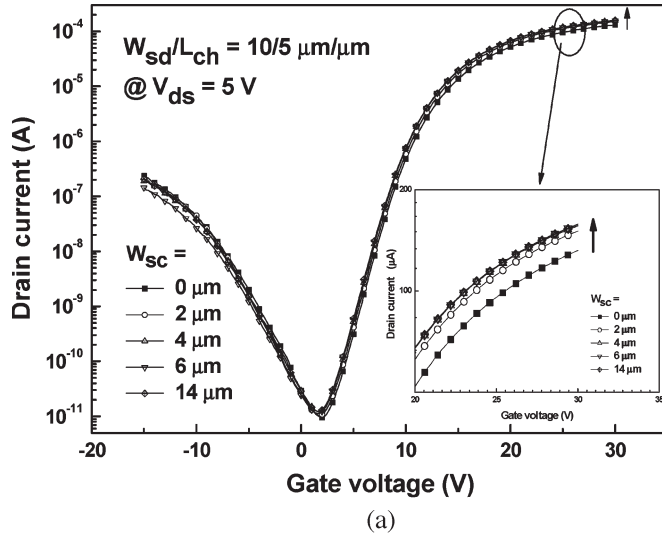
and

$$R_{\mathrm{mc}} = \frac{L_{\mathrm{ch}}}{W_{\mathrm{sd}} \mu_{\mathrm{eff}} C_{\mathrm{ox}} (V_{\mathrm{gs}} - V_{\mathrm{th}})} \tag{3}$$

where R_{mc} is the resistance of the main-channel region in the linear region, R_{mc} is the channel resistance of the conventional structure in the linear region [16], and C_{ox}, μ_{eff}, and V_{th} are the gate-dielectric-capacitance per unit area, effect mobility, and threshold voltage, respectively. According to (2), the total channel resistance (R_{tot}) of the test structure is smaller than that of the main-channel region (R_{mc}). In other words, the R_{tot} of the test structure is smaller than that of the conventional structure. Therefore, in the linear region, the ON-state drain–current of the test structure is higher than that of the conventional structure. As discussed, when the distance of current path is sufficiently long, the resistance of current path would be too large for the current flow. Thus, we suggest that in the linear region, the distribution of most current-flow paths should be restricted within a certain effective width in the side-channel region $(W_{\mathrm{sc,eff}})$, and the ON-state drain–current will become gradually independent of W_{sc} as W_{sc} increases. In other words, the ON-state drain–current of the test structure is saturated at a certain value when W_{sc} is sufficiently large.

C. Electrical Characteristics of the Test Structure $(W_{\mathrm{ch}} > W_{\mathrm{sd}})$ and the Conventional Structure $(W_{\mathrm{ch}} = W_{\mathrm{sd}})$ in the Linear Region

Figs. 4–6 present the experimental data for the test structure. In Fig. 4(a), the I_{ds}–V_{gs} transfer characteristics of the test structure with different side-channel widths are compared with those of the conventional sample. The ON-state drain–currents of the test structures are all higher than those of the conventional structure for different side-channel widths. Additionally, the ON-state drain–current of the test structure initially increases as the side-channel width (W_{sc}) increases and then becomes



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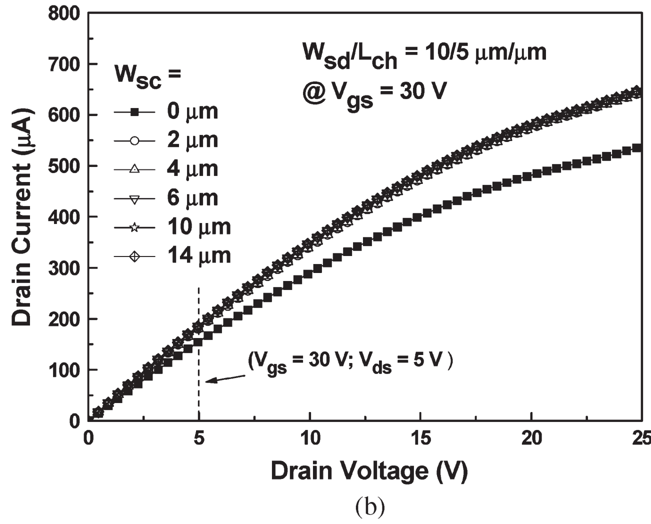
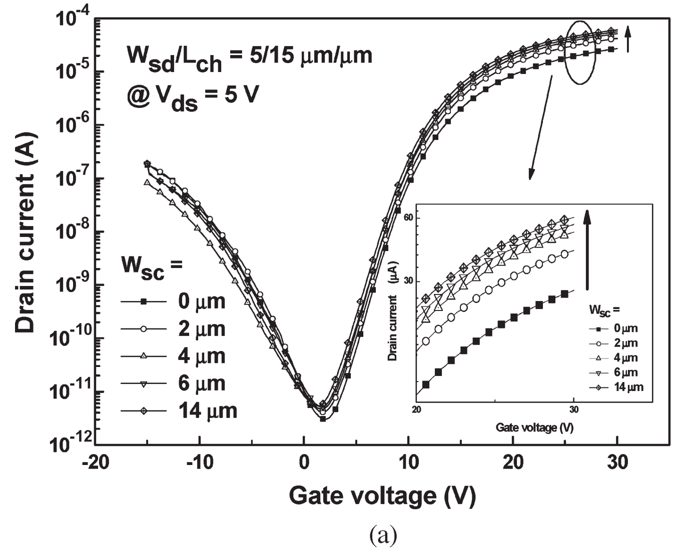


(b)

Fig. 4. (a) I_{ds}–V_{gs} transfer characteristics; (b) I_{ds}–V_{ds} output characteristics of the test structure with $L_{\mathrm{ch}}/W_{\mathrm{sd}} = 10\ \mu\mathrm{m}/5\ \mu\mathrm{m}$ with different side-channel widths (W_{sc}) compared with the conventional structure.



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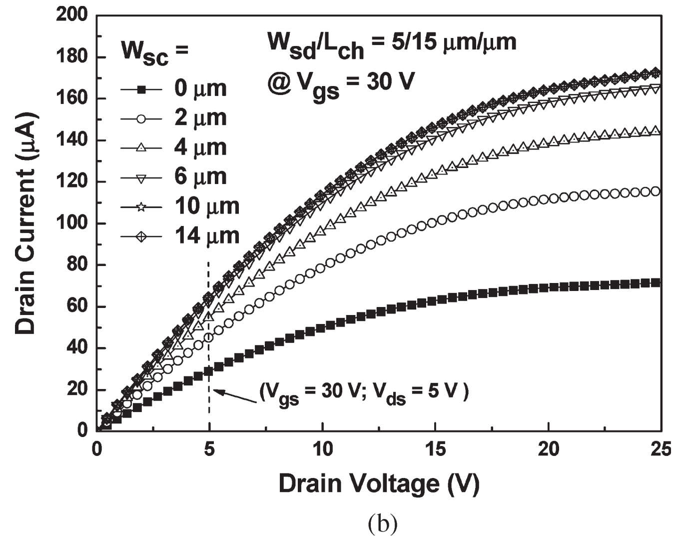


(b)

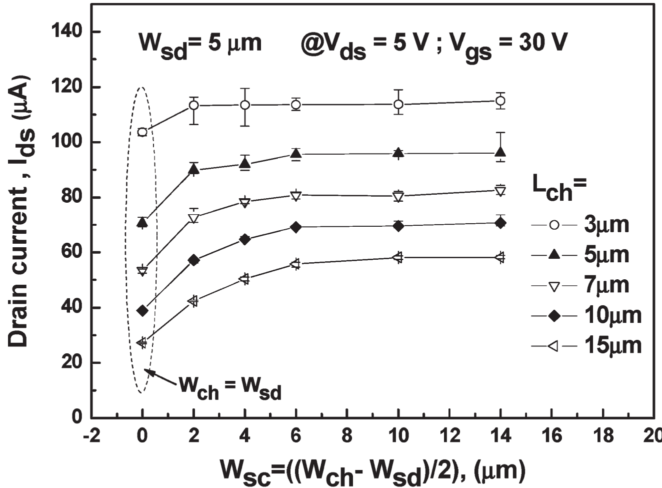
Fig. 5. (a) I_{ds}–V_{gs} transfer characteristics; (b) I_{ds}–V_{ds} output characteristics of the test structure of $L_{\mathrm{ch}}/W_{\mathrm{sd}} = 5\ \mu\mathrm{m}/15\ \mu\mathrm{m}$ with different side-channel widths (W_{sc}) compared with the conventional structure.

gradually independent of W_{sc} after reaching a certain W_{sc} value, even when the $W_{\mathrm{sd}}/L_{\mathrm{ch}}$ ratio of the test structure decreases from 10 μm/5 μm to 5 μm/15 μm [Fig. 5(a)]. These experimental results are consistent with the observations and suggestions in Section III-B. Figs. 4(b) and 5(b) show the output characteristics of the test structure with different side-channel widths. The ON-state drain–currents of the test structure are larger than those of the conventional structure in both linear and saturation regions. Additionally, according to the output characteristics [Figs. 4(b) and 5(b)] in the linear region, the channel resistance reduces as W_{sc} increases. Therefore, according to the experimental results (Figs. 4 and 5) and (2), we conclude that the main reason for a high ON-state drain–current of the test structure is low channel resistance.

Fig. 6 shows that the ON-state drain–current distributions of the test structure varied with the side-channel width for different channel lengths and the source/drain widths. There were 20 test TFTs measured for each condition. Based on the experimental results [Fig. 6(a) and (b)], the ON-state drain–current of the test structure initially increases as W_{sc} increases and then gradually becomes saturated when W_{sc} exceeds a threshold value. This special side-channel width is called the effective side-channel width ($W_{\mathrm{sc,eff}}$), and most current-flow lines are included within its corresponding effective channel width ($W_{\mathrm{ch,eff}}$), as obtained from (1). The effect in which a high ON-state drain–current is obtained when the channel width is larger than that of the source/drain is called the side-channel current effect (SCCE). Moreover, the value of the effective side-channel width ($W_{\mathrm{sc,eff}}$) decreases as the channel length increases, even when the source/drain width increases from 5 to 10 μm. This experimental finding is consistent with the simulation results (Fig. 2).

To analyze the increased ratio of the ON-state drain–current caused by the SCCE, the average values of the ON-state drain–current gain (A_i) versus the side-channel width are plotted [Fig. 7(a) and (b)]. The ON-state drain–current gain (A_i) is defined as

$$A_i \equiv \frac{I_{\mathrm{ds},t} - I_{\mathrm{ds},c}}{I_{\mathrm{ds},c}} \tag{4}$$



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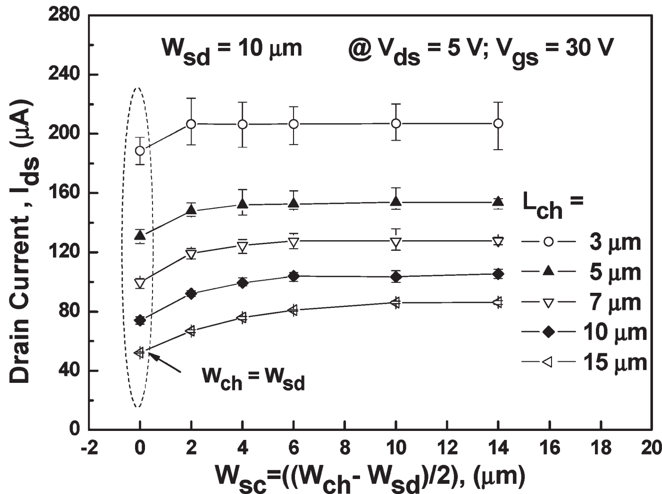
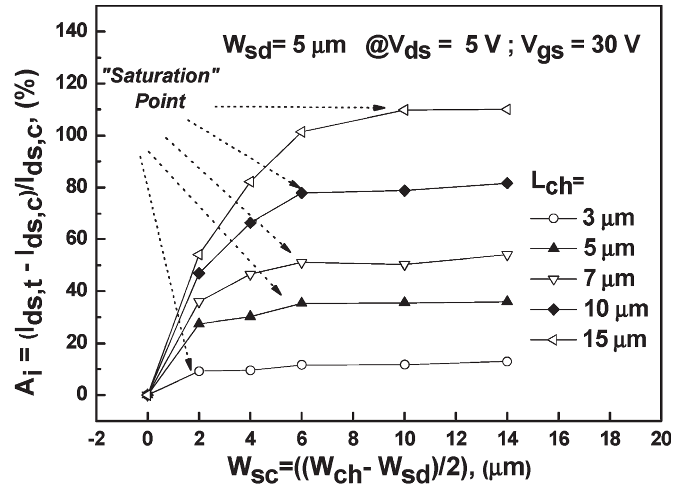


(b)

Fig. 6. Distributions of the ON-state drain–currents of the test structure with (a) $W_{\mathrm{sd}} = 5\ \mu$m; (b) $W_{\mathrm{sd}} = 10\ \mu$m as a function of the side-channel width W_{sc}.



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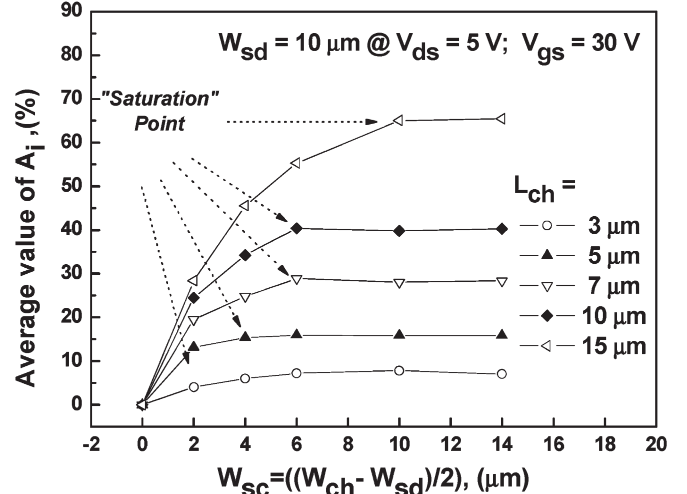


(b)

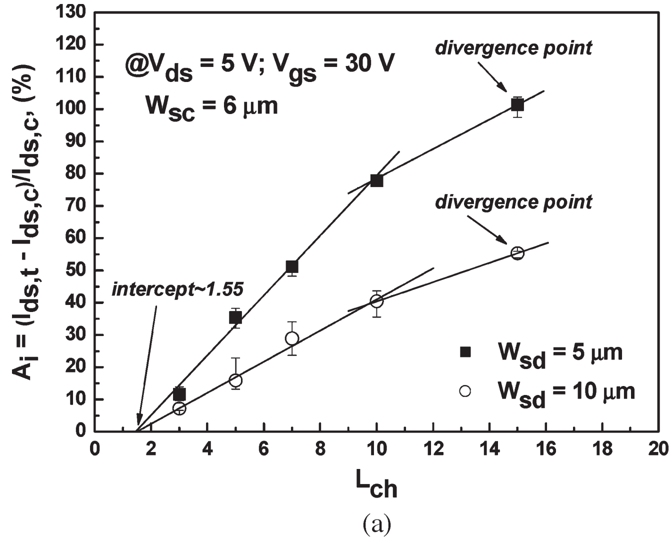
Fig. 7. Average values for the ON-state drain–current gain A_i of the test structure with (a) $W_{\mathrm{sd}} = 5\ \mu$m and (b) $W_{\mathrm{sd}} = 10\ \mu$m as a function of the side-channel width W_{sc}.

where $I_{\mathrm{ds},c}$ is the ON-state drain–current of the conventional structure, $I_{\mathrm{ds},t}$ is the ON-state drain–current of the test structure with different side-channel widths, and $(I_{\mathrm{ds},t} - I_{\mathrm{ds},c})$ is the net value of the ON-state drain–current flow through region II.

Based on the experimental results [Fig. 7(a) and (b)], the average ON-state drain–current gain (A_i) of the test structure increases as the channel length increases. Additionally, for the same channel length (such as $L_{\mathrm{ch}} = 15\ \mu$m), the effective side-channel widths $(W_{\mathrm{sc,eff}})$ of $W_{\mathrm{sd}} = 5\ \mu$m and $W_{\mathrm{sd}} = 10\ \mu$m are approximately the same. These experimental results are consistent with the simulation results [Fig. 2(b)–(d)]. In other words, the increase in the source/drain width (or main-channel width) does not significantly increase the distributions of current-flow lines in region II. However, the reduction of the W_{sd} from 10 to 5 μm increases the average value of A_i. Therefore, we conclude that the effective side-channel width $(W_{\mathrm{sc,eff}})$ is dependent on the channel length (L_{ch}) and independent of the source/drain width (W_{sd}), and the SCCE is dependent on the side-channel width, the channel length, and the source/drain width.

D. Relationship Among the ON*-State Drain–Current or the* ON*-State Drain–Current Gain and the Channel Length, the Side-Channel Width, and the Source/Drain Width in the Linear Region*

To investigate the relationship among the ON-state drain–current gain (A_i), the channel length, the side-channel width, and the source/drain width, this paper analyzes the distributions of the ON-state drain–current gain (A_i) against L_{ch} and the $L_{\mathrm{ch}}/W_{\mathrm{sd}}$ ratio with different channel widths and the side-channel widths (Figs. 8 and 9), respectively. The ON-state current gains A_i is directly proportional to L_{ch} for both $W_{\mathrm{sd}} = 5$ and 10 μm [Fig. 8(a) and (b)]. Moreover, the ON-state current gains A_i is directly proportional to the $L_{\mathrm{ch}}/W_{\mathrm{sd}}$ ratio for both $W_{\mathrm{sd}} = 5$ and 10 μm [Fig. 9(a) and (b)].



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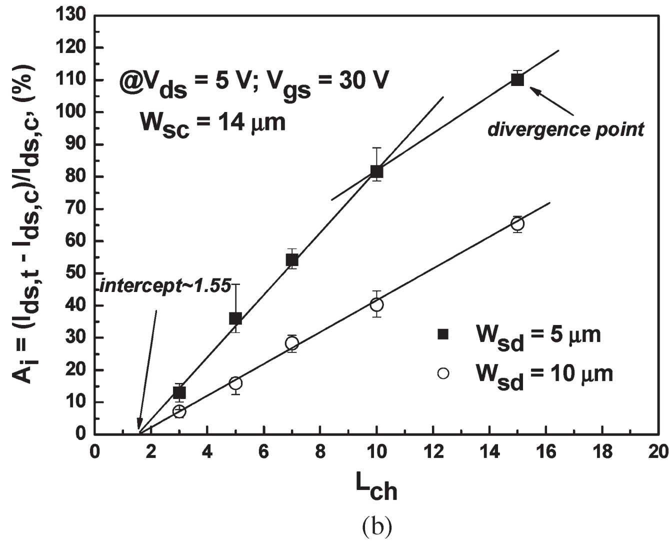
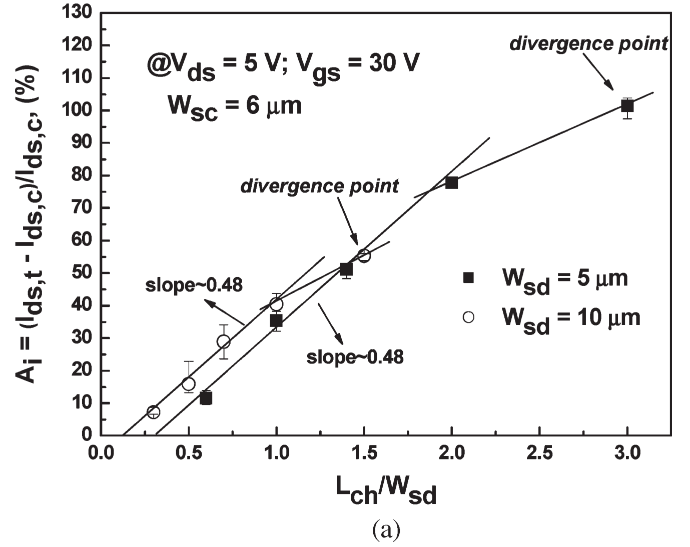


(b)

Fig. 8. Distributions of the ON-state drain–current gain A_i of the test structure with (a) $W_{\rm sc} = 6$ μm and (b) $W_{\rm sc} = 14$ μm, as compared with channel length $L_{\rm ch}$.



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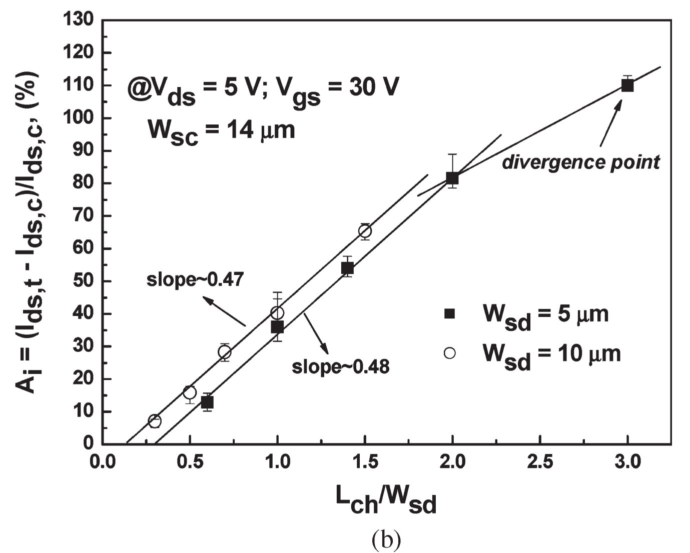

(b)

Fig. 9. Distributions of the ON-state drain–current gain A_i of the test structure with (a) $W_{\rm sc} = 6$ μm; (b) $W_{\rm sc} = 14$ μm compared with the ratio of the channel length to the source/drain width $L_{\rm ch}/W_{\rm sd}$.

Therefore, we conclude that the ON-state current gain is directly proportional to $L_{\rm ch}$ and the $L_{\rm ch}/W_{\rm sd}$ ratio and depends on $W_{\rm sc}$.

According to the experimental results (Figs. 8 and 9), the simple relationship among the ON-state drain–current gain (A_i), the channel length $L_{\rm ch}$, and the source/drain width $W_{\rm sd}$ can be written as

$$A_i \cong B\frac{L_{\rm ch} + C}{W_{\rm sd}} \tag{5}$$

where B and C are constants.

In the case of $W_{\rm sc} \geq W_{\rm sc.eff}$, B is approximately 0.48 based on the slopes of the auxiliary straight lines [Fig. 9(a) and (b)], and C is roughly -1.55 according to the intercepts of the auxiliary straight lines [Fig. 8(a) and (b)].

By combining (4) and (5), the maximum ON-state drain–current gain $(A_{i,\max})$ caused by the SCCE is obtained as follows:

$$A_{i,\max} \equiv \frac{I_{{\rm ds},t,\max} - I_{{\rm ds},c}}{I_{{\rm ds},c}} \cong 0.48\left(\frac{L_{\rm ch} - 1.55}{W_{\rm sd}}\right). \tag{6}$$

In the case of $W_{\rm sc} \geq W_{\rm sc.eff}$, if the channel length and the source/drain width are determined, the saturated or maximum ON-state drain–current of the test structure $(I_{{\rm ds},t,\max})$ can be written as

$$I_{{\rm ds},t,\max} \cong \left[1 + 0.48\left(\frac{L_{\rm ch} - 1.55}{W_{\rm sd}}\right)\right] I_{{\rm ds},c}. \tag{7}$$

Fig. 10 presents the experimental data and the calculated data. The calculated data roughly agrees with the experimental data for different source/drain widths and different applied drain biases ($V_{\rm ds} = 5$ V or 10 V) (Fig. 10).

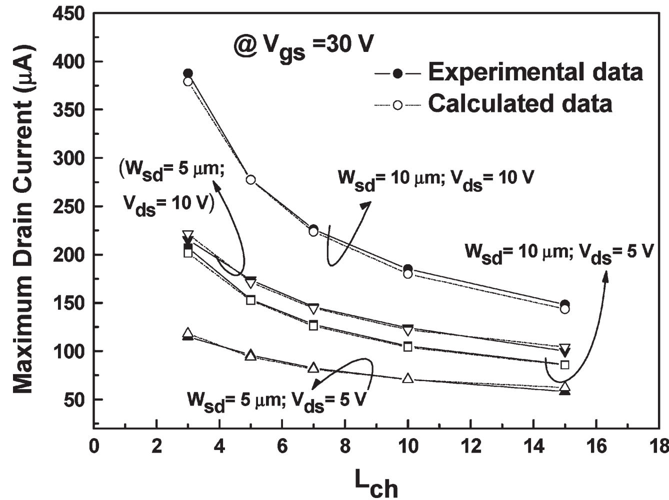

Fig. 10. Experimental and calculated maximum ON-state drain current for the test structure with different source/drain widths and different applied drain biases compared with the channel length L_{ch}, in which solid symbols represent the experimental data and empty symbols represent the calculated data obtained from (7).

However, for $L_{\mathrm{ch}} = 15\ \mu$m [Figs. 8(a) and 9(a)], the experimental data diverge from the auxiliary straight line because the side-channel width (W_{sc}) of the test structure of $L_{\mathrm{ch}} = 15\ \mu$m, which is 6 μm, is smaller than the effective side-channel width ($W_{\mathrm{sc,eff}}$) of the test structure of $L_{\mathrm{ch}} = 15\ \mu$m, which is approximately 10 μm (Fig. 7). Therefore, the ON-state drain–current gain (A_i) is limited by the side-channel width (W_{sc}), and the experimental data of $L_{\mathrm{ch}} = 15\ \mu$m cannot be fitted to the auxiliary straight line. However, for the case of $L_{\mathrm{ch}}/W_{\mathrm{sd}} = 15\ \mu\mathrm{m}/5\ \mu$m [Figs. 8(b) and 9(b)], the experimental data are not fitted to the auxiliary straight line, even though $W_{\mathrm{sc}}(= 14\ \mu\mathrm{m})$ is larger than $W_{\mathrm{sc,eff}}(\sim 10\ \mu\mathrm{m})$. It has been reported that the channel resistance is directly proportional to the $L_{\mathrm{ch}}/W_{\mathrm{sd}}$ ratio [16]. A large $L_{\mathrm{ch}}/W_{\mathrm{sd}}$ ratio indicates substantial channel resistance. Therefore, the main reason that the experimental data of $L_{\mathrm{ch}}/W_{\mathrm{sd}} = 15\ \mu\mathrm{m}/5\ \mu$m are not fitted to the auxiliary straight line [Figs. 8(b) and 9(b)] is that a large channel resistance dominates.

Therefore, when the channel width is larger than the source/drain width, the SCCE is generated, and this effect will cause an increase in the ON-state drain–current due to the additional current-flow paths existing in the side-channel regions and low channel resistance. As the side-channel width increases, the ON-state drain–current initially increases and then gradually becomes independent of the side-channel width when the side-channel width is larger than the effective side-channel width, which depends on the channel width and is independent of the source/drain width. This paper also demonstrates that the ON-state drain–current gain (A_i) is directly proportional to the channel length (L_{ch}) and the ratio of the channel length to the source/drain width ($L_{\mathrm{ch}}/W_{\mathrm{sd}}$) and dependent on the side-channel width. Moreover, when the ratio of the channel length to the source/drain width is excessively large, high channel resistance caused by a large ratio of the channel length to the source/drain width will suppress the SCCE and limit the increase in the ON-state drain–current gain.

IV. Conclusion

This paper focuses on the ON-state drain–current of a special structure with a wide channel width and a narrow source/drain width in the linear region. In the linear region, the ON-state drain–current of this special structure is larger than that of the conventional structure, in which the channel width is identical to the source/drain width, which is due to the additional current-flow paths and low channel resistance. The ON-state drain–current of this special structure is dependent on the channel length, the source/drain width, and the side-channel width. Moreover, a simple relationship among the ON-state drain–current, the source/drain width, and the channel length is identified. These experimental results will prove helpful to further understand the carrier-transport mechanisms in the ON-state when the channel width is larger than the source/drain width. These experimental results will also prove useful in the development of complete ON-state current modeling.

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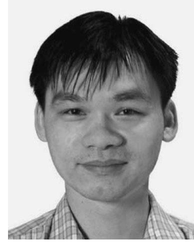

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