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The formation of nickel-silicon-nitride nanocrystals by sputtering a comixed target in the argon and nitrogen environment is proposed in this letter. High resolution transmission electron microscope analysis clearly shows the nanocrystals embedded in the silicon nitride and x-ray photoelectron spectroscopy also shows the chemical material analysis of nanocrystals. The memory window of nickel-silicon-nitride nanocrystals enough to define 1 and 0 states is obviously observed, and a good data retention characteristic to get up to 10 years is exhibited for the nonvolatile memory application. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2760144]

Nonvolatile nanocrystal memories have recently been one of the promising candidates to take the replace of conventional floating gate nonvolatile memory because the discrete traps as the charge storage media have effectively improved data retention under endurance test for the device scaling down.[1–3] In past years, the requirements of next-generation nonvolatile nanocrystal memory are the high density cells, low-power consumption, high-speed operation, and good reliability. Hence, the nonvolatile metal nanocrystal memory devices were extensively investigated over semiconducting nanocrystals because of several advantages, such as stronger coupling with the conduction channel, higher density of states (transport perspectives) than semiconductor (i.e., larger charge storage), and a wide range of available work functions (faster programming time and better data retention).[4,5] A nonvolatile memory device with metal nanocrystals has been formed by several experiment techniques, for instance, self-assembled of tungsten (W) nanocrystal by using thermal oxidation process,[6] separation of nickel (Ni) or gold (Au) nanocrystal by direct thermal annealing,[7,8] and formation of platinum (Pt) or cobalt (Co) nanocrystal by using molecular beam epitaxy.[9,10] Besides, the charge trapping layer also can contain some Si–N bonds which increase trapping states to improve charge storage capacity and program/erase efficiency for the nonvolatile metal nanocrystal memory devices, such as metal-oxide-nitride-oxide-semiconductor structure or silicon-germanium-nitride (SiGeN) structure.[11,12]

In this study, an ease process for nickel-silicon-nitride (NiSiN) nanocrystal formation will be proposed by sputtering a comixed target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and nitrogen (N_2) environment at room temperature. It was found that the NiSiN nanocrystals embedded in the silicon nitride (SiN_x) due to larger Gibbs free energy of chemical bond of Si–N than Ni–N at the room temperature.[13,14] In addition, high resolution transmission electron microscope (HRTEM) and x-ray photoelectron spectroscopy (XPS) were adopted for the microstructure analysis and the chemical material analysis of NiSiN nanocrystals. Furthermore, this fabrication technique of NiSiN nanocrystals can be compatible with current manufacture process of the integrated circuit manufacture.

This memory-cell structure in this letter was fabricated on a 4 in. *p*-type silicon (100) wafer. After a standard RCA process, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace. Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ comixed target in the Ar [24 SCCM (SCCM denotes cubic centimeter per minute at STP)] and N_2 (10 SCCM) environment at room temperature, and the dc sputtering power was set to 80 W. Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition system at 300 °C. Hence, these ternary nanocrystals could be found to precipitate and embed in SiN_x during the foregoing process. Al gate electrodes on back and front sides of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Electrical characteristics, including the capacitance-voltage (*C-V*) hysteresis, current density–voltage (*J-V*), and retention characteristics, were also performed. The *J-V* and *C-V* characteristics were measured by Keithley 4200 and HP4284 precision *LCR* meter with high frequency of 100 kHz.

Figure 1 exhibits a cross-sectional HRTEM image of the nitrogen incorporated $Ni_{0.3}Si_{0.7}$ film containing spherical and separated nanocrystals embedded in the SiN_x matrix. It is found that the thickness of tunnel oxide is larger than 3 nm due to the contribution of SiN_x matrix by HRTEM analysis. This SiN_x matrix can be used to improve charge storage ability for nonvolatile memory application.[12] Moreover, the av-

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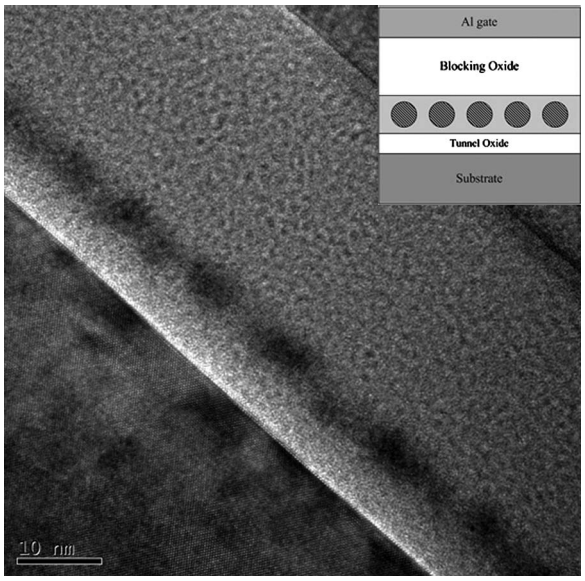

FIG. 1. Cross-sectional high resolution transmission electron microscope (HRTEM) analysis of nitrogen incorporated $Ni_{0.3}Si_{0.7}$ film between the tunnel oxide and the blocking oxide. The nanocrystal size and density are about 5–6 nm and 1.08×10^{12} cm^{-2}, respectively. The inset shows the memory structure diagram.

erage diameter of the nanocrystals is approximately 5–6 nm and the area density of the nanocrystals is estimated to be about 1.08×10^{12} cm^{-2} by HRTEM analysis.

To further invetigate the nanocrystals, we have performed XPS analysis by using an Al $K\alpha$(1486.6 eV) x-ray radiation to demonstrate the chemical composition of the nanocrystals. To correct the possible charging effect of the film, the binding energy was calibrated using the C 1*s* (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. Figure 2(a) shows the XPS Ni 2*p* core-level photoemission spectra which consist of two main peaks, $2p_{3/2}$(~855 eV) and $2p_{1/2}$(~873 eV), with two small satellite peaks. According to the values of other literature, Ni $2p_{3/2}$ binding energies are at 852.3 and 853.4 eV for metallic nickel (Ni–Ni) and Ni silicide (Ni–Si), respectively.[15] However, it cannot be found that the above-mentioned peak signals are observed at the Ni $2p_{3/2}$ peak by XPS analysis. Due to the strong electronegativity of nitrogen atom, it is reasonably assumed that the larger Ni $2p_{3/2}$ binding energy (~855 eV) of the nanocrystals can be assigned to Ni–Si–N ternary bond. This result is also supported by the XPS N 1*s* photoemission spectra, as shown in Fig. 2(b). By the fitting result of binding energy, it is found that the main peak can be compose into two components which center at 398.5 and 397 eV corresponding to Si–N bond and Ni–N bond, respectively.[16,17]

For chemical characteristics of Si–N and Ni–N, the enthalpies ($-\Delta H$) at room temperature are 470 and 70–85 kJ mol^{-1}, respectively.[13,14] Hence, because of the higher enthalpy of Si–N compared with Ni–N, the N radicals can interact with Si atom easier than Ni atom during the sputtering process. It can be considered that a nitridation reaction will induce self-assembled phenomenon of NiSiN nanocrystal, as shown in Fig. 1. In the previous research, Ni atom can diffuse in the SiN_x even at room temperature and formation of a NiSiN ternary solid solution.[18] Therefore, the nanocrystals are simple and uniform to be formed at low

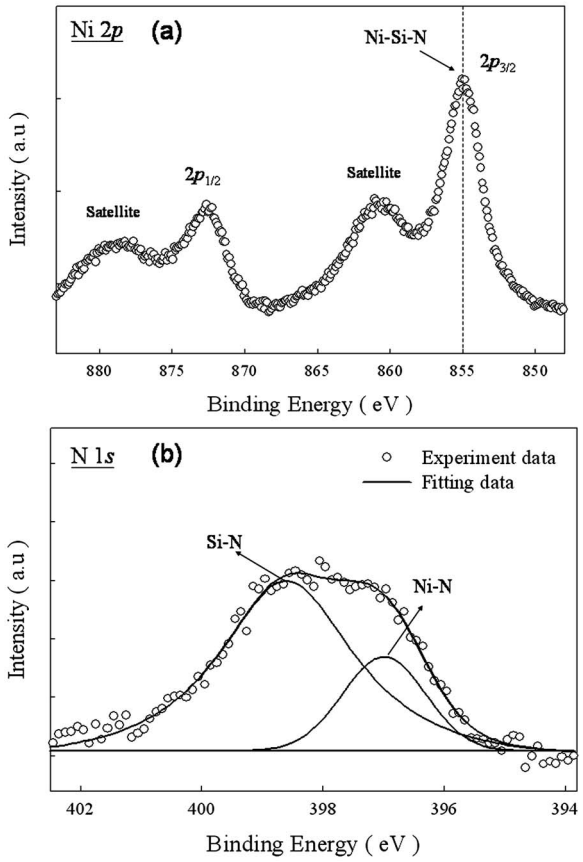

FIG. 2. (a) Ni 2*p* and (b) N 1*s* x-ray photoelectron spectroscopy (XPS) analyses of the nanocrystals. Empty circles and straight line indicate experimental and fitting results, respectively.

temperature by sputtering a comixed target in the Ar/N_2 environment.

The typical capacitance-voltage (*C-V*) hysteresis obtained with gate voltage from accumulation to inversion and in reverse is shown in Fig. 3. It is clearly observed that 1.5 and 3.5 V memory windows can be obtained under ±10 and ±12 V operations, respectively. The MOIOS structure with the NiSiN nanocrystals embedded in SiN_x matrix exhibits its clear counterclockwise hysteresis by a flatband voltage shift (V_{fb}), indicating the significant memory effect. We consider that the charges can be stored in both the NiSiN nano-

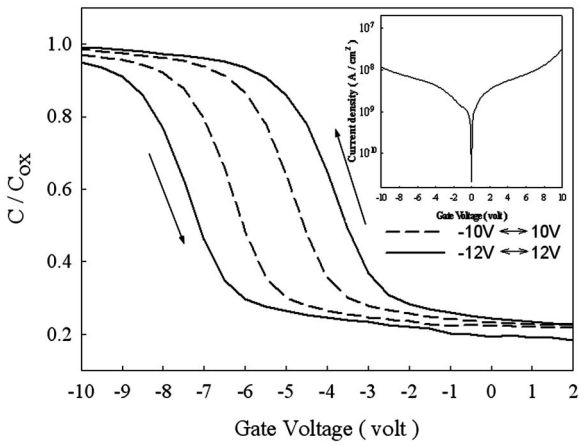

FIG. 3. Capacitance-voltage (*C-V*) hysteresis of the fabricated MOIOS structure with the NiSiN nanocrystals embedded in SiN_x matrix as a charge trapping layer. The inset shows current density–voltage (*J-V*) characteristics.

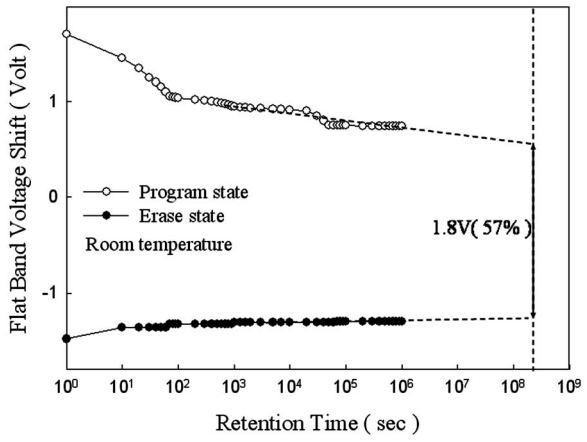

FIG. 4. Retention characteristics of the memory structure with NiSiN nanocrystals embedded in SiN_x matrix using a ±10 V gate voltage stress for 5 s at room temperature. The dotted line is the extrapolated value of retention data after 1000 s.

crystal and the SiN_x traps. Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate. Hence, this memory window of NiSiN nanocrystals embedded in SiN_x matrix is enough to be defined 1 and 0 states. In addition, current density–voltage (*J-V*) characteristics in the inset of Fig. 3 show the current density of the MOIOS structure by gate voltage sweeping from 0 to 10 V and 0 to −10 V. It is evident that the high quality of blocking oxide can avoid the stored carriers of charge trapping layer to leak into gate electrode.

Retention characteristics of the memory structure with NiSiN nanocrystals are illustrated in Fig. 4. The retention measurements are performed at room temperature by operating a ±10 V gate voltage stress for 5 s. The V_{fb} is obtained by comparing the *C-V* curves from a charged state and a quasineutral state. When carriers are stored in the nanocrystals, the stored charges will raise the nanocrystal potential energy and increase the probability of escaping from the nanocrystal to the silicon substrate.[19] Moreover, carriers trapped in the shallow traps are unstable and can easily leak back to the silicon substrate. It is found that the window of V_{fb} significantly reduces during the first 1000 s and then becomes more stable for long retention time. This result is consistent with partial carrier trapping in the shallow trap state of the SiN_x matrix around the nanocrystals. However, we use an extrapolation to give a long-term predictable result (dotted line) after 1000 s (stable region of retention) and extrapolate a memory window of 1.8 V (total charge hold ratio 57%) after 10 years. The majority carriers stored in the deep trapping states of NiSiN nanocrystal surrounding with SiN_x matrix exhibit good retention characteristics.

In conclusion, the nonvolatile memory structure of NiSiN nanocrystals embedded in SiN_x matrix was fabricated by sputtering a comixed target in the Ar/N_2 ambiance at room temperature. A larger memory window of 3.5 V was observed after ±12 V voltage sweep for nonvolatile memory application. In addition, the date retention of the nanocrystal memory device is also good enough to maintain for 10 years.

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[1]S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, Tech. Dig. - Int. Electron Devices Meet. **1995**, 521.
[2]Y. C. King, T. J. King, and C. Hu, Tech. Dig. - Int. Electron Devices Meet. **1998**, 115.
[3]J. D. Blauwe, IEEE Trans. Nanotechnol. **1**, 72 (2002).
[4]Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, IEEE Trans. Electron Devices **49**, 9 (2002).
[5]C. Lee, U. Ganguly, V. Narayanan, T. H. Hou, J. Kim, and E. C. Kan, IEEE Electron Device Lett. **26**, 12 (2005).
[6]T. C. Chang, P. T. Liu, S. T. Yan, and S. M. Sze, Electrochem. Solid-State Lett. **8**, G71 (2005).
[7]J. J. Lee, Y. Harada, J. W. Pyun, and D. L. Kwong, Appl. Phys. Lett. **86**, 103505 (2005).
[8]C. C. Wang, J. Y. Tseng, T. B. Wu, L. J. Wu, C. S. Liang, and J. M. Wu, J. Appl. Phys. **99**, 026102 (2006).
[9]Ch. Sargentis, K. Giannakopoulos, A. Travlos, and D. Tsamakis, J. Phys.: Conf. Ser. **10**, 53 (2005).
[10]D. Zhao, Y. Zhu, R. Li, and J. Liu, Solid-State Electron. **50**, 2 (2006).
[11]C. Lee, T. H. Hou, and E. C. Kan, IEEE Trans. Electron Devices **52**, 12 (2005).
[12]C. H. Tu, T. C. Chang, P. T. Liu, H. C. Liu, S. M. Sze, and C. Y. Chang, Appl. Phys. Lett. **89**, 162105 (2006).
[13]D. R. Lide, *CRC Handbook of Chemistry and Physics*, 81st ed. (CRC, Boca Raton, FL, 2000), Vol. 81, p. 5-3.
[14]E. K. Parks, G. C. Nieman, K. P. Kerns, and S. J. Riley, J. Chem. Phys. **108**, 3731 (1998).
[15]C. D. Wagner, W. M. Riggs, L. E. Davis, J. F. Moulder, and G. E. Muilenberg, *Handbook of X-Ray Photoelectron Spectroscopy* (Perkin-Elmer, Eden Prairie, MN, 1975), p. 298.
[16]I. Crupi, D. Corso, G. Ammendola, S. Lombardo, C. Gerardi, B. DeSalvo, G. Ghibaudo, E. Rimini, and M. Melanotte, IEEE Trans. Nanotechnol. **2**, 4 (2003).
[17]Y. Wang, Z. W. Fu, X. Li. Yue, and Q. Z. Qin, J. Electrochem. Soc. **151**, E162 (2004).
[18]L. Aballe, L. Gregoratti, A. Barinov, M. Kiskinovaa, T. Clausen, S. Gangopadhyay, and J. Falta, Appl. Phys. Lett. **84**, 5031 (2004).
[19]C. W. J. Beenakker, Phys. Rev. B **44**, 1646 (1991).