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The feasibility of using Cu/CuMg as a source/drain metal for the island-in amorphous silicon thin film transistors (*a*-Si:H TFTs) has been investigated. The issue of adhesion between the Cu film and n^+-a-Si layer has been overcome by introducing the Cu/CuMg alloy. Furthermore, the suppression of Schottky leakage current in metal/*a*-Si:H structure was also observed in the island-in *a*-Si:H TFT. The island-in *a*-Si:H TFT exhibited the mobility of 0.52 cm^2/V s, the subthreshold slope of 0.78 V/decade, and the V_{th} of 3.02 V. The experimental result also showed superior performance of the *a*-Si:H TFT with minimal loss of critical dimension and good thermal stability. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2767147]

Amorphous silicon thin film transistors (*a*-Si:H TFTs) have been widely used as switching devices in active matrix liquid crystal displays (AM LCDs). The *a*-Si:H TFT is particularly advantageous to the production of large flat panel displays and facilitates mass production.[1,2] Because *a*-Si:H is a photosensitive material, the main objectives for flat panel display application are to enhance the field effect mobility and to reduce the off-state leakage current under backlight llumination.[3] The off-state leakage current under light illumination is, in particular, a serious problem in the projection and/or multimedia displays that require high intensity backlight illumination. In order to reduce the parasitic capacitance between the gate and source/drain electrodes, a self-aligned *a*-Si:H TFT structure has been proposed. However, the higher off-state leakage current under light illumination compared to a conventional TFT has been observed.[4] Moreover, to improve the motion blur of thin film transistor liquid crystal displays (TFT LCDs), the double frequency addressing has been proposed to improve the moving image quality. Unfortunately, the double rate operation also reduces the device charging time and therefore reduces the TFT-LCD brightness.[5,6] As a result, the reduction of off-state photoleakage current in *a*-Si:H TFT is very important for a high quality TFT-LCD technology.

The most widely adopted method to lower the off-state photoleakage current is to reduce the thickness of undoped *a*-Si:H layer. However, the reduced undoped *a*-Si:H thickness would decrease the production yield of large size TFT-LCDs and also decrease the field effect mobility of the TFT devices.[7] The off-state dark leakage current of *a*-Si:H TFT mainly originates from the photoinduced hole current at the interface between *a*-Si:H and gate SiN layers. In contrast, electrons are the majority carriers of off-state current for the *a*-Si:H TFT under light illumination, since electron mobility is much higher than that of hole.[8] Akiyama *et al.* have proposed a light-shield (island-in) structure, which has the *a*-Si:H island completed inside the gate electrode edge, to reduce the light-induced photoleakage current.[9] However, for the light-shield structure fabricated with conventional process, a problem has arisen in that the Schottky contact between the metal and intrinsic *a*-Si:H layer, which is good for the hole current to flow through, resulted in a large off current at negative gate bias. Other methods are also proposed to reduce the Schottky leakage current, such as n^+ *a*-Si capping and sidewall *a*-Si:H oxidations.[10,11] However, an additional process was required to reduce Schottky leakage current. In this letter, the island-in *a*-Si:H TFTs with the CuMg alloy metal was used in the source/drain metal structure as good adhesion layer and provided good characteristic of the off-state leakage.

After a 300-nm-thick MoW gate electrode was deposited and patterned on the glass substrate, the *a*-Si:H TFT devices were fabricated by depositing a 300-nm-thick silicon nitride

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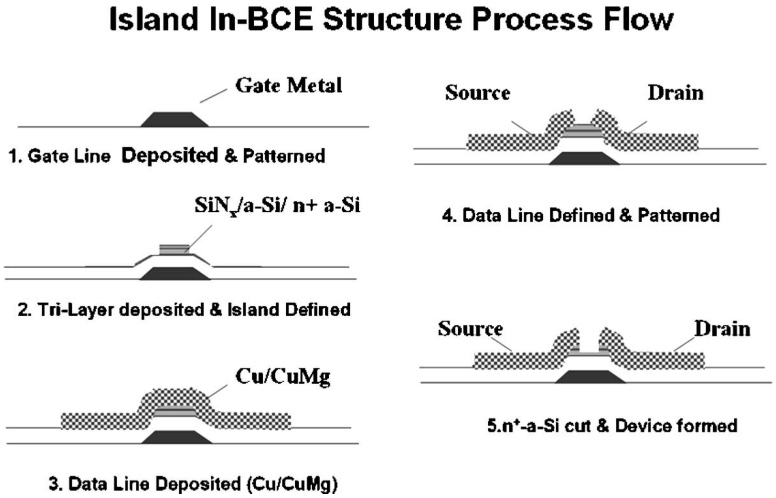

FIG. 1. Detailed process flow of the proposed island-in a-Si:H TFT with the Cu/CuMg source/drain and a back-channel-etched (BCE) inverted-staggered TFT structure.

(SiN_x), a 200-nm-thick a-Si:H active layer, and a 50-nm-thick n^+–a-Si:H layer subsequently on the MoW gate using plasma enhanced chemical vapor deposition method. After the island-in a-Si:H active islands were patterned, a thin CuMg alloy layer (50 nm) was deposited by dc magnetron sputtering a 99.99% purity level CuMg alloy target (4.5 at. % Mg) at room temperature. Afterward, a 300-nm-thick Cu layer was continuously deposited by sputtering on the CuMg alloy layer without breaking the vacuum. The Cu/CuMg metal was patterned for forming source/drain electrodes. Finally, the n^+–a-Si:H layer on the TFT channel region was etched with the source/drain pattern electrodes as the etching mask. The detail process flow is illustrated in Fig. 1. The sputtering conditions of Cu and CuMg alloys were as follows: the base pressure of the deposition chamber was 7.0×10^{-7} torr, the Ar pressure was 6 mtorr, the sputtering power was 1500 W, and the substrate temperature was at room temperature. The resistivity of the metal film was measured by the four-point probe. To investigate the adhesion ability between the Cu/CuMg alloy and trilayer, the 3M 610 tape test technology was performed. The Cu/CuMg alloy as the source/drain metal after wet etch process was also confirmed by the scanning electron microscopy (SEM) and optical microscopy (OM). The dimension of both the channel length and width was 16 and 40 μm for the TFT devices. The electrical measurement was carried out at a HP 4156C precision semiconductor parameter analyzer.

Table I shows the comparison of resistivity and adhesion between different Cu metals and trilayer by using the 3M 610 tape test method. Although the resistivity of the physical vapor deposited Cu film is only 2.6 $\mu\Omega$ cm, the 3M tape test failed due to the poor adhesion of the Cu film on the trilayer. Doping the Mg element into Cu could improve the adhesion and could pass the 3M tape test. The doping element increases, however, the alloy resistivity from 2.6 to 8.7 $\mu\Omega$ cm. As a result, the CuMg alloy film acting as a buffer layer could improve the adhesion between the Cu and trilayer. The source/drain metal structure of Cu/CuMg alloy has low resistivity compared with the pure Cu film and could pass the 3M tape test. By using the Cu/CuMg alloy structure, therefore, a low resistance metal line with a good adhesion can be obtained experimentally. The inset of Fig. 2 showed the OM picture of the a-Si:H TFT after wet etching with the Cu/CuMg alloy source/drain metal. The SEM picture also showed the cross section of the a-Si:H TFT with the Cu/CuMg alloy source/drain metal, as shown in Fig. 2. The conventional value of the taper angle used in the TFT LCD was from 45° to 70°. The Cu/CuMg as the source/drain metal has exhibited a much desired taper angle (~42°), beneficial for film step coverage and preventing pinhole formation through the passivation dielectric layer. The poor film step coverage and the pinhole formation through the passivation dielectric layer always resulted in the electrical degradation, such as larger top gate dielectric leakage and device characteristics failure for the double gate structure.[12–15] Thermal stability is another critical requirement for metal gate application. Since the metallic Cu has higher heat endurance than Al, the electrical characteristics degradation was not observed at 300 °C, 60 min in the vacuum chamber for the Cu/CuMg alloy as the source/drain metal on the trilayer. The island-in a-Si:H TFT with the Cu/CuMg alloy source/drain metal demonstrated the field effect mobility of 0.52 cm^2/V s

TABLE I. Adhesion and resistivity of metal on n^+–a-Si:H layer.

	Thickness (nm)	Resistivity ($\mu\Omega$ cm)	3M-610 tape test
Pure Cu	300	2.6	No pass
Cu Mg alloy	50	8.7	Pass
Cu/CuMg alloy	300/50	2.63	Pass

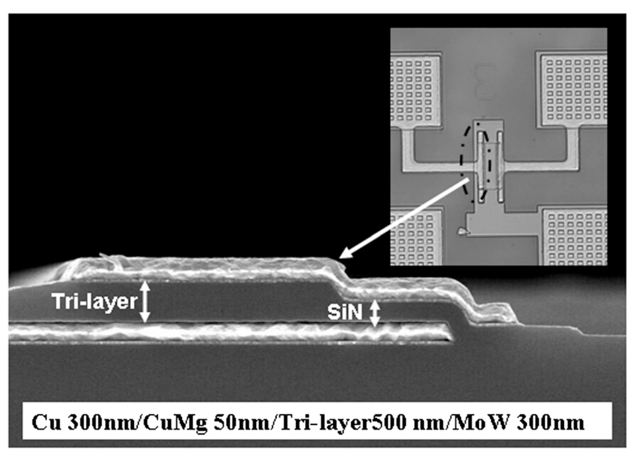

FIG. 2. SEM cross-sectional image of the island-in a-Si:H TFT with Cu/CuMg source/drain metal after a completed TFT manufacture process. The inset shows surface profile of OM picture.

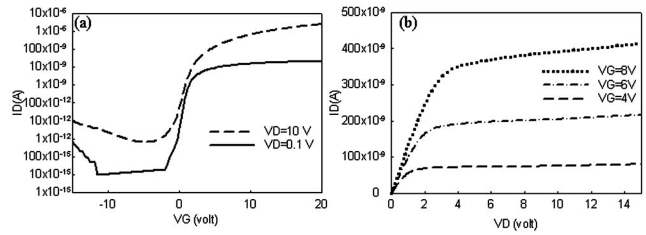

FIG. 3. (a) Transfer characteristics (I_D-V_G curve) of the island-in a-Si:H TFT with Cu/CuMg source/drain after the 300 °C, 60 min annealing process in the vacuum chamber. The channel length and width are 16 and 40 μm, respectively. (b) The output characteristics (I_D-V_D curve) of the island-in a-Si:H TFT with Cu/CuMg source/drain after the 300 °C, 60 min annealing process in the vacuum chamber.

(extracted from the linear I_D-V_G plot, where the V_{DS}=0.1 V), the subthreshold slope of 0.78 V/decade, the threshold voltage of 3.02 V (extracted from the linear I_D-V_G plot, where the V_{DS}=0.1 V), and the I_{on}/I_{off} ratio of 10^6 at V_{DS}=10 V, as shown in Fig. 3(a). Furthermore, the output characteristic of island-in a-Si:H TFT is also shown in Fig. 3(b), measured at the gate voltages sweeping from 4 to 8 V by a voltage step of 2 V. It is shown that no serious current crowding effect is observed in the Cu/CuMg alloy source/drain metal a-Si:H TFT device. It also means that the voltage applied on the TFT was not limited by the source/drain contacted resistance.

However, there was no serious Schottky leakage current observed, as shown in Fig. 3(a). This may be due to the formation of Ohmic contact between the a-Si island edge and Mg. According to previous report, the Ohmic behavior is observed for metals having work function (ϕ_m) lower than the electronic affinity (χ_s) of the a-Si:H film (χ_s $\sim$4.0±0.1 eV). Because the ϕ_m of Mg was 3.46 eV, it is easy for Mg to form the Ohmic contact with a-Si:H.[16] Therefore, the island-in a-Si:H TFT has shown non-Schottky leakage behavior.

The island-in a-Si:H TFT with the Cu/CuMg alloy as source/drain metal has been developed in this work. The CuMg alloy film acting as a buffer layer could improve the adhesion between the Cu and trilayer. In addition, the suppression of Schottky leakage current in metal/a-Si:H structure was observed with the use of CuMg as source/drain metal. The desired taper angle of the Cu/CuMg alloy electrode can be obtained by applying a wet etch process with ferric chloride base etchant. The Cu/CuMg electrode with ideal taper angle and hillock-free dielectric film formation was suitable for the application of double gate structure. Compared to the typical a-Si:H TFT, the Cu alloy source/drain a-Si:H TFT exhibited the same device performance.

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