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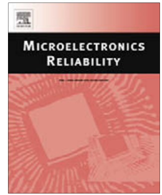

The impact of high-frequency characteristics induced by intrinsic parameter fluctuations in nano-MOSFET device and circuit

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ABSTRACT

This work estimates the influences of the intrinsic parameter fluctuations consisting of metal gate workfunction fluctuation (WKF), process variation effect (PVE) and random dopant fluctuation (RDF) on 16-nm-gate planar metal–oxide–semiconductor field effect transistors (MOSFETs) and circuits by using an experimentally validated three-dimensional device and coupled device–circuit simulations. The dominance fluctuation source in threshold voltage, gate capacitance, cut-off frequency, high-frequency gain, 3 dB bandwidth, unity-gain bandwidth, power, and the power-added efficiency has been found. Similar to the trend of the cut-off frequency, the PVE and RDF dominate both the device and circuits characteristic fluctuations due to the significant gate capacitance fluctuations and the WKF is less important at this simulation scenario.

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1. Introduction

Variabilities of performance and yield in nanoscale complementary metal oxide semiconductor (CMOS) devices are great of interest and become crucial for circuit design. The intrinsic device parameter fluctuations that result from process variation effect (PVE) [1], random discrete dopants fluctuation (RDF) [2–8], and other causes substantially impact device and circuit characteristics [9]. Although high-κ/metal-gate technology [10] is the key to reduce the intrinsic parameter fluctuations, the use of metal as a gate material introduces a new source of random variation, the workfunction fluctuation (WKF) [11,12]. The WKF-induced threshold voltage (V_{th}) fluctuation has been reported and the scope is limited to the transistors [13]. Additionally, the device and circuit performance may depend on different device characteristics. The identification of the dominant fluctuation source in the device and circuit characteristic fluctuations is urgent for the development of advanced nanoscale CMOS technologies. The impact of intrinsic parameter fluctuations on the high-frequency characteristics and power-efficiency is lacked. A comprehensive understanding of these fluctuations' effect on nanoscale CMOS transistors and circuits is urgent.

In this study, we extensively estimate the influences of the intrinsic parameter fluctuations (PVE, WKF, and RDF) on 16-nm-gate planar bulk MOSFETs' DC/AC and circuits' high-frequency characteristics. The results of our study show that for the device AC characteristics including gate capacitance and cut-off frequency fluctuations, the WKF is found to bring less impact on these two characteristics due to the screening effect of the inversion layer. Similar to the trend of the cut-off frequency, the PVE and RDF dominate the high-frequency property and the power-added efficiency of a common-source amplifier. The major fluctuation sources in nanoscale transistors and circuits have been presented herein and then verified by the related devices and circuits characteristics.

2. Simulation technique

The devices we investigated is the 16-nm-gate planar bulk MOSFETs (width: 16 nm) with amorphous-based TiN/HfSiON gate stacks and an EOT of 1.2 nm. The nominal channel doping concentrations are 1.48×10^{18} cm^{-3} and the V_{th} is calibrated. Fig. 1a–d illustrates the RDF-induced fluctuation, the simulation mainly follows our recent work [7–9], 758 dopants are randomly generated in a large cube of (80 nm)^3, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in Fig. 1a. Then the large cube is partitioned into 125 (16 nm)^3 sub-cubes.

The numbers of dopants vary from 0 to 14, and the average number is 6. These sub-cubes are mapped into the device channel for the 3D device simulation with discrete dopants, as shown in Fig. 1h. The PVE includes gate length deviation and line edge roughness, and we use V_{th} roll-off characteristics to estimate PVE-induced fluctuations, as shown in Fig. 1e [9]. For WKF, the device gate area is composed of a small number of grains, as shown in Fig. 1e. A Monte-Carlo approach is proposed for examining such effect, the gate area is first partitioned into several parts. Then, the workfunction of each partitioned area is randomly generated based on the properties of metal; the TiN is used in our work, as shown in

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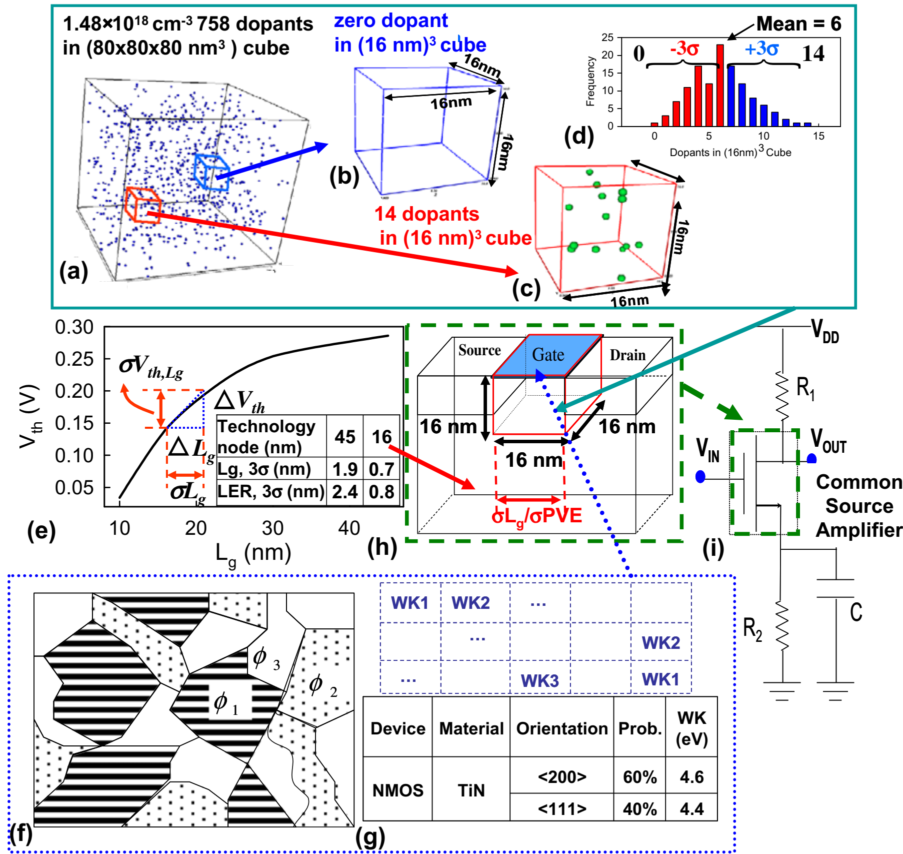

Device	Material	Orientation	Prob.	WK (eV)
NMOS	TiN	<200>	60%	4.6
		<111>	40%	4.4

Fig. 1. (a) 758 Dopants are randomly generated in a large cube of (80 nm)^3. The number of channel dopants in device may vary from 0 to 14, and the average number is 6 (b–d). (e) The V_{th} roll-off characteristics for estimating PVE. (f) The gate area is composed of a small number of grains, and the estimation of WKF according to the probability in (g). (h) The explored 16 nm planar MOSFETs for 3D simulation. (i) The tested common-source amplifier.

Fig. 1g. The effective device workfunction is the average of all parts and used for estimation of WKF-induced fluctuations. Fig. 1i is the explored common-source amplifier, in which a coupled device–circuit simulation approach [10] is employed to ensure the best accuracy. The physical models and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [9].

3. Results and discussion

Fig. 2 indicates the components of threshold voltage fluctuation (σV_{th}) for the examined planar bulk NMOSFETs. The total σV_{th}, $\sigma V_{th,total}$, are obtained from the statistical addition shown in below:

$$\sigma^2_{V_{th,total}} \approx \sigma^2_{V_{th,PVE}} + \sigma^2_{V_{th,WKF}} + \sigma^2_{V_{th,RDF}} \tag{1}$$

The $V_{th,PVE}$, $V_{th,WKF}$, and $V_{th,RDF}$ are the PVE-, WKF-, and RDF-induced σV_{th}, respectively. The results show that the RDF dominates the V_{th} fluctuation in NMOSFETs. Notably, the statistical addition of individual fluctuation sources herein, Eq. (1), simplifies the variability analysis of nano-devices and circuits, significantly [13]. The dominant source of fluctuation will not be significantly altered. Fig. 3 summarizes the gate capacitance fluctuations (σC_g) with 0, 0.5 V and 1.0 V gate bias. Different to the results of V_{th} fluctuation, the WKF brought less impact on gate capacitance fluctuation. At zero gate bias or negative gate bias, the accumulation layer screens the impact of WKF. Additionally, at low gate bias, the total capacitance decreases because of the increased depletion region. The associated value of C_g fluctuation is small. The capacitive response is then dominated by increment of inversion in the moderate

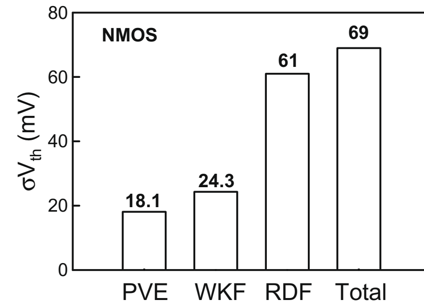

Fig. 2. The σV_{th} induced by PVE, WKF, and RDF for n-type planar NMOSFETs.

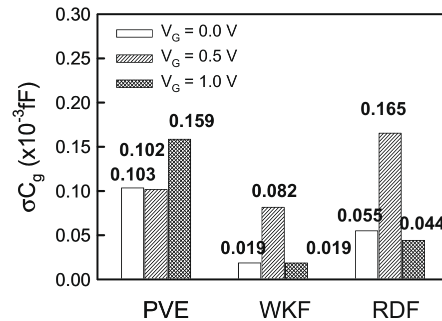

Fig. 3. The σC_g at V_G = 0, 0.5, and 1 V for n-type planar MOSFETs with PVE, WKF, and RDF.

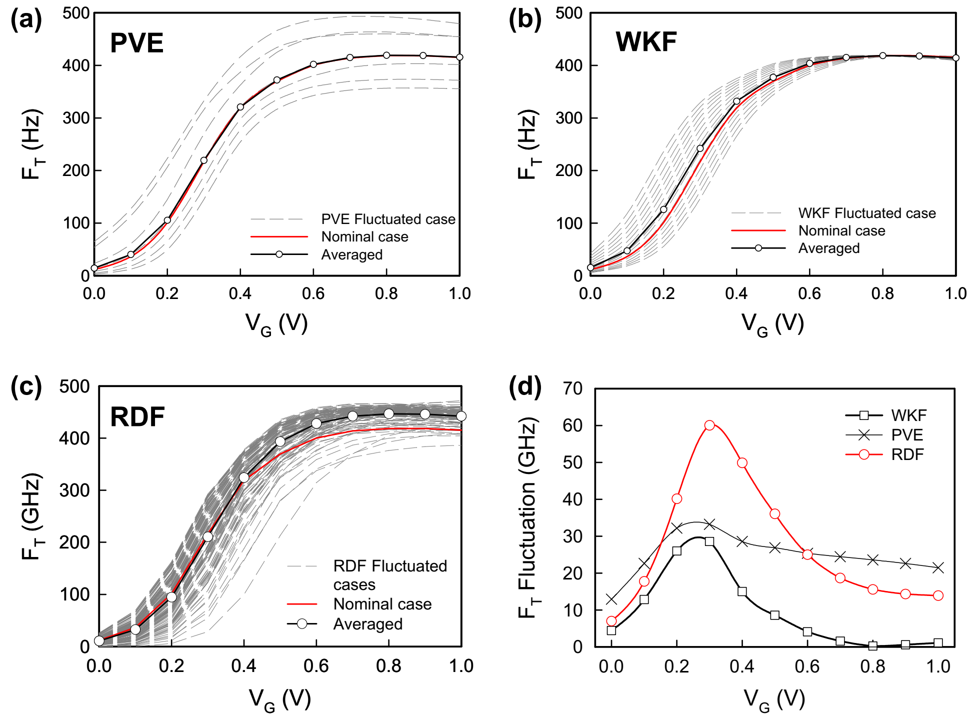

Fig. 4. The σF_T induced by: (a) PVE, (b) WKF, and (c) RDF. (d) The summarized σF_T for the studied planar MOSFETs.

inversion. The device characteristics are then impacted by intrinsic parameter induced electrostatic potentials. If the high V_G is achieved, the inversion layer is formed below the surface of the gate oxide and the total gate capacitance is mostly contributed by the gate oxide capacitance (C_{ox}). Therefore, the variation of capacitance now again becomes the variation of capacitance of gate oxide (C_{ox}). Under strong inversion, the gate capacitance is dominated by the inversion layer and a small change resulting from the WKF in the voltage across the MOS structure will induce a differential change in the inversion layer charge density.

The WKF is therefore bringing less impact on the gate capacitance fluctuation because the inversion charge responds to the change in capacitor voltage (i.e., the WKF is now screened by the inversion layer). Similarly, in RDF, the impact of the individual dopants induced electrostatic potential variation is screened by the inversion layer itself. However, the screening effect of inversion layer is weakened by discrete dopants positioned near the channel surface. Therefore, the gate capacitance fluctuation is still obviously fluctuated at high gate bias. Our preliminary results show that the PVE and RDF dominate the gate capacitance fluctuations at all gate bias conditions, respectively. The impact of the WKF on C_g is reduced significantly due to the screening effect. Notably, the PVE brings direct impact on gate length and therefore influences the gate capacitance. The PVE induced gate capacitance fluctuation is independent of screening effect and should be noticed when the transistor operated in high gate bias.

Fig. 4a–c shows the cut-off frequency ($F_T = v_{sat}/2\pi L_g = g_m/2\pi C_g$) and its fluctuation versus V_G, in which the solid line shows the nominal case with 1.48×10^{18} cm^{-3} channel doping, the dashed lines are fluctuated cases, and the symbol line shows averaged result. The g_m and v_{sat} are the transconductance and the saturation velocity of the transistors, respectively. WKF-induced F_T fluctuation diminished as the saturation of the carrier velocity occurs. However, the PVE-induced F_T fluctuation is still significant owing to the direct influence of gate length (L_g) on gate capacitance. As for RDF, the carrier-impurity scattering alters the saturation velocity, and therefore F_T fluctuation does not diminish in high-field region. Note that the nominal and the averaged values of F_T are similar to the results of WKF and PVE. However, in RDF, the deviation between the nominal and the averaged F_T increases as V_G increases due to the randomness of carrier-impurity scattering events and carrier velocity variations [14]. The intrinsic parameter induced F_T fluctuations are summarized in Fig. 4d, where the RDF and PVE are the two major factors. The RDF and PVE play the dominating factor in the F_T fluctuation. Notably, the impacts of RDF and WKF on F_T fluctuation are suppressed at higher V_G (>0.6 V) due to the screening effect. The obtained results are similar to the results as shown in Fig. 3, in which the WKF bring insignificant impact on C_g and F_T.

Fig. 5 presents the characteristics of the employed common-source power amplifier circuits. The nominal output power, the circuit gain, and the power-added-efficiency of the common-source power amplifier as a function of the input power are plotted, where P_{out} and P_{in} are output and input power, respectively. A sinusoid input wave with 0.5 V offset voltage is used as input signal. The de-

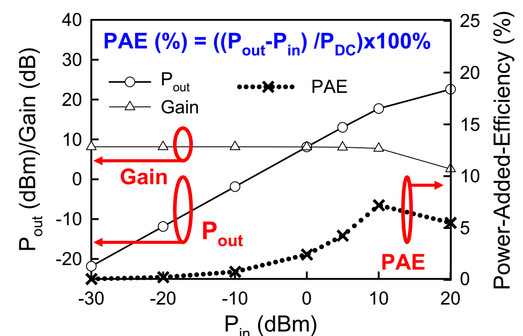

Fig. 5. Output power, circuit gain, and power-added-efficiency of the explored common-source power amplifier as a function of input power. The calculation of PAE follows the formula as shown in the inset.

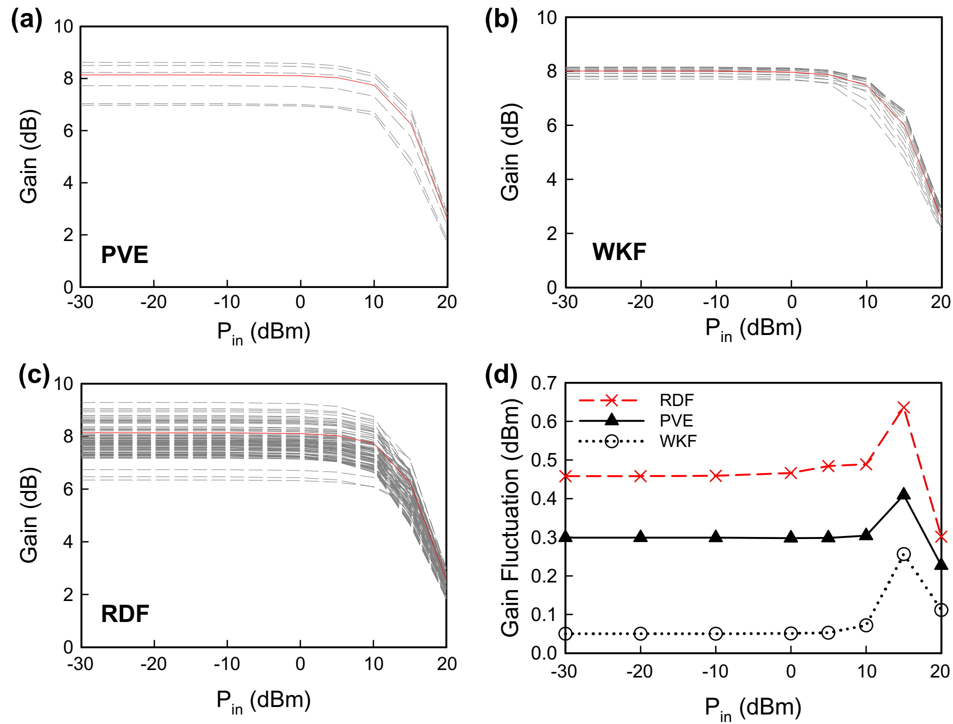

Fig. 6. The circuit gain characteristics of the planar MOSFETs power amplifier with: (a) PVE, (b) WKF, and (c) RDF fluctuations, respectively. (d) The summarized circuit fluctuations.

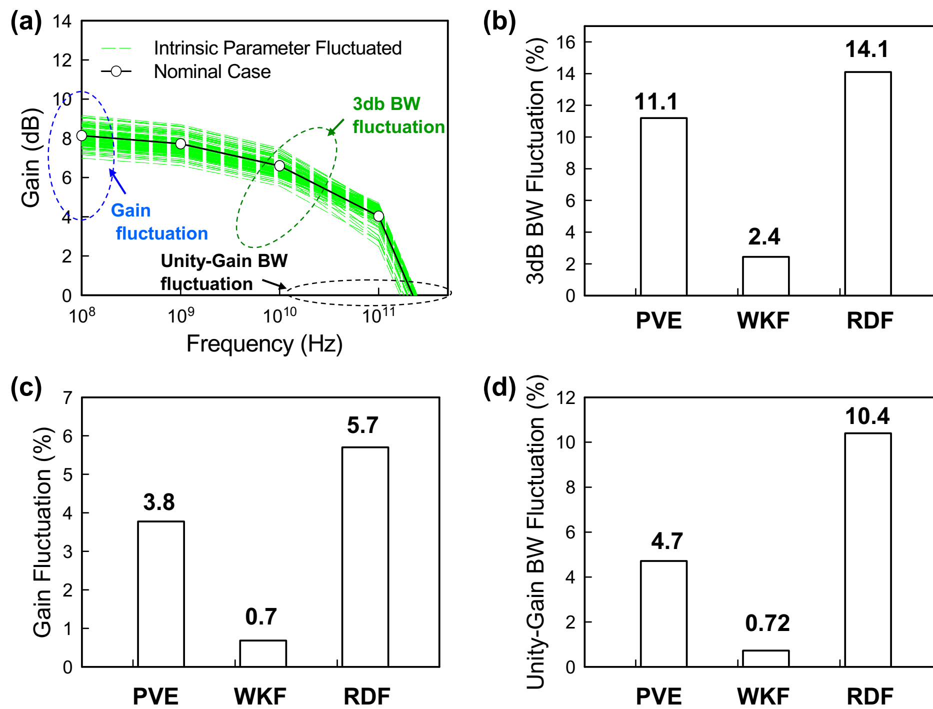

Fig. 7. (a) The frequency response of the planar MOSFETs common-source amplifiers, in which (b) 3 dB bandwidth, (c) gain, and (d) unity-gain bandwidth are extracted.

vice channel is continuously doped and the operation frequency is 10^8 Hz. Owing to the limitation of output signal swing, the nominal value of P_{out} is saturated after 10 dB m input power, which in turn decreases the gain of circuit. The gain fluctuations of the planar MOSFETs resulted from PVE, WKF, and RDF are then explored in Fig. 6a–c. Since the PVE and RDF dominate gate capacitance fluctuations due to significant affected the channel length and depletion region, the PVE and RDF play important roles in high-frequency characteristic fluctuation, as shown in Fig. 6d. Effects of WKF in high-frequency characteristics are negligible in this scenario. Addi-

tionally, the input signal is a sinusoid wave; therefore, the device may operate in different operational region if the amplitude of the sinusoid wave is large enough. The enlarged gain fluctuation with increasing input power is resulted from the larger portion of device operation in linear region. While the magnitude of input signal swing increases larger than 0.178 V (the input power is larger than 15 dB m), a part of device operation enters the cut-off region and therefore decreases the gain fluctuation. The high-frequency characteristic fluctuations are then investigated in Fig. 7a, where the fluctuation of the high-frequency circuit gain, the 3 dB bandwidth, and the unity-gain bandwidth are extracted, as shown in Fig. 7b–d, respectively. Similar to the result of Figs. 3 and 4, the RDF and PVE dominates the high-frequency characteristic fluctuations and WKF become marginal in this analyzing skeleton.

4. Conclusions

In this study, we have estimated the influences of the intrinsic parameter fluctuations in 16-nm planar MOSFETs and circuits. Our results have shown that the RDF dominates the device threshold voltage fluctuation. For gate capacitance and cut-off frequency fluctuation, due to the screen effect of the device inversion layer, the WKF can be neglected. For the high-frequency characteristics, the circuit gain, the power, and the power-added efficiency were explored. Similar to the trend of the device cut-off frequency, the PVE and RDF are dominated and the WKF shows less impact. We are currently working on studying the possible correlations between each fluctuation sources. The interaction of V_{th} change due to different sources may be important and need to be properly incorporated.

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