Design and Analysis of a Millimeter-Wave Direct Injection-Locked Frequency Divider With Large Frequency Locking Range

Chung-Yu Wu, *Fellow, IEEE*, and Chi-Yao Yu

***Abstract*—In this paper, direct injection-locked frequency dividers (ILFDs), which operate in the millimeter-wave (MMW) band, are analyzed. An analytically equivalent model of the direct ILFDs is developed, and important design guidelines for a large frequency locking range are obtained from it. These guidelines are: 1) maximize the quality factor of the passive load; 2) maintain low output amplitude; and 3) increase the dc overdrive voltage of the input device. A direct ILFD without varactors is designed and fabricated using a 0.13-μm bulk CMOS process to verify the developed model and design guidelines. A pMOS current source is used to restrict the output amplitude and to increase the dc overdrive voltage of the input device to achieve a large frequency locking range. The size of the input device is only 3.6 μm/0.12 μm and the measured frequency locking range is 13.6% at 70 GHz with a power consumption of 4.4 mW from a supply voltage of 1 V. In short, the proposed divider has the potential to be integrated into an MMW phase-locked loop system.**

***Index Terms*—Frequency locking range, injection-locked frequency divider (ILFD), millimeter-wave (MMW) integrated CMOS circuit, phase-locked loop (PLL), 0.13-μm bulk CMOS technology.**

I. Introduction

With RAPID advances in CMOS technology, the CMOS circuit operating in the millimeter-wave (MMW) band has attracted increasing interest and research [1]–[16]. Since frequencies around 60 GHz have been opened for unlicensed use in the U.S. and Japan, it seems possible that such circuits can be used in the front-end systems of gigabits/s point-to-point links, wireless local area networks, high data-rate wireless personal area networks, and radars.

In general, phase-locked loops (PLLs) are extensively used in CMOS RF front-end systems as frequency synthesizers or clock sources to generate local oscillating signals. In an MMW PLL, the main blocks with the highest operating frequency are typically the voltage-controlled oscillator (VCO) and the frequency divider. More specifically, the main design issues of an MMW VCO concern the oscillating frequency tuning range, phase noise, power consumption, and output power level [7]–[10]. Most of these degrade as the input capacitance of the next stage, which may be a frequency divider, increases. Therefore, the reduction of the input capacitance of the divider becomes very important as the operating frequency to the MMW band increases. In addition, the wide operating frequency range of the divider is also important in the MMW band in order to cover the inevitable shift of the center operating frequency caused by the process variations in the small values of integrated spiral inductance or parasitic capacitance. A small operating frequency range will severely reduce the reliability of the MMW PLL. Therefore, the main design challenge facing the MMW divider designers is to reduce input capacitance while maintaining a wide operating frequency range. As in other integrated CMOS RF circuits, power consumption and noise performance are also important in divider design.

In comparison with flip-flop-based static frequency dividers [11], injection-locked frequency dividers (ILFDs) [12]–[14] generally have lower power consumption and higher frequency capability in bulk CMOS technologies. However, ILFDs usually suffer from narrow locking ranges. This limitation can be significantly improved by proper structure selection and correct design methodology, as will be shown in this paper. As the scaling down of CMOS technology toward a 90- or 65-nm node, ILFDs provide a good low-power design choice besides the static dividers in the MMW PLL integration [16].

A conventional *LC*-based ILFD is shown in Fig. 1(a). The input stage $M_{\rm in}$ is used to provide both an input signal path and a dc bias path. Thus, $M_{\rm in}$ is typically large, resulting in a large input capacitance. Moreover, the input signal is significantly degraded by the parasitic capacitor $C_{\rm tail}$ in Fig. 1(a). By using a peaking inductor between the drain terminal of $M_{\rm in}$ and the ground, this problem can be reduced [18]; however, this strategy requires a greater chip area. Moreover, the Miller divider proposed in [15] faces the same problems of a large input capacitance and the need for a peaking inductor.

The 50-GHz direct ILFD in [12], as shown in Fig. 1(b), provides a solution for MMW operation with a low input capacitance, but it suffers from a narrow frequency locking range. Therefore, the passive loads of a direct ILFD in another study [14] are optimized to increase the frequency locking range. However, the power consumed by the resulting ILFD is relatively large, probably because the devices involved are also large and a current-limiting device is absent. Varactors are used at the output nodes in another ILFD [13] to increase the locking range. However, with a PLL system design, the need to synchronize the controlling voltages between the varactors in both the VCO and divider significantly increases design complexity.

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The authors are with the Institute of Electronic Engineering, National Chiao-Tung University, Hsinchu, 300 Taiwan, R.O.C. (e-mail: p9111846@alab.ee.nctu.edu.tw).

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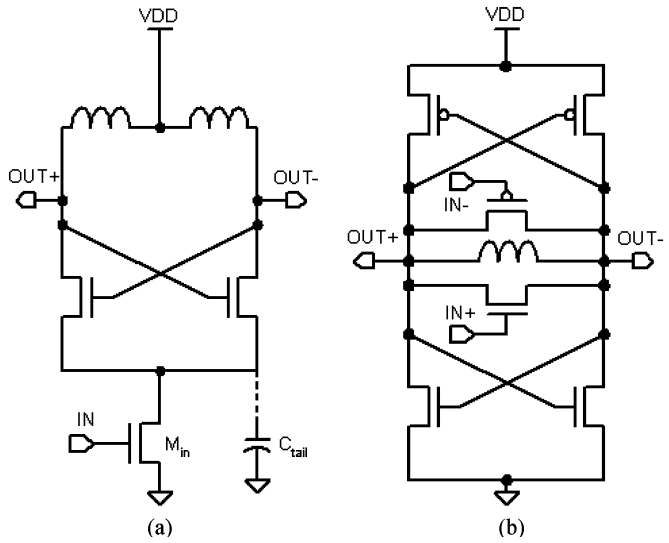

Fig. 1. Schematic diagrams of: (a) a conventional ILFD and (b) a direct ILFD [12].

In this study, an analytical model and design guidelines of a direct ILFD are presented. Based on the developed model and guidelines, a direct ILFD without a varactor is designed and fabricated using 0.13-μm bulk CMOS technology. With a simple pMOS current source and a suitable design, the proposed direct ILFD has a low input capacitance, large frequency locking range, low power consumption, and favorable noise suppression capability. Therefore, the proposed direct ILFD can be integrated with an MMW VCO into an MMW PLL system.

The frequency locking range of a conventional ILFD [19] is given by $2\omega_o\eta/3Q$, where ω_o and Q are the resonant frequency and the quality factor of the *LC* resonator, respectively, and η is the injection ratio. Accordingly, the locking range is inversely proportional to the Q factor of the *LC* resonator. However, the proposed analytical model herein reveals that for a direct ILFD, increasing the Q factor can reduce the power consumption without reducing the locking range. This result differs from the conventional one. For verification, the other direct ILFD with an *LC* resonator with a lower Q is fabricated and comparative measurements are made.

The measurements show that the center frequency of the proposed direct ILFD is around 70 GHz. The operating frequency range is 13.6% at 70 GHz with 4.4 mW from a supply voltage of 1 V and an input device size of only 3.6 μm/0.12 μm, which is smaller than that used in another study [12].

This paper is organized as follows. Section II proposes the analytical model and design guidelines of a direct ILFD. Based on these design guidelines, the circuit design considerations of the proposed direct ILFD are presented in Section III. The phase-noise analysis is presented in Section IV. The measured results are described and discussed in Section V. Finally, Section VI draws some conclusions.

II. Analytical Model and Design Guidelines

The general block diagram of a differential direct ILFD is shown in Fig. 2. The active G_m cell with positive feedback is designed to provide a negative resistance to compensate for the power loss from the resistive load per oscillating cycle for

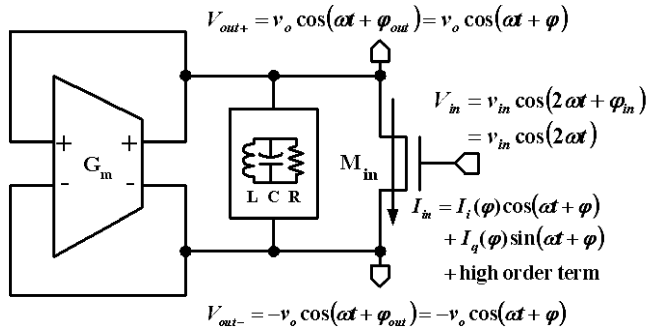

Fig. 2. General block diagram of a differential direct ILFD.

the stable output oscillating signals. L, C, and R represent the equivalent passive loads of the active G_m cell. The input stage is implemented by using an nMOS $M_{\rm in}$ only. The input voltage $V_{\rm in} = v_{\rm in}\cos(2\omega t + \varphi_{\rm in})$ is applied to the gate node of $M_{\rm in}$, where $\varphi_{\rm in}$ is the input phase. For the sake of convenience, it is assumed that $\varphi_{\rm in} = 0$, as shown in Fig. 2. If the input frequency 2ω falls into the divided-by-2 locking range, then the differential output voltages $V_{t,{\rm out}\pm}$ at the drain and the source nodes of $M_{\rm in}$ are given by $\pm v_o\cos(\omega t + \varphi_{\rm out})$, where $\varphi_{\rm out}$ is the output phase. If $\varphi_{\rm in} = 0$, then $\varphi_{\rm out}$ can be denoted as φ, which represents the phase difference between the input and output signals. In this situation, $M_{\rm in}$ can be regarded as a mixing device and the mixing channel current of $M_{\rm in}$ is denoted by $I_{\rm in}$.

In most cases, the input voltage is a large signal so $M_{\rm in}$ is operated in the on–off mode. Fig. 3(a) and (b) shows the two sample waveforms of $V_{\rm in}, V_{\rm out}\pm$ and $I_{\rm in}$, as φ is equal to $\pi/2$ and $\pi/4$, respectively. As shown in Fig. 3, the time interval between the two neighboring turn-on periods of $M_{\rm in}$ is π/ω. Since the frequency of the differential output voltages at the drain and source nodes of the $M_{\rm in}$ is exactly half of that of the input voltage, the resulting $I_{\rm in}$ in the two neighboring turn-on periods displays the same shapes, but opposite polarities as those shown in Fig. 3(a) and (b). Therefore, the fundamental frequency of $I_{\rm in}$ is ω and the fundamental component of $I_{\rm in}$ is denoted by $I_{{\rm in},\omega}$.

To develop the desired analytical model, $I_{{\rm in},\omega}$ is decomposed into in-phase and quadrature components

$$I_{{\rm in},\omega} = I_i(\varphi)\cos(\omega t + \varphi) + I_q(\varphi)\sin(\omega t + \varphi)\cdot \qquad (1)$$

As shown in Fig. 3(a) and (b), the shape of $I_{\rm in}$ strongly depends on φ. Therefore, the amplitudes of both components in (1) should also be the functions of φ.

In fact, φ is determined by the input frequency 2ω Fig. 4(a)–(c) plots the HSPICE simulated waveforms of $V_{\rm in}, V_{\rm out}\pm$, and $I_{\rm in}$ when 2ω is equal to, larger than, or smaller than $2\omega_o$, where ω_o is the resonant frequency of the equivalent passive load in Fig. 2. The waveforms of $I_i\cos(\omega t + \varphi)$ and $I_q\cos(\omega t + \varphi)$ calculated from $I_{\rm in}$ are also shown in each. Fig. 4(a) plots the waveforms in the case of $2\omega = 2\omega_o$. In this case, φ equals $\pi/2$ and $I_q(\pi/2) = 0$ so the phase of $I_{{\rm in},\omega}$ is the same as the output voltage signal. Therefore, $M_{\rm in}$ can be modeled as a single resistor $R_{\rm in}$ with the value of $I_i(\pi/2)/2v_o$. The equivalent model in this case is also shown in Fig. 4(a)

When the input frequency 2ω exceeds $2\omega_o$, as the waveforms plotted in Fig. 4(b), φ becomes slightly smaller than $\pi/2$ so

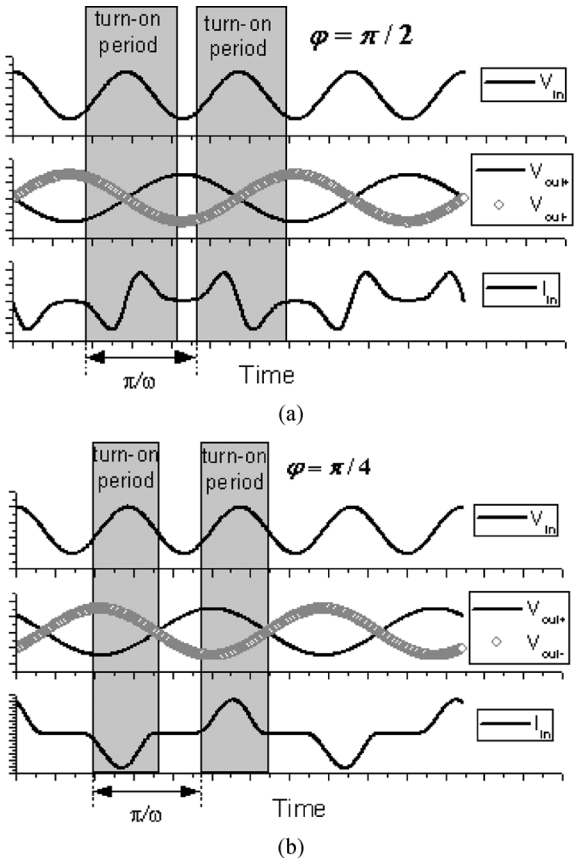

Fig. 3. Two waveforms of $V_{\rm in}, V_{\rm out}\pm$, and $I_{\rm in}$, as φ is equal to: (a) $\pi/2$ and (b) $\pi/4$.

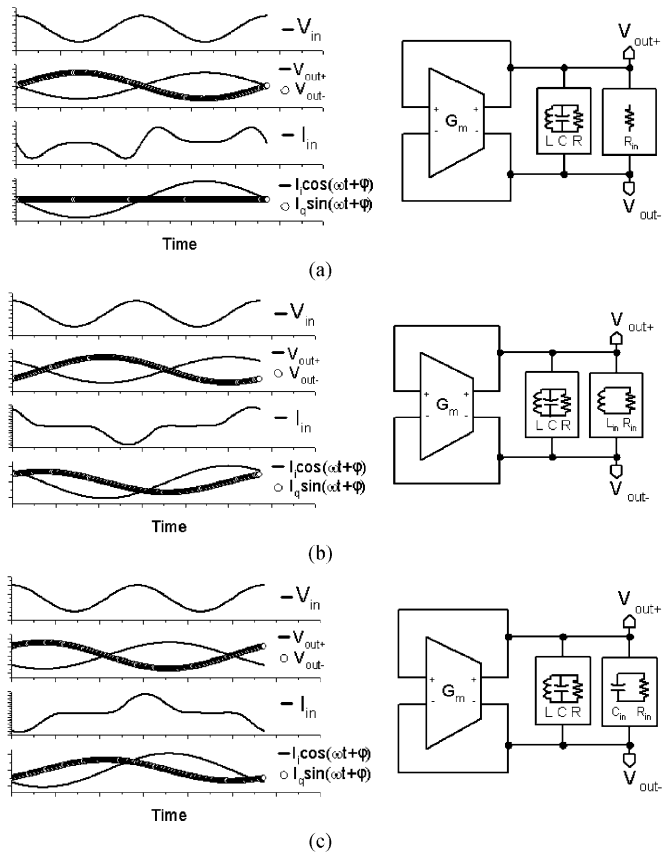

Fig. 4. Simulated waveforms of $V_{\rm in}, V_{\rm out\pm}, I_{\rm in}, I_i\cos(\omega t+\varphi), I_q\sin(\omega t+\varphi)$ and the equivalent model as: (a) $2\omega = 2\omega_o$, (b) $2\omega > 2\omega_o$, and (c) $2\omega < 2\omega_o$.

$I_{{\rm in},\omega}$ lags behind the output voltage signal. Therefore, $I_q(\varphi)$ is larger than 0 and $M_{\rm in}$ can be modeled as $R_{\rm in}$ in parallel with an inductor $L_{\rm in}\cdot R_{\rm in}$ and $L_{\rm in}$ are calculated as

$$R_{\rm in} = I_i(\varphi)/2v_o \tag{2}$$

and

$$L_{\rm in} = 2v_o/\omega I_q(\varphi) \approx 2v_o/\omega_o I_q(\varphi). \tag{3}$$

The equivalent model in this case is also presented in Fig. 4(b). The output frequency ω can be easily calculated as

$$\begin{aligned}\omega &= 1/\sqrt{C(L\|L_{\rm in})}\\ &\approx \sqrt{(1+2\omega_o L v_o/I_q(\varphi))/LC}\\ &\approx \omega_o + I_q(\varphi)/4Cv_o.\end{aligned} \tag{4}$$

Therefore, the maximum available value of $\omega, \omega_{\max}$ is determined by the maximum available value of $I_q(\varphi)/2v_o$, which is denoted by $g_{q,\max}\cdot\omega_{\max}$, and is given by

$$\omega_{\max} \approx \omega_o + \frac{1}{2C}\left(\frac{I_q(\varphi)}{2v_o}\right)_{\max} \equiv \omega_o + \frac{g_{q,\max}}{2C}. \tag{5}$$

The waveforms and equivalent model of the final case in which the input frequency 2ω is less than $2\omega_o$ are shown in Fig. 4(c). In this case, φ becomes slightly larger than $\pi/2$ such that $I_{{\rm in},\omega}$ leads to the output voltage signal. Therefore, $I_q(\varphi)$ is smaller than 0 and $M_{\rm in}$ can be modeled as $R_{\rm in}$ in parallel with a capacitor $C_{\rm in}$, whose capacitance is given by

$$C_{\rm in} = I_q(\varphi)/2v_o\omega \approx I_q(\varphi)/2v_o\omega_o. \tag{6}$$

The output frequency ω can be easily calculated as

$$\begin{aligned}\omega &= 1/\sqrt{L(C+C_{\rm in})}\\ &\approx \sqrt{1/LC\,(1-I_q(\varphi)/2\omega_o C v_o)}\\ &\approx \omega_o - |I_q(\varphi)/4Cv_o|.\end{aligned} \tag{7}$$

Therefore, the minimum available value of $\omega, \omega_{\min}$ is determined by the minimum available $I_q(\varphi)/2v_o$, which is denoted by $g_{q,\min}\cdot\omega_{\min}$, and can be expressed as

$$\omega_{\min} \approx \omega_o - \frac{1}{2C}\left|\left(\frac{I_q(\varphi)}{2v_o}\right)_{\min}\right| \equiv \omega_o - \frac{|g_{q,\min}|}{2C}. \tag{8}$$

From (5) and (8), the input frequency locking range denoted by $\Delta\omega_{\rm in}$ can be calculated as

$$\Delta\omega_{\rm in} = 2(\omega_{\max}-\omega_{\min}) = \left(g_{q,\max}+|g_{q,\min}|\right)/C. \tag{9}$$

Given the symmetric differential structure in Fig. 2, for a particular output voltage amplitude v_o, $g_{q,\max}$ equals $-g_{q,\min}$, and

(9) can be further simplified as

$$\Delta\omega_{\rm in} = 2g_{q,\max}/C = 2\omega_o^2 L g_{q,\max}. \tag{10}$$

According to (10), $g_{q,\max}$ should be designed as large as possible to maximize the locking range $\Delta\omega_{\rm in}$ for fixed values of L and ω_o. However, since all voltage signals that are applied to $M_{\rm in}$ are large signals, no analytical equation exists for $g_{q,\max}$. Therefore, HSPICE is adopted to find the values of $g_{q,\max}$ in the variously biased cases. Fig. 5(a)–(d) shows contour maps of $g_{q,\max}$ for various dc overdrive voltages $V_{\rm ov}$ of $M_{\rm in}$ and output voltage amplitudes v_o with different input voltage amplitudes $v_{\rm in}$. In all these cases, $g_{q,\max}$ increases with $V_{\rm ov}$ for a fixed v_o and decreases as v_o increases in the high-$V_{\rm ov}$ region.

According to the proposed model, shown in Fig. 4, and the derived locking range equation (10), for a fixed L, the quality factor $Q = R/\omega L$ of the passive load in Fig. 4 does not directly influence the locking range. More accurately, the value of Q only indirectly influences the locking range through a change in $V_{\rm ov}$ or v_o, which changes $g_{q,\max}$, as shown in Fig. 5. For example, for a given G_m cell, a low Q of the passive load results in a smaller v_o and, thus, a larger $g_{q,\max}$ and the locking range that is given by (10). However, in low and high Q cases, the locking ranges can more fairly be compared with a fixed v_o and $V_{\rm ov}$. In this situation, $g_{q,\max}$ is fixed, as shown in Fig. 5, such that the locking ranges in low and high Q cases are the same for a fixed L and ω_o, as determined by (10). Since a lower Q passive load has a lower R, the G_m cell needs to consume more power in order to compensate for R to maintain the same output voltage amplitude v_o at resonance. Therefore, for any required v_o, using a higher Q passive load can reduce the power requirement without any reduction in the locking range.

From the above analysis, some design guidelines for a direct ILFD can be inferred. Firstly, $V_{\rm ov}$ of the input device should be designed as large as possible to maximize the $g_{q,\max}$ and frequency locking range. Secondly, a tradeoff exists between the output voltage amplitude v_o and the frequency locking range. Therefore, v_o should be set at its minimum tolerant value to maximize the frequency locking range. Finally, the Q factor of the passive load should be as large as possible to reduce the required dc power consumption without reducing the frequency locking range.

III. Circuit Design

A. Circuit Structure

Based on the design guidelines in Section II, the proposed ILFD circuit for high-speed operation is shown in Fig. 6. The circuit structure is simple in that it has no varactor, but it still provides a large frequency locking range.

In order to reduce the input capacitance, nMOS $M_{\rm in}$ is used as the only input stage to generate the injected current $I_{\rm in}$. Furthermore, instead of a complementary cross-coupled pair [12], an nMOS cross-coupled pair is used to implement the G_m cell in Fig. 2. Since the frequency locking range is inversely proportional to the total capacitance value at the output node, as in (10), the absence of a pMOS cross-coupled pair can significantly increase the frequency locking range. Adding a pMOS current source M_p, as shown in Fig. 6, provides two advantages over an ILFD presented in an earlier study [14], increasing the locking range. Firstly, since a tradeoff exists between the output

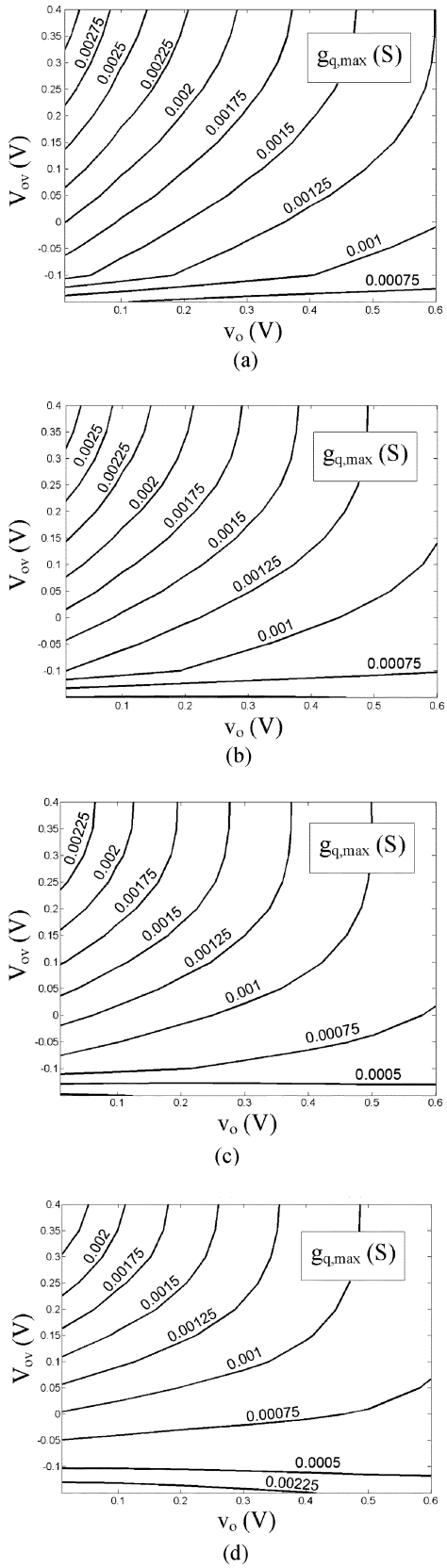

Fig. 5. Contour maps of $g_{q,\max}$ as: (a) $v_{\rm in} = 0.6$ V, (b) $v_{\rm in} = 0.5$ V, (c) $v_{\rm in} = 0.4$ V, and (d) $v_{\rm in} = 0.3$ V.

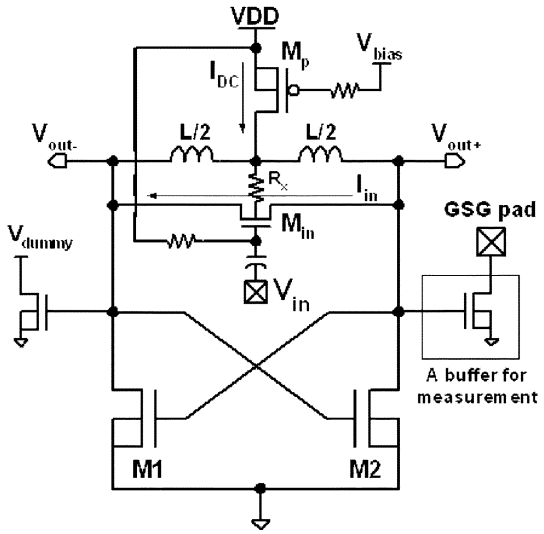

Fig. 6. Circuit structure of the proposed direct ILFD.

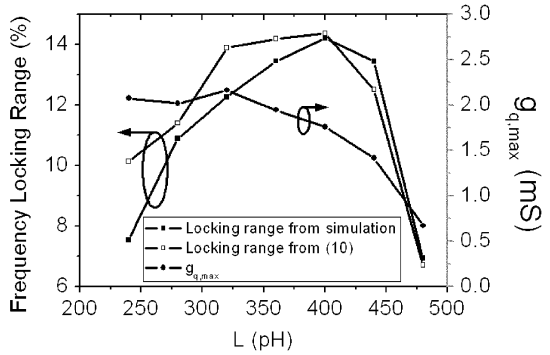

Fig. 7. Simulated frequency locking ranges and $g_{q,\max}$ with different values of the inductor.

voltage amplitude and the frequency locking range, the output voltage amplitude can be set to its minimum value by designing an appropriate dc current of M_p to maximize the locking range. Secondly, the dc voltage at the output node can be set much lower than the VDD because the dc current is limited by M_p. Therefore, $M_{\rm in}$ can be biased in the high overdrive voltage region. Additionally, through the resistor R_x, the dc voltage at the substrate node of $M_{\rm in}$ can be equal to those at the drain and source nodes such that the threshold voltage of $M_{\rm in}$ can be kept low to increase overdrive voltage.

B. Size of Input Stage

As the operating frequency increases to the MMW band, the size of the input nMOS $M_{\rm in}$ shown in Fig. 6 is restricted by the input capacitance since a large input capacitance makes the integration of an ILFD with an MMW VCO difficult. In the design, the target of the operating frequency is 70 GHz, and the width of the input nMOS $M_{\rm in}$ is designed as 3.6 μm, with the minimum length. From the simulation, the input capacitance of $M_{\rm in}$ is less than 10 fF, which is an acceptable load for an on-chip 70-GHz VCO.

C. Design of pMOS Current Source

The dc current of the pMOS current source denoted by $I_{\rm DC}$ directly influences the output voltage amplitude v_o. According to the model in Fig. 4, v_o can be estimated as $I_{\rm DC}(R||R_{\rm in})$ [20]. Notably, a tradeoff exists between v_o and the frequency locking range. Therefore, $I_{\rm DC}$ should be designed appropriately such that v_o just equals the required value at the edges of the frequency locking range.

D. Design of Integrated Spiral Inductor and Cross-Coupled Pair

Since the small size of $M_{\rm in}$ constrains the value of $g_{q,\max}$, careful design of an integrated spiral inductor and cross-coupled pair to achieve a large frequency locking range is important. It can be seen from (10) that the frequency locking range is proportional to the inductor value L. Initially, the frequency locking range increases with an increase in inductance. However, as L increases over an optimum value, the locking range begins to drop for the following two reasons. Firstly, the output center frequency ω_o can be expressed as

$$\omega_o \approx \sqrt{1/L\,(2W_{1,2}C_{\rm ov} + C_{\rm ox}W_{1,2}L_{1,2}/3 + C_{\rm next})}$$

where $W_{1,2}$ $(L_{1,2})$ is the width (length) of M_1 and M_2 in Fig. 6, $C_{\rm ov}$ is the overlap capacitance per unit width, $C_{\rm ox}$ is the gate–oxide capacitance per unit area, and $C_{\rm next}$ is capacitance from the next stage. Thus, as L increases, $W_{1,2}$ must be reduced to maintain the required ω_o. At a fixed dc current, this drop increases the dc gate voltages of M_1 and M_2 and, thus, reduces the overdrive voltage of $M_{\rm in}$ and $g_{q,\max}$ and, thus, the locking range. Secondly, if $W_{1,2}$ is too small to maintain enough G_m, such that the power loss per oscillating cycle from R and $R_{\rm in}$ in Fig. 4 cannot be compensated for when the input frequency falls in the range specified in (10), then the frequency locking range rapidly declines. Therefore, in this design, iterative simulations are required to find the optimum inductance of the spiral inductor for the maximum frequency locking range.

As mentioned in Section III-C, the Q factor of the passive load should be designed as large as possible to reduce the power consumption or $I_{\rm DC}$. Accordingly, no extra resistor is connected in parallel to the inductor in the proposed circuit.

The results of Ansoft's Nexxim simulation involving the frequency locking ranges with various inductances are shown in Fig. 7. In the simulation, the center output frequency is around 70 GHz, the input amplitude is 0.6 V, the input nMOS size is 3.6 μm/0.12 μm, and the minimum required output voltage amplitude is 250 mV. The $g_{q,\max}$ value in each case is obtained from Fig. 5 so the locking range can be given by (10). Fig. 7 also plots the $g_{q,\max}$ value and the locking range given by (10), which are consistent with the simulation results.

In order to consider the frequency shift resulting from the process and temperature variation [17], the corner models provided by the foundry are used to simulate the performance of the proposed divider. The shift of the center frequency is 6.98% from 0 °C FF corner to 100 °C SS corner. The simulated input sensitivity curves with an inductance of 400 pH in these two

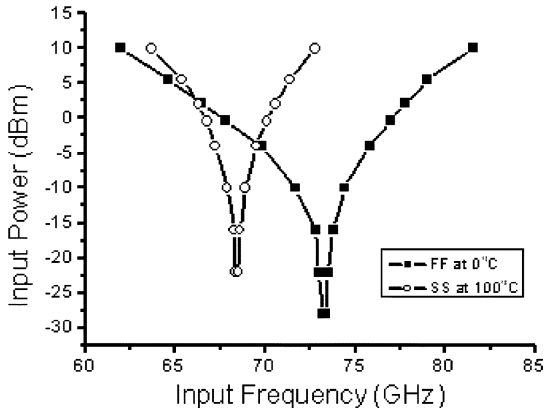

Fig. 8. Simulated input sensitivity curves in the corner cases.

extreme cases are shown in Fig. 8. The locking range of the divider is sufficient to cover the frequency shift as the input power is larger than 0 dBm.

IV. Phase-Noise Analysis

Here, the noise model in an earlier study [19] is modified and used to analysis the phase noise of a direct ILFD. The block diagram of a direct ILFD is redrawn in Fig. 9(a) with the active G_m cell replaced by a negative resistor $-R_{\rm act}$. $I_{{\rm in},\omega}$ is now given by a single sinusoidal function

$$\begin{aligned} I_{{\rm in},\omega} &= i_{\rm in,amp}\cos(\omega t+\alpha) \\ &= i_{\rm in,amp}\cos\left(\omega t+\varphi_{\rm out}+\gamma(\varphi_{\rm in}/2-\varphi_{\rm out})\right) \end{aligned} \tag{11}$$

where $i_{\rm in,amp}$ is the amplitude of $I_{{\rm in},\omega}$ and α is the phase of $I_{{\rm in},\omega}$, which can be decomposed to $\varphi_{\rm out}$ and the extra phase γ. Here, γ is related to the phase difference between the input and output voltage signal and, thus, it can be given as a function of $\varphi_{\rm in}/2-\varphi_{\rm out}$.

Fig. 9(b) presents the linear loop for the phase noise analysis, where $\varphi_{n,{\rm in}}$ and $\varphi_{n_{\rm out}}$ are the random variables that represent the small phase fluctuations of the input and output voltage signals. Here, $Z(\omega_m)$ represents the small phase response of the equivalent load in Fig. 9(a) and is given by

$$Z(\omega_m)=\frac{1}{1+2jQ_{\rm eq}\omega_m/\omega_o} \tag{12}$$

where $Q_{\rm eq}$ is the quality factor of the equivalent load and $\omega_m=\omega-\omega_o$ is the offset frequency. The values of the partial differentiations in Fig. 9(b) can be easily calculated using

$$\frac{\partial\alpha}{\partial\varphi_{\rm in}}=\frac{1}{2}\gamma'\left(\frac{1}{2}\varphi_{\rm in}-\varphi_{\rm out}\right) \tag{13}$$

and

$$\frac{\partial\alpha}{\partial\varphi_{\rm out}}=1-\gamma'\left(\frac{1}{2}\varphi_{\rm in}-\varphi_{\rm out}\right) \tag{14}$$

where γ is the derivative of γ. From (12)–(14), the transfer function of the input and output phase-noise spectral densities $S_{\varphi n\_{\rm in}}$ and $S_{\varphi n\_{\rm out}}$, respectively, is given by

$$\frac{S_{\varphi n\_{\rm out}}(\omega_m)}{S_{\varphi n\_{\rm in}}(\omega_m)}=\frac{14}{1+(\omega_m/\omega_P)^2} \tag{15}$$

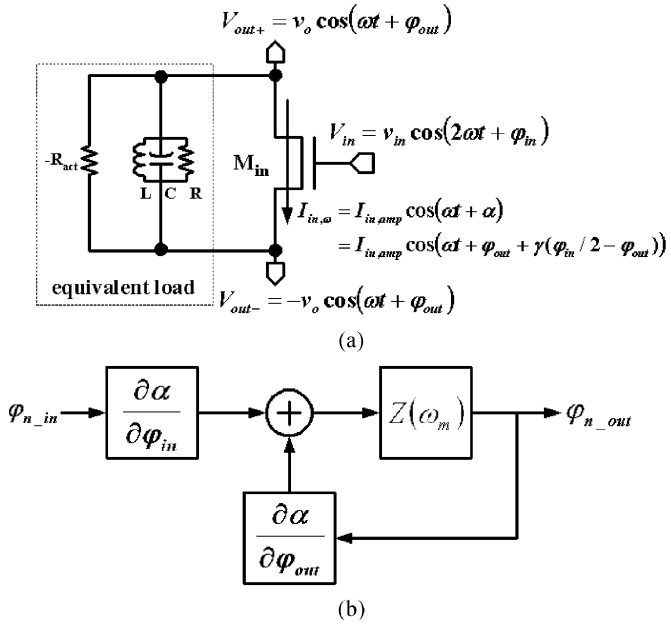

Fig. 9. (a) Block diagram of the direct ILFD. (b) Linear loop for the phase-noise analysis.

where

$$\omega_P=\omega_o\gamma'\left(12\varphi_{\rm in}-\varphi_{\rm out}\right)/2Q_{\rm eq}. \tag{16}$$

The calculation of the transfer function of the free-running and output phase-noise spectral densities ($S_{\varphi n\_{\rm free-run}}$ and $S_{\varphi n\_{\rm out}}$) is as in an earlier cited study [19]; only the result is shown here as follows:

$$\frac{S_{\varphi n\_{\rm out}}(\omega_m)}{S_{\varphi n\_{\rm free-run}}(\omega_m)}=\frac{(\omega_m/\omega_P)^2}{1+(\omega_m/\omega_P)^2}. \tag{17}$$

From (15), the input phase noise appears at the output with a 6-dB reduction and low-pass shaping, dominating the output phase noise when the offset frequency is less than ω_P. When the offset frequency exceeds ω_P, then from (17), the output phase noise is dominated by the phase noise of the divider in free run. This result is similar to that of a conventional ILFD. The simulated curves of $S_{\varphi n\_{\rm out}}/S_{\varphi n\_in}$ with various $\omega_o, V_{\rm ov}$ and $v_{\rm in}$ at the central frequency are plotted in Fig. 10. From Fig. 10, $\omega_P/2\pi$ increases with $\omega_o/2\pi$ and generally exceeds 1 GHz when $\omega_o/2\pi > 35$ GHz and $V_{\rm ov} > 0V$. Therefore, with respect to noise, this structure is also suitable for MMW operations because as ω_o becomes large, its internal noise can be suppressed even at a large offset frequency.

V. Measurement Results

The proposed ILFD shown in Fig. 6 is designed and fabricated using 0.13-μm bulk CMOS technology with a supply voltage of 1 V. The size of the $M_{\rm in}$ is only 3.6 μm/0.12 μm. A low- Q ILFD with a resistor that is connected in parallel with L to reduce the Q factor is also fabricated on the same chip to observe the relationship between the locking range and the Q factor. The chip micrographs of both fabricated ILFDs are shown in Fig. 11.

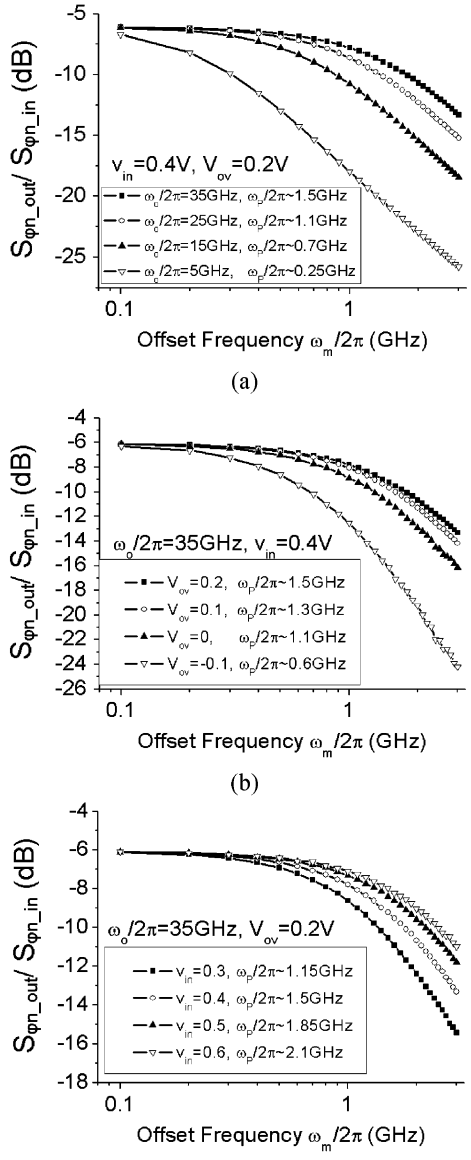

Fig. 10. Simulated curves of $S_{\varphi n\mathrm{out}}/S_{\varphi n,\mathrm{in}}$ with different: (a) ω_o, (b) V_{ov}, and (c) V_{in} at the central frequency.

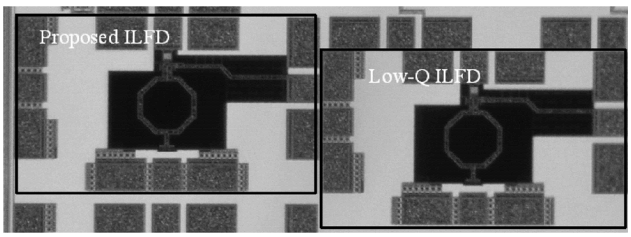

Fig. 11. Micrographs of ILFDs.

After the losses from the cable and buffer have been deembedded, the measured output amplitudes versus the input frequencies for the various values of I_{DC} are presented in Fig. 12(a). The locking range can be determined by the difference between the frequencies at the two ends of each curve in Fig. 12(a). Fig. 12(b) plots the curves of the locking range and the minimum output amplitude in throughout the locking

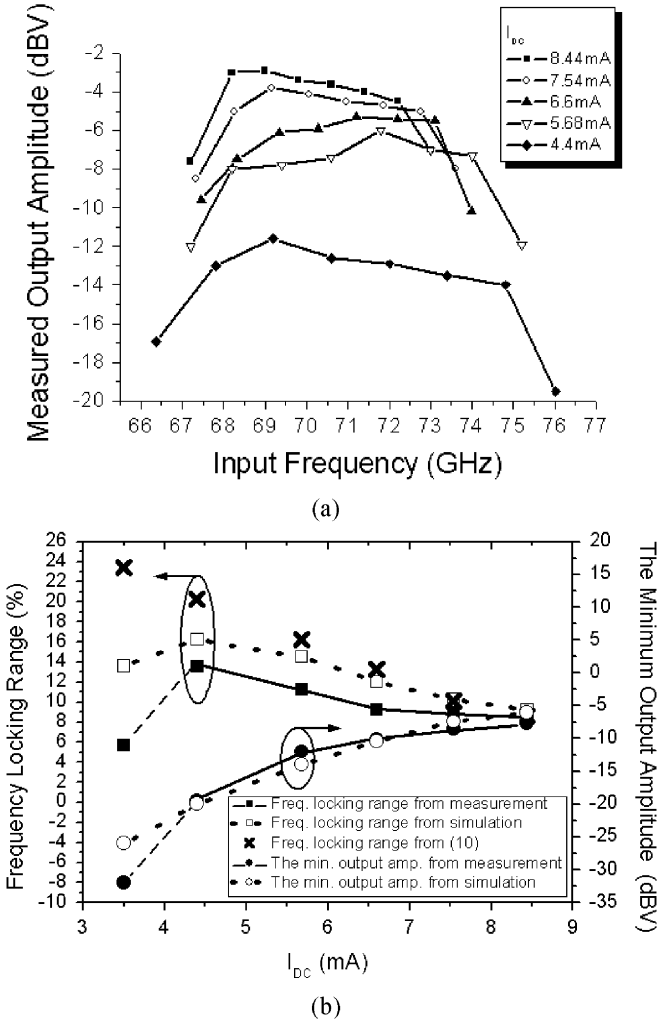

Fig. 12. (a) Measured output amplitude versus input frequency. (b) Measured and calculated/simulated locking range and the minimum output amplitude versus I_{DC}.

range versus I_{DC}. The simulated and calculated curves are also shown for comparison. The locking range can be increased significantly by choosing a suitable value for I_{DC} at the cost of a reduced output voltage amplitude. This result is consistent with those of the analysis. Notably, I_{DC} should be kept larger than the specific current to maintain a sufficient G_m to compensate for the power loss form the equivalent resistive load per oscillating cycle. Otherwise, the stable output oscillating signals cannot be maintained. Thus, the locking range declines rapidly, as shown in the long broken-line regions of the measured curves in Fig. 12(b). The maximum measured locking range is 13.6% (66.4–76 GHz) with an I_{DC} of 4.4 mA from a 1-V supply. Except at the low I_{DC}, the calculated locking ranges from (10) are consistent with the measurement results.

The measured frequency locking ranges as the supply voltage decreases to 0.8 V are plotted in Fig. 13. The locking ranges are considerably smaller than those in the 1-V case because the drop in the supply voltage reduces the overdrive voltage of M_{in} and also $g_{q,\max}$. This result is also consistent with analytic results.

The measured locking ranges versus the output voltage amplitudes of the proposed and low-Q ILFDs are plotted

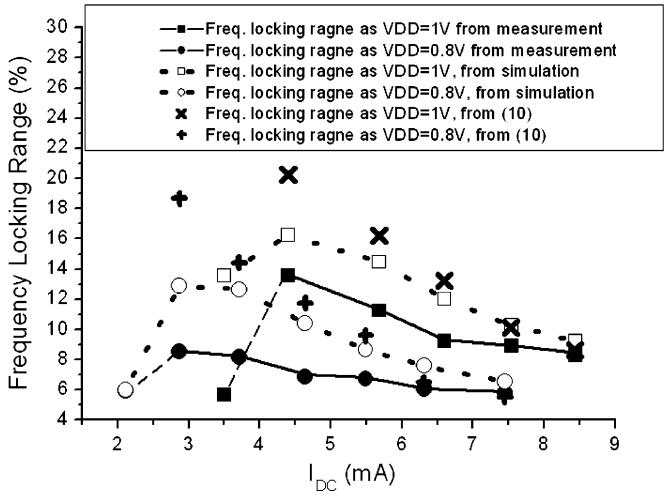

Fig. 13. Locking range as the supply voltages are 0.8 and 1 V.

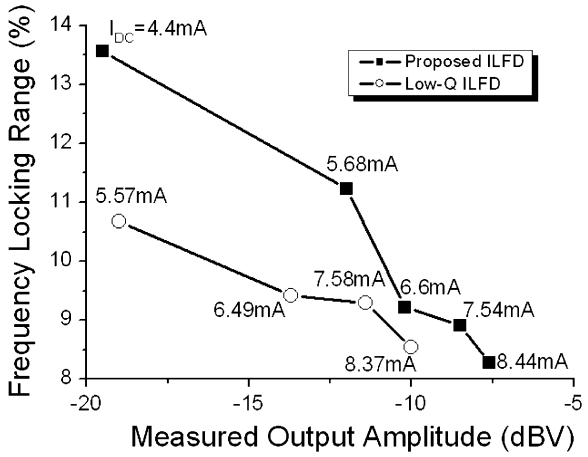

Fig. 14. Measured locking ranges versus output voltage amplitudes of both proposed and low-Q ILFDs.

in Fig. 14. The value of $I_{\rm DC}$ in each case is marked on the measured curves. For any required output voltage amplitude, reducing the Q factor not only increases the required $I_{\rm DC}$, but also reduces the frequency locking range. The locking range declines because an increase in $I_{\rm DC}$ reduces the overdrive voltage and thereby also $g_{q,\max}$. The measured input sensitivities of both dividers are plotted in Fig. 15. The proposed ILFD also has a greater input sensitivity than the low-Q ILFD.

The measured output phase noise and phase noise of the input signal from the Agilent MMW Source Module E8257DS15 [22] are both plotted in Fig. 16(a). This figure reveals that the output phase noise is determined by the input phase noise below the 300-kHz offset frequency. Beyond the 300-kHz offset, the output phase noise is corrupted by a flat noise floor of approximately -120 dBc/Hz. The waveform of this extra noise is flat and shapeless so its source is not within the closed loop that is shown in Fig. 9(b). Since only the single-ended output signal is measured, this noise floor may be from the common-mode noise from the pMOS current source, supply voltage, and ground, or the instrument itself. The output phase noise and the phase noise in free run are both plotted in Fig. 16(b). Although

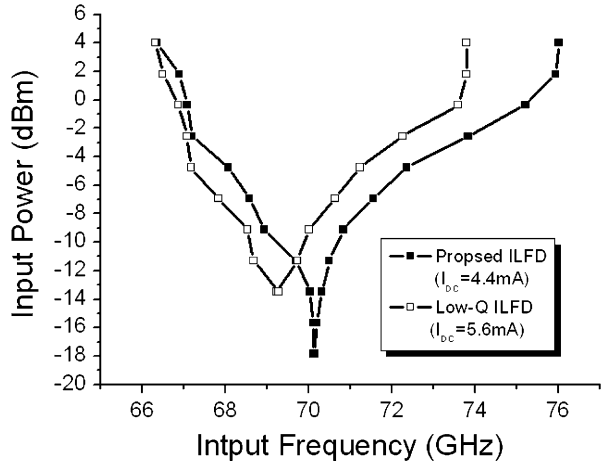

Fig. 15. Measured input sensitivities of both ILFDs.

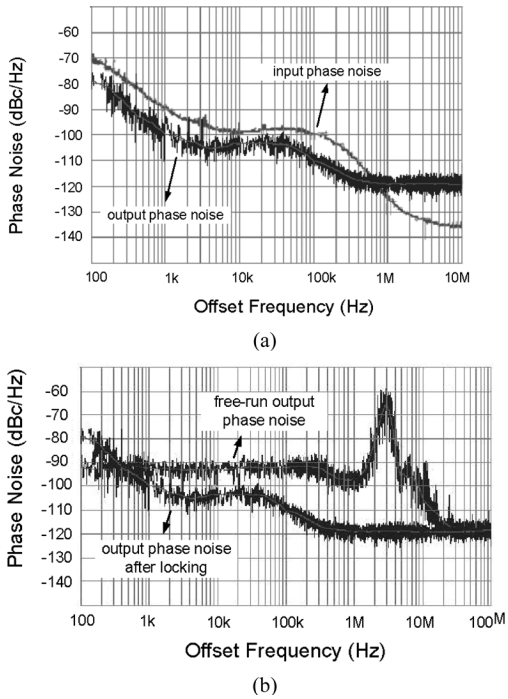

Fig. 16. (a) Measured output phase noise and the phase noise of input signal from Agilent MMW Source Module E8257DS15 [22]. (b) Measured output phase noise and the free-run phase noise.

the output signal in free run is noisy, the output phase noise after locking is almost independent of the phase noise in free run below the 10-MHz offset frequency. Beyond the 10-MHz offset frequency, the phase noise in free run is also corrupted by a flat noise floor at around -120 dBc/Hz. Therefore, the internal noise in the loop in Fig. 9(b) from the ILFD is observably suppressed before the 10-MHz offset frequency at the very least.

The performances of the proposed divider and other CMOS frequency dividers at above 40 GHz are compared in Table I. Without a varactor, the locking range of the proposed divider is 13.6% at 70 GHz. Finally, the device size of the input stage is 3.6 μm/0.12 μm, which is smaller than that presented elsewhere [12].

TABLE I
PERFORMANCE COMPARISON BETWEEN THE PROPOSED CMOS ILFD AND OTHER CMOS FREQUENCY DIVIDERS

	This work	[12]	[13]	[14]	[15]
Technology	0.13μm	0.13μm	90nm	0.2μm	0.18μm
Divided number	2	2	4	2	2
Input frequency	70GHz	50GHz	70GHz	55GHz	40GHz
VDD	1V	1.5V	0.5V	1V	2.5V
Locking Range	13.57%	0.16%	12.4%	5.89%	5.8%
With/without varactors	Without	Without	With	Without	Without
Power consumption	4.4mW	3mW	2.75 mW	10.1 mW	16.8 mW
Size of the input device	3.6μm/ 0.12μm	6μm/ 0.12μm	--	--	--

VI. SUMMARY

In this paper, an analytical model for a direct ILFD is presented. From the proposed model, important design guidelines have been developed. Based on the design guidelines, a 70-GHz direct ILFD has been designed and fabricated using 0.13-μm bulk CMOS technology, where a pMOS current source was used to restrict the output voltage amplitude and to increase the overdrive voltage of the input device to improve the frequency locking range. For a direct ILFD, a higher Q passive load can release the power required without decreasing the frequency locking range. Even if the input device size is small and the varactor is not used, the frequency locking range is large. Therefore, the proposed direct ILFD can be integrated with an MMW VCO easily and is a favorable choice for use in a CMOS MMW PLL system.

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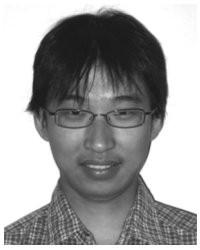
Chung-Yu Wu S'76–M'76–SM'96–F'98) was born in 1950. He received the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 1976 and 1980, respectively.

Since 1980, he has been a consultant to high-tech industry and research organizations and has built up strong research collaborations with high-tech industries. From 1980 to 1983, he was an Associate Professor with National Chiao Tung University. From 1984 to 1986, he was a Visiting Associate Professor with the Department of Electrical Engineering, Portland State University, Portland, OR. Since 1987, he has been a Professor with National Chiao Tung University. From 1991 to 1995, he served as the Director of the Division of Engineering and Applied Science, National Science Council, Taiwan, R.O.C. From 1996 to 1998, he was honored as the Centennial Honorary Chair Professor with National Chiao Tung University. He is currently the President and Chair Professor of National Chiao Tung University. In Summer 2002, he conducted post-doctoral research with the University of California at Berkeley. He has authored or coauthored over 250 technical papers in international journals and conferences. He hold 19 patents, including nine U.S. patents. His research interests are nanoelectronics, biochips, neural vision sensors, RF circuits, and computer-aided design (CAD) analysis.

Dr. Wu is a member of Eta Kappa Nu and Phi Tau Phi. He was a recipient of 1998 IEEE Fellow Award and a 2000 Third Millennium Medal. He has also been the recipient of numerous research awards presented by the Ministry of Education, National Science Council (NSC), and professional foundations in Taiwan, R.O.C.



Chi-Yao Yu was born in Taipei, Taiwan, R.O.C., in 1978. He received the Master's degree in communication engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 2002, and is currently working toward the Ph.D. degree at National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

His current research is focused on communication systems, mixed-signal integrated circuit design, CMOS MMW circuits, and CMOS RF front-end circuit design.