

Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO₃ Metal–Insulator–Metal Capacitors

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Abstract—We have studied the stress reliability of low-energy-bandgap high- κ SrTiO₃ metal–insulator–metal capacitors under constant voltage stress. By using a high-work-function Ni electrode (5.1 eV), we reduced the degrading effects of stress on the capacitance variation ($\Delta C/C$), the quadratic voltage coefficient of capacitance (VCC- α), and the long-term reliability, in contrast with using a TaN. The improved stress reliability for the Ni electrode capacitors is attributed to a reduction of carrier injection and trapping.

Index Terms—High work function, metal–insulator–metal (MIM), Ni, reliability, SrTiO₃ (STO).

I. INTRODUCTION

WHEN SCALING down the device size of metal–insulator–metal (MIM) capacitors [1]–[12] used for analog, RF, and DRAM functions in ICs, it is necessary to continuously increase the capacitance density ($\epsilon_0\kappa/t_\kappa$) [1]. To achieve this goal, the only choice is to increase the κ value of the dielectrics, which have evolved from Al₂O₃, HfO₂–Al₂O₃ [2]–[5], Nb₂O₅ [6], TiTaO ($\kappa \sim 45$ –50) [7]–[9] to SrTiO₃ (STO; $\kappa \sim 50$ –200) [10]–[14]. However, few studies of the stress reliability of the analog characteristics of MIM devices have been reported [4], [5], beyond considerations of the simple time-dependent dielectric breakdown, despite its importance for circuit applications. This stress degradation is particularly a concern in low-breakdown field and small-bandgap STO materials, which also leads to high leakage currents because of the small conduction band discontinuity (ΔE_C) with respect to Si [15]. Here, we describe the stress reliability of the analog characteristics of STO MIM capacitors. The use of high-work-

function Ni instead of TaN electrodes not only reduces the high-temperature leakage current but also improves the constant voltage stress degradations of the capacitance variation ($\Delta C/C$) and the quadratic voltage coefficient of capacitance (VCC- α). The improved stress tolerance arises from reduced carrier injection and trapping in the MIM capacitor.

II. EXPERIMENTAL PROCEDURE

The process to integrate the MIM capacitors into a very large scale integration backend process began with depositing a 2- μ m-thick SiO₂ isolation layer on the Si substrates. Then, the TaN/Ta layers were deposited by sputtering and subsequently treated in a nitrogen plasma, which largely improves oxygen deficiency and capacitance density degradation by forming interfacial TaON during postdeposition anneal [10]–[12]. A 25-nm-thick sputtered STO dielectric was then deposited, followed by a 420 °C furnace anneal for 30 min under an oxygen ambient, to improve the dielectric quality. This lower thermal budget process, compared with previous nanocrystal STO approaches [10], [11], is desirable for backend integration, but comes at the expense of a lower κ value. In addition, it is generally accepted that the STO mixed with amorphous and crystalline phase by low-temperature process achieves better uniformity, compared with high-temperature-formed polycrystalline phase as reported in previous study [18]. Finally, a TaN or Ni was deposited and patterned to form the top capacitor electrode. The fabricated devices, having a 20 \times 20- μ m area, were characterized by capacitance–voltage (C – V) and J – V measurements using an HP4156B semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively.

III. RESULTS AND DISCUSSION

Fig. 1(a) and (b) shows the J – V and C – V characteristics of STO MIM devices, respectively. For negative bias, with electron injection from the upper electrode, use of a Ni as the electrode gave approximately two orders of magnitude lower leakage current at 125 °C than devices using a TaN. At positive bias, the leakage current is also reduced. This is due to additional voltage drop by band bending shown in the inserted thermal equilibrium band diagram, which originated from the higher work function of a Ni (5.1 eV) than a TaN (~ 4.5 eV). Thus, improved leakage currents are obtained at both positive and negative bias [7]. The effect of voltage stress on the C – V

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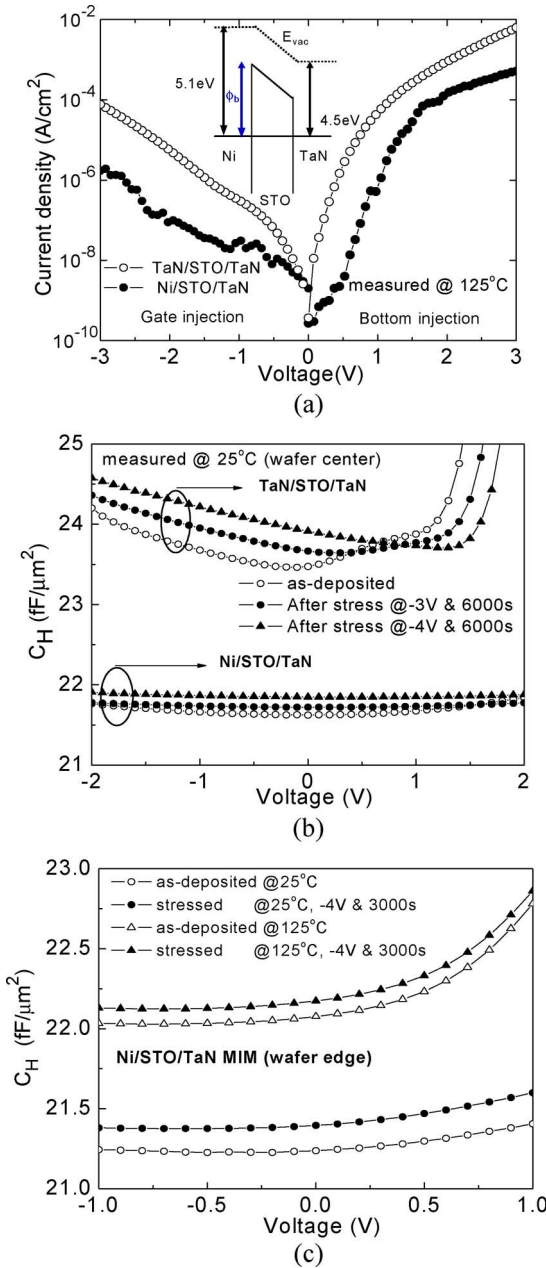


Fig. 1. (a) J - V characteristics of [Ni or TaN]/STO/TaN capacitors, measured at 125 °C. The inserted figure is the band alignment of the STO MIM device with TaN or Ni as the upper electrode. (b) C - V characteristics of [Ni or TaN]/STO/TaN capacitors before and after different voltage stress at 25 °C. (c) C - V characteristics of Ni/STO/TaN capacitors before and after constant voltage stress at 25 °C and 125 °C.

characteristics is also shown in Fig. 1(b). The TaN top electrode gives slightly larger capacitance than the Ni electrode, which may be due to process variation and difference in capacitance from the space charge effect by different work function [16]. However, only 9% difference in capacitance cannot explain the one to two orders of magnitude leakage current difference shown in Fig. 1(a). Furthermore, the desired smaller $\Delta C/C$ value after stress is displayed when using a Ni electrode. These results are for the 25 °C case rather than the normally used 85 °C ~ 125 °C [17]. This is because the stress-induced degradation of $\Delta C/C$ was larger at 25 °C than at 125 °C, as shown in Fig. 1(c)—we suggest that this may be due to the

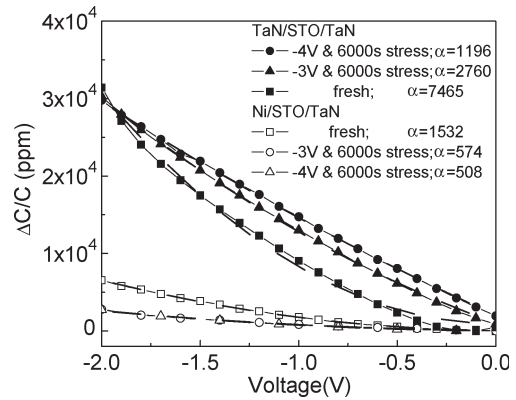


Fig. 2. $\Delta C/C$ - V characteristics of MIM capacitors with Ni and with TaN electrodes.

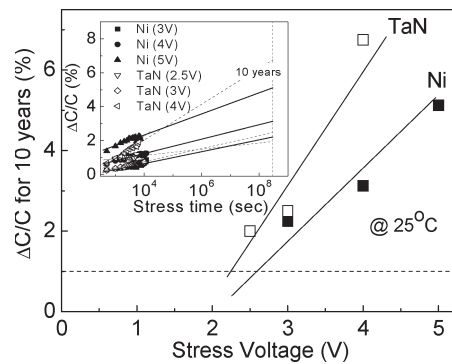


Fig. 3. $\Delta C/C$ versus stress voltage for a ten-year reliability period. The $\Delta C/C$ values for ten-year stress were obtained from the inserted figure of the extrapolated $\Delta C/C$ versus stress time to ten years.

charge detrapping in the small-bandgap STO MIM capacitor at elevated temperatures. The higher $\Delta C/C$ at 125 °C is due to the higher carrier injection at higher temperature, which gives much higher carrier concentration and a smaller relaxation time and leads to a larger capacitance variation [3], [4].

For analog/RF functions in a circuit, both small $\Delta C/C$ and $VCC-\alpha$ are required. Here, $\Delta C/C$ can be expressed as $VCC-\beta \times V + VCC-\alpha \times V^2$, where $VCC-\alpha$ is the linear coefficient of the VCC. Fig. 2 shows the effect of constant voltage stress on the $\Delta C/C - V$ characteristics of STO MIM capacitors with the TaN or Ni electrodes. By using a Ni, the required small $\Delta C/C$ and $VCC-\alpha$ were achieved, regardless of the stress. In general, the stress produced a lower $VCC-\alpha$, which is related to the charge trapping in the STO and the STO/metal interface. The trapped charges decrease the carrier mobility in the dielectric by electrostatic scattering, which in turn produces a smaller $VCC-\alpha$, according to a free-carrier-injection model [3], [4].

The $\Delta C/C$ for a ten-year operational span is also important. Fig. 3 shows the $\Delta C/C$ as a function of stress voltage for a ten-year reliability, these data were obtained from the inserted $\Delta C/C$ plot by extrapolating to that time. Here, the stress was performed at 25 °C rather than 125 °C, which should be a worse case as indicated by the results in Fig. 1(c). In addition, the capacitors with a Ni electrode show smaller $\Delta C/C$ for a stress extrapolated to ten years than the TaN case. Thus, we suggest that the reduced charge injection by higher work

function electrode may cause less trap or defect formation during the stress, which in turn suppress new dipole generation and achieve better $\Delta C/C$. Moreover, the relative smooth surface and mixed amorphous nanocrystalline STO [18], which is formed by low-temperature process, may also reduce the charge trapping in interface and grain boundaries, respectively. It is worth noting that only $< 1\%$ 10-year $\Delta C/C$ is obtained by linear extrapolation to 1 V. This is suitable for achieving good reliability for analog applications at 45-nm node and beyond operated at 1 V and less. Thus, the high-work-function Ni electrode not only decreases the leakage current in our devices but also improves the $\Delta C/C$ arising from charge trapping and the stress reliability.

IV. CONCLUSION

The stress reliability of low-bandgap STO MIM capacitors was investigated. The stress degradation of $\Delta C/C$, $VCC-\alpha$, and the ten-year extrapolated reliability can be improved by using a high-work-function Ni rather than a TaN electrode. The Ni electrodes also have an added economic advantage over high-work-function noble metals.

REFERENCES

- [1] *The International Technology Roadmap for Semiconductors*, 2005, San Jose, CA: Semicond. Ind. Assoc. [Online]. Available: www.itrs.net
- [2] H. Hu, S. J. Ding, H. F. Lim, C. Zhu, M. F. Li, S. J. Kim, X. F. Yu, J. H. Chen, Y. F. Yong, B. J. Cho, D. S. H. Chan, S. C. Rustagi, M. B. Yu, C. H. Tung, A. Du, D. My, P. D. Fu, A. Chin, and D. L. Kwong, "High performance HfO₂-Al₂O₃ laminate MIM capacitors by ALD for RF and mixed signal IC applications," in *IEDM Tech. Dig.*, 2003, pp. 379–382.
- [3] C. Zhu, H. Hu, X. Yu, S. J. Kim, A. Chin, M. F. Li, B. J. Cho, and D. L. Kwong, "Voltage and temperature dependence of capacitance of high-k HfO₂ MIM capacitors: A unified understanding and prediction," in *IEDM Tech. Dig.*, 2003, pp. 879–882.
- [4] S.-J. Ding, H. Hu, C. Zhu, S. J. Kim, X. Yu, M.-F. Li, B. J. Cho, D. S. H. Chan, M. B. Yu, S. C. Rustagi, A. Chin, and D.-L. Kwong, "RF, DC, and reliability characteristics of ALD HfO₂-Al₂O₃ laminate MIM capacitors for Si RF IC applications," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 886–894, Jun. 2004.
- [5] K. Takeda, R. Yamada, T. Imai, T. Fujiwara, T. Hashimoto, and T. Ando, "DC-stress-induced degradation of analog characteristics in Hf_xAl_(1-x)O MIM capacitors," in *IEDM Tech. Dig.*, 2006, pp. 359–362.
- [6] S. J. Kim, B. J. Cho, M. B. Yu, M.-F. Li, Y.-Z. Xiong, C. Zhu, A. Chin, and D. L. Kwong, "High capacitance density ($> 17 \text{ fF}/\mu\text{m}^2$) Nb₂O₅-based MIM capacitors for future RF IC applications," in *VLSI Symp. Tech. Dig.*, 2005, pp. 56–57.
- [7] K. C. Chiang, A. Chin, C. H. Lai, W. J. Chen, C. F. Cheng, B. F. Hung, and C. C. Liao, "Very high- κ and high density TiTaO MIM capacitors for analog and RF applications," in *VLSI Symp. Tech. Dig.*, 2005, pp. 62–63.
- [8] K. C. Chiang, C. C. Huang, A. Chin, W. J. Chen, S. P. McAlister, H. F. Chiu, J. R. Chen, and C. C. Chi, "High- κ Ir/TiTaO/TaN capacitors suitable for analog IC applications," *IEEE Electron Device Lett.*, vol. 26, no. 7, pp. 504–506, Jul. 2005.
- [9] K. C. Chiang, C. H. Lai, A. Chin, T. J. Wang, H. F. Chiu, J. R. Chen, S. P. McAlister, and C. C. Chi, "Very high density ($23 \text{ fF}/\mu\text{m}^2$) RF MIM capacitors using high- κ TiTaO as the dielectric," *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 728–730, Oct. 2005.
- [10] K. C. Chiang, C. C. Huang, A. Chin, W. J. Chen, H. L. Kao, M. Hong, and J. Kwo, "High performance micro-crystallized TaN/SrTiO₃/TaN capacitors for analog and RF applications," in *VLSI Symp. Tech. Dig.*, 2006, pp. 126–127.
- [11] K. C. Chiang, C. C. Huang, A. Chin, G. L. Chen, W. J. Chen, Y. H. Wu, and S. P. McAlister, "High performance SrTiO₃ metal-insulator-metal capacitors for analog applications," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2312–2319, Sep. 2006.
- [12] K. C. Chiang, C. H. Cheng, H. C. Pan, C. N. Hsiao, C. P. Chou, A. Chin, and H. L. Hwang, "High temperature leakage improvement in metal-insulator-metal capacitors by work-function tuning," *IEEE Electron Device Lett.*, vol. 28, no. 3, pp. 235–237, Mar. 2007.
- [13] M. Iwabuchi and T. Kobayashi, "Growth and characterization of epitaxial SrTiO₃ thin films with prominent polarizability," *J. Appl. Phys.*, vol. 75, no. 10, pp. 5295–5301, May 1994.
- [14] K. Abe and S. Komatsu, "Epitaxial growth of SrTiO₃ films on Pt electrodes and their electrical properties," *Jpn. J. Appl. Phys.*, vol. 31, no. 9B, pp. 2985–2988, Sep. 1992.
- [15] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electron devices," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 18, no. 3, pp. 1785–1791, May 2000.
- [16] K. Morito, T. Suzuki, S. Sekiguchi, H. O. Okushi, and M. Fujimoto, "Electrical characterization of SrTiO₃ thin films grown on Nb-doped SrTiO₃ single crystals," *Jpn. J. Appl. Phys.*, vol. 39, no. 1, pp. 166–171, Jan. 2000.
- [17] C. H. Lai, A. Chin, H. L. Kao, K. M. Chen, M. Hong, J. Kwo, and C. C. Chi, "Very low voltage SiO₂/HfON/HfAlO/TaN memory with fast speed and good retention," in *VLSI Symp. Tech. Dig.*, 2005, pp. 54–55.
- [18] J. L. Cousins and D. E. Kotecki, "Simulation of the variability in micro-electronic capacitors having polycrystalline dielectrics," *IEEE Electron Device Lett.*, vol. 23, no. 5, pp. 267–269, May 2002.