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(54) **FLEXIBLE NON-VOLATILE MEMORY**

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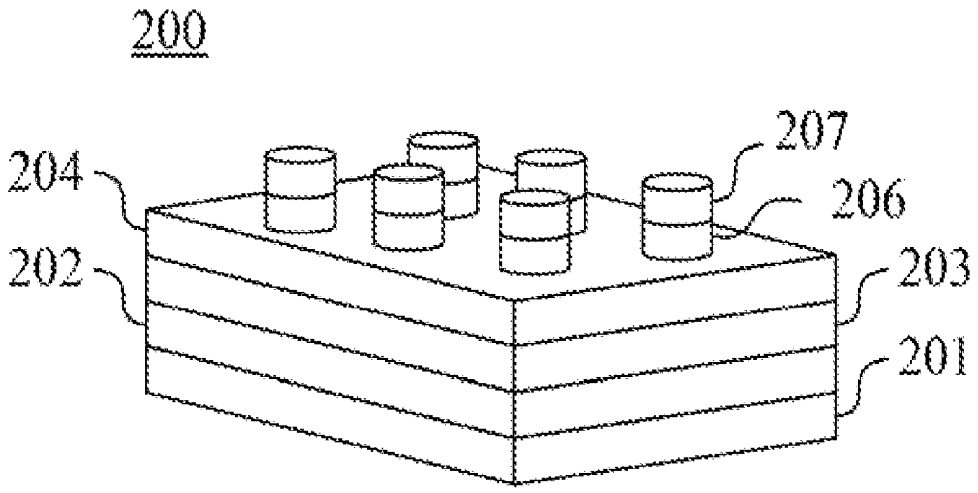
CPC ***H01L 45/00*** (2013.01)
USPC **257/4**; 438/104

(57) **ABSTRACT**

A manufacturing method for manufacturing a flexible non-volatile memory is provided. The manufacturing method comprises the steps outlined below. A flexible substrate is provided. A planarization layer is formed on the flexible substrate. A metal bottom electrode layer is deposited on the planarization layer. A mask is formed to define a plurality of patterns. An AZTO layer having a plurality of electrically independent AZTO cells is deposited on the metal bottom electrode layer corresponding to the patterns. A top electrode layer is deposited on the AZTO layer corresponding to the AZTO cells to form a plurality of non-volatile memory cells.



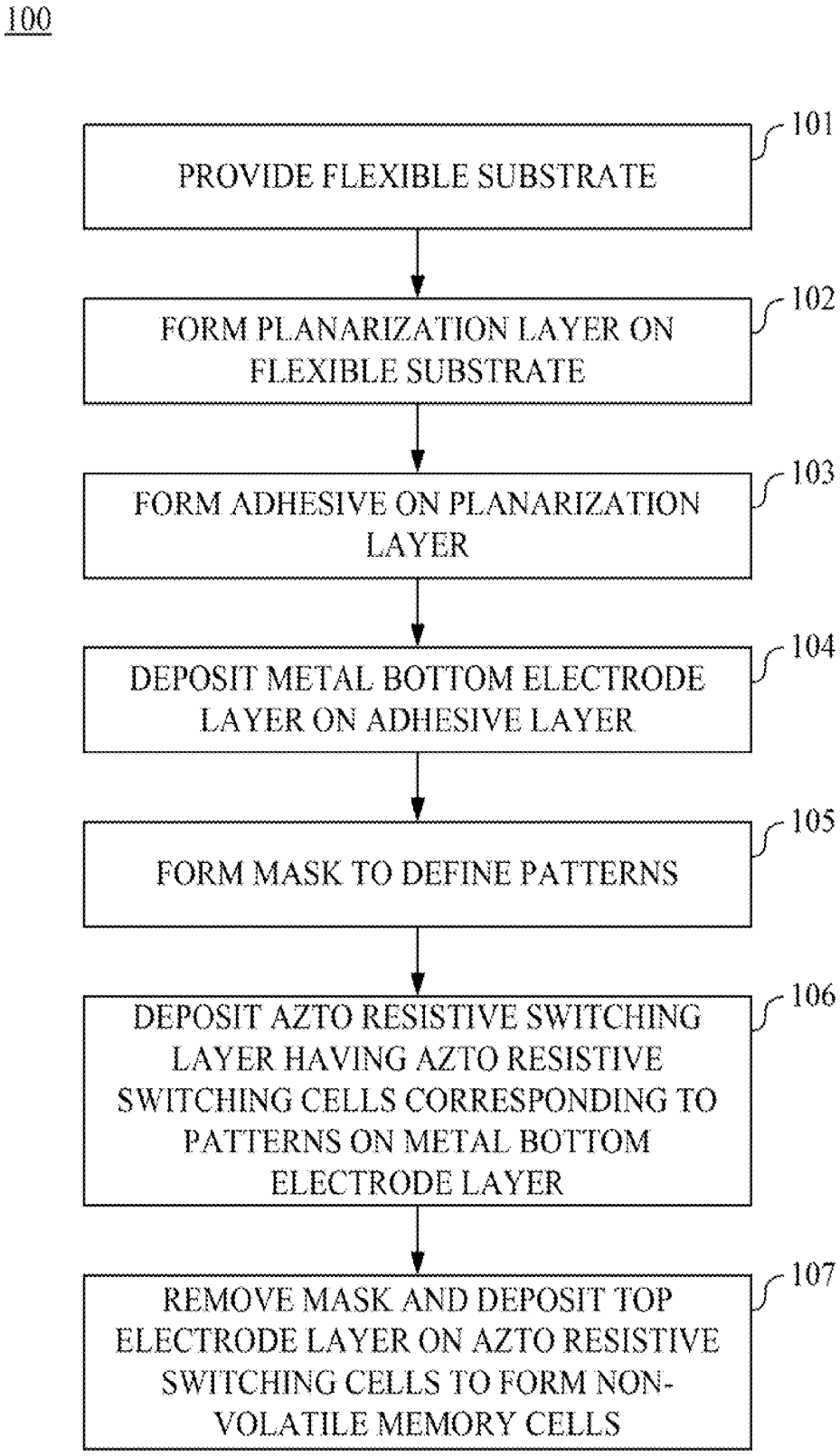

100
PROVIDE FLEXIBLE SUBSTRATE
101
FORM PLANARIZATION LAYER ON FLEXIBLE SUBSTRATE
102
FORM ADHESIVE ON PLANARIZATION LAYER
103
DEPOSIT METAL BOTTOM ELECTRODE LAYER ON ADHESIVE LAYER
104
FORM MASK TO DEFINE PATTERNS
105
DEPOSIT AZTO RESISTIVE SWITCHING LAYER HAVING AZTO RESISTIVE SWITCHING CELLS CORRESPONDING TO PATTERNS ON METAL BOTTOM ELECTRODE LAYER
106
REMOVE MASK AND DEPOSIT TOP ELECTRODE LAYER ON AZTO RESISTIVE SWITCHING CELLS TO FORM NON-VOLATILE MEMORY CELLS
107

FIG. 1

FIG. 2A

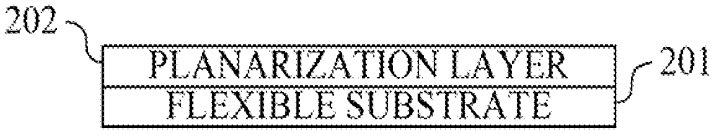


FIG. 2B

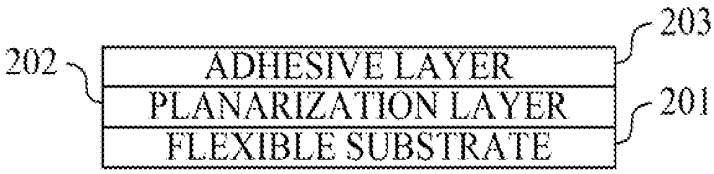


FIG. 2C

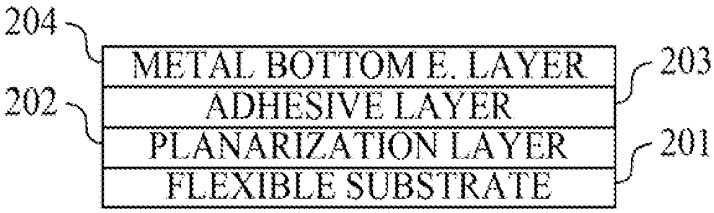


FIG. 2D

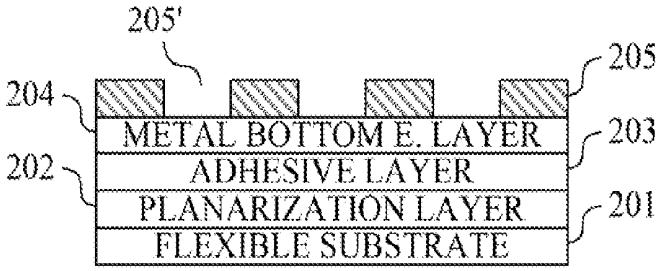


FIG. 2E

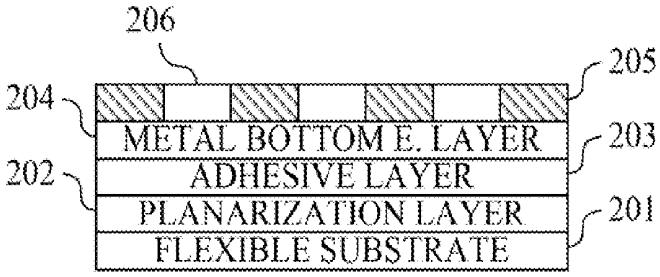


FIG. 2F

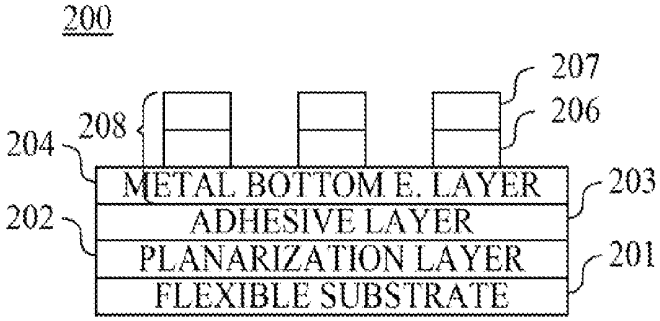


FIG. 2G

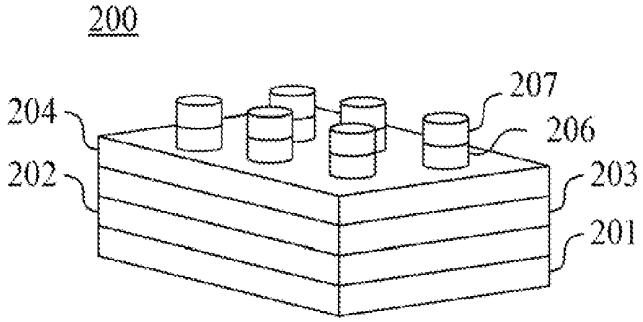


FIG. 2H

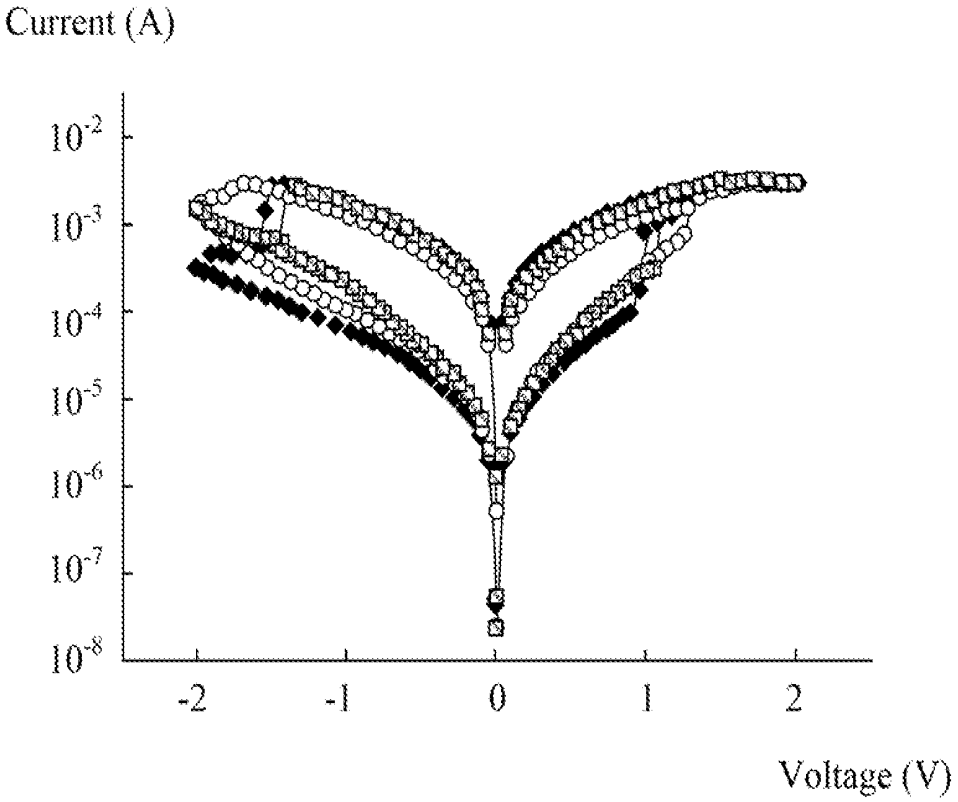


FIG. 3

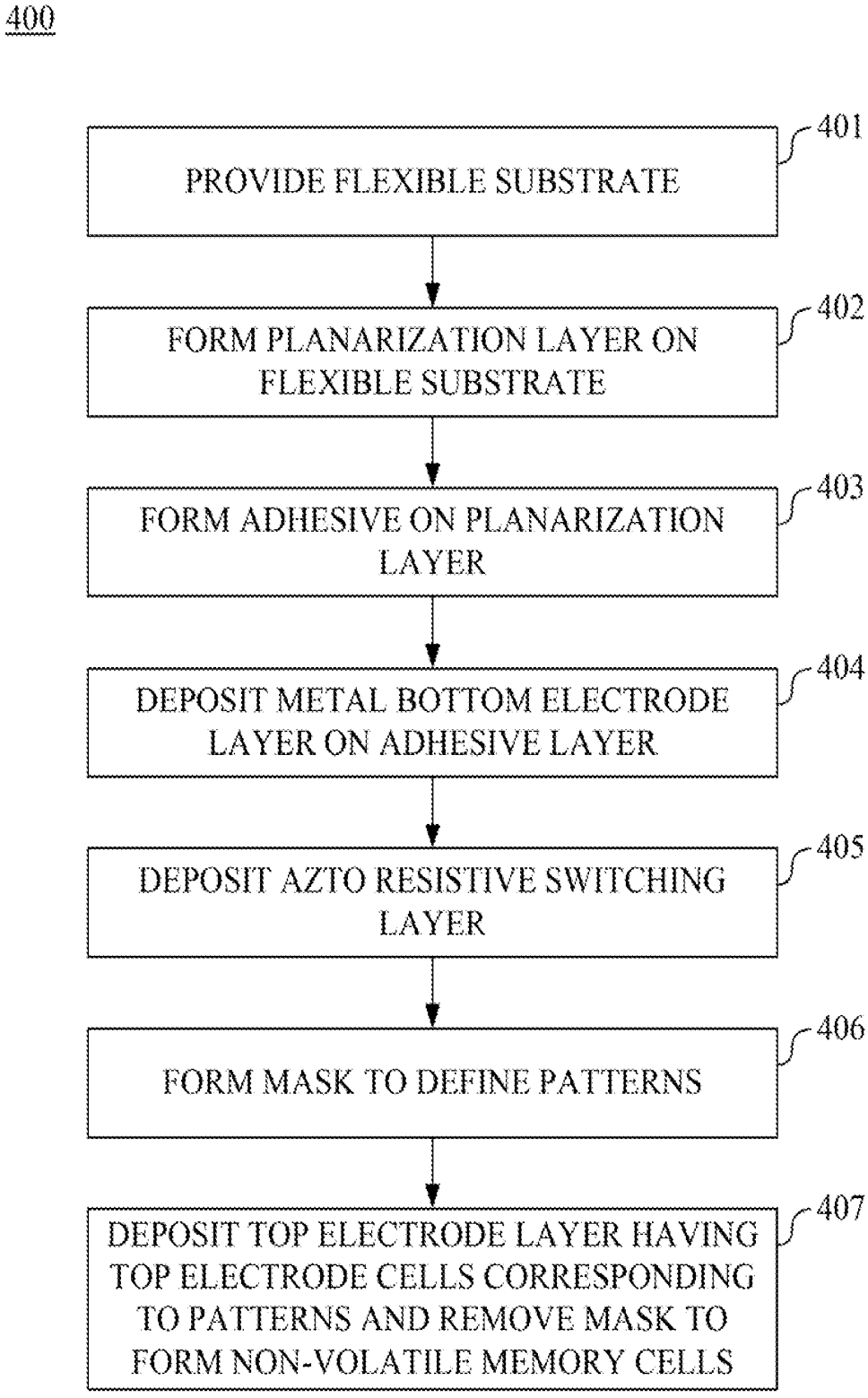

400
PROVIDE FLEXIBLE SUBSTRATE
401
FORM PLANARIZATION LAYER ON FLEXIBLE SUBSTRATE
402
FORM ADHESIVE ON PLANARIZATION LAYER
403
DEPOSIT METAL BOTTOM ELECTRODE LAYER ON ADHESIVE LAYER
404
DEPOSIT AZTO RESISTIVE SWITCHING LAYER
405
FORM MASK TO DEFINE PATTERNS
406
DEPOSIT TOP ELECTRODE LAYER HAVING TOP ELECTRODE CELLS CORRESPONDING TO PATTERNS AND REMOVE MASK TO FORM NON-VOLATILE MEMORY CELLS
407

FIG. 4

FIG. 5A

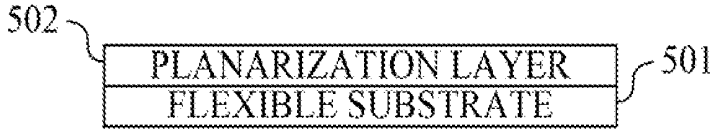


FIG. 5B

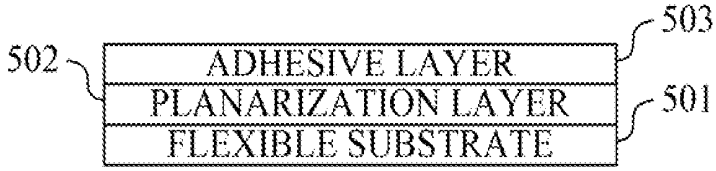


FIG. 5C

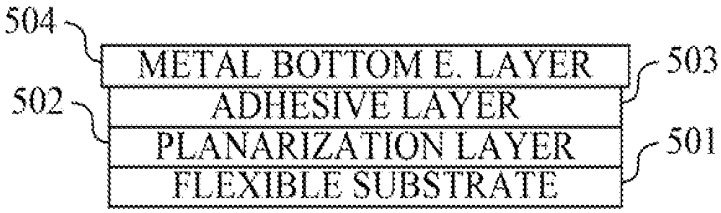


FIG. 5D

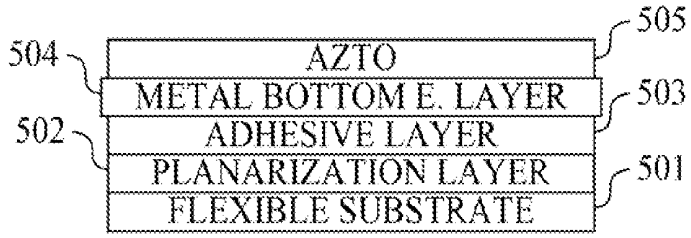


FIG. 5E

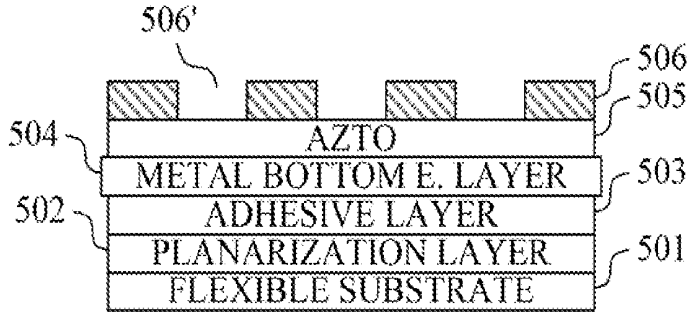


FIG. 5F

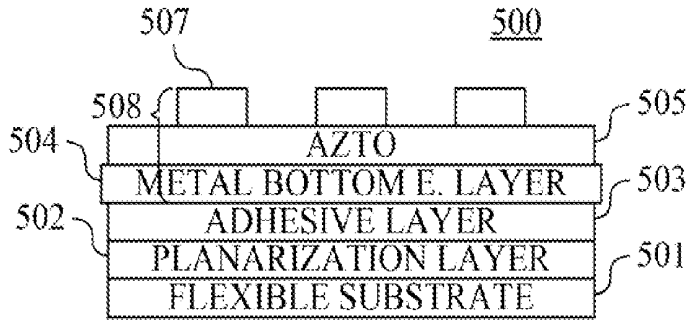


FIG. 5G

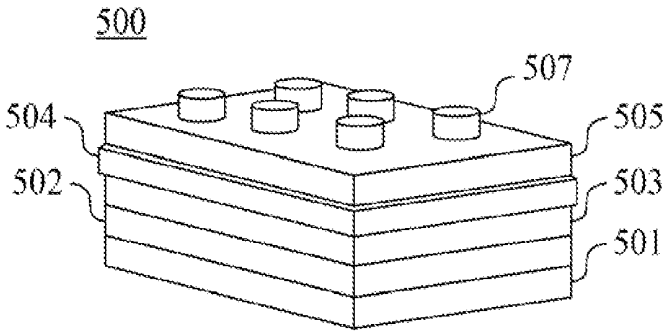


FIG. 5H

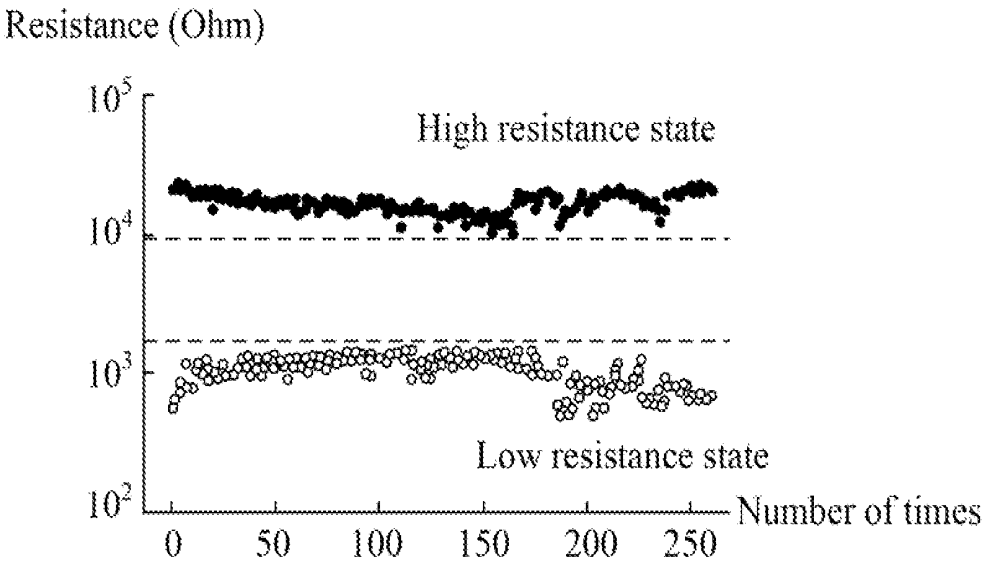

Resistance (Ohm)
10^5
10^4
10^3
10^2
High resistance state
Low resistance state
Number of times
0
50
100
150
200
250

FIG.6

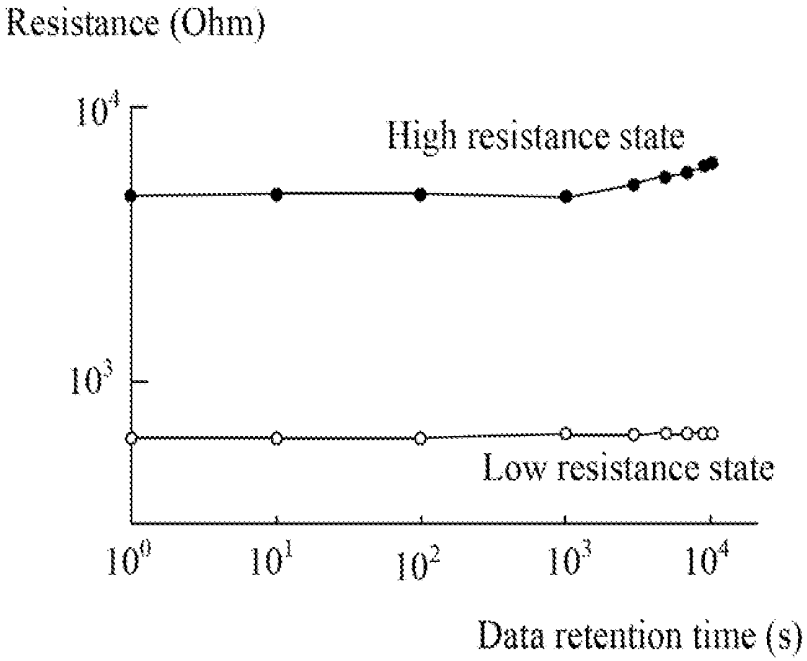

Resistance (Ohm)
10^4
10^3
High resistance state
Low resistance state
10^0
10^1
10^2
10^3
10^4
Data retention time (s)

FIG. 7

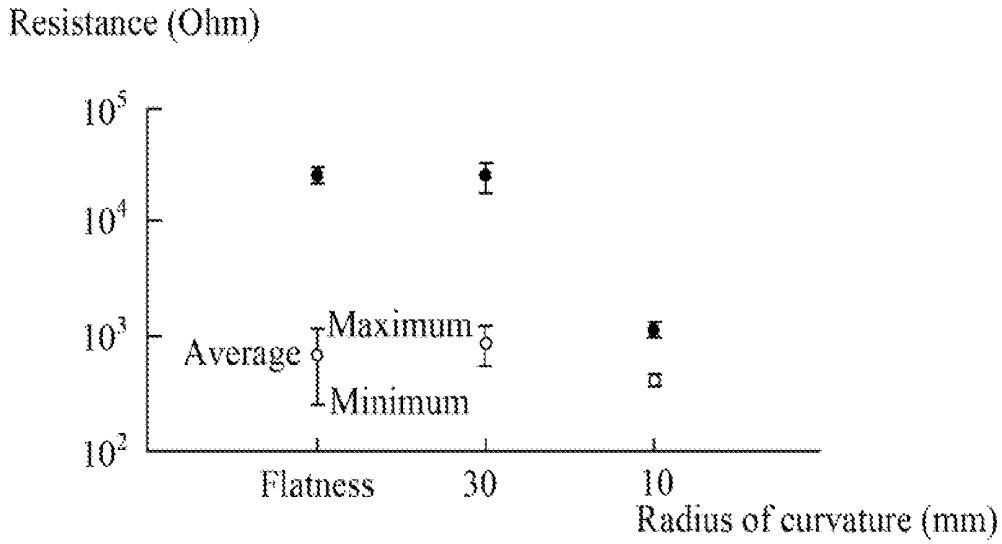

Resistance (Ohm)
10^5
10^4
10^3
10^2
Average
Maximum
Minimum
Flatness
30
10
Radius of curvature (mm)

FIG. 8

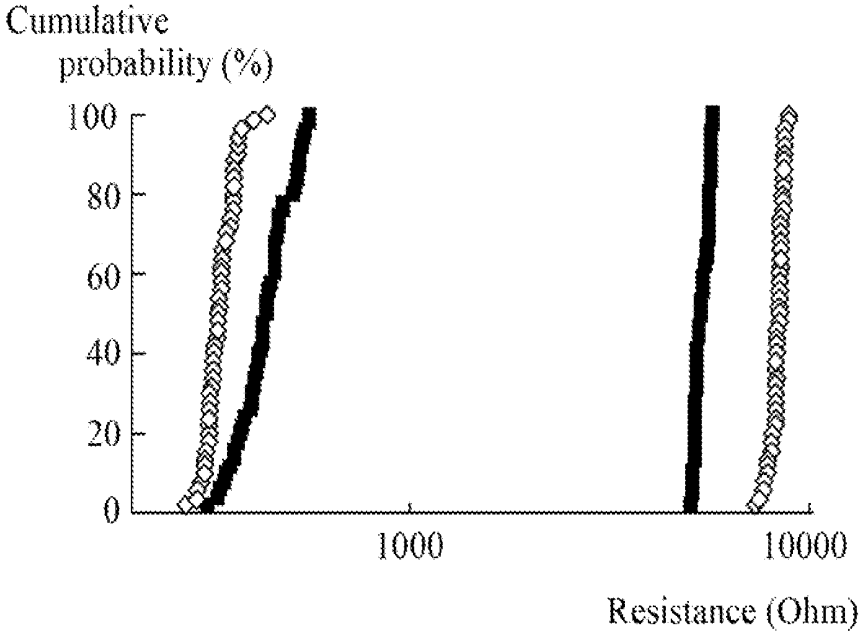

Cumulative probability (%)
100
80
60
40
20
0
1000
10000
Resistance (Ohm)

FIG. 9

FLEXIBLE NON-VOLATILE MEMORY

RELATED APPLICATIONS

[0001] This application claims priority to Taiwan Application Serial Number 101132514 filed Sep. 6, 2012, which is herein incorporated by reference.

BACKGROUND

[0002] 1. Technical Field

[0003] The present disclosure relates to a memory and its manufacturing method. More particularly, the present disclosure relates to a flexible non-volatile memory and a manufacturing method of the same.

[0004] 2. Description of Related Art

[0005] Memory devices can be distinguished into volatile memory devices and non-volatile memory devices, in which the volatile memory devices can be further categorized into DRAM (dynamic random access memory) and SRAM (static random access memory). These memory devices are widely used due to their high access speed. On of the most popular non-volatile memory device is flash memory. However, the shortcomings of the flash memory devices such as high operating voltage, slow rewriting speed, and limited number of rewrites make them unreliable. Further, due to the smaller size of the devices, the gate oxide layer of the flash memory devices becomes thinner and causes larger leakage current. Recently, the resistive non-volatile memory devices gains attention because of their advantages of simple structure, low operating voltage, fast rewriting speed, high applicability to multi-bit applications, good endurance of read/write, small size, non-destructive read operation and low cost.

[0006] In recent years, the development of the resistive non-volatile memory devices is considered as the best candidate for high-density device in the next generation. The common structure used by the resistive non-volatile memory devices is MN (metal layer/intrinsic layer/metal layer). An external bias voltage is used to modify the resistance of the devices to perform the read and the write operations such that the devices can switch between a high resistance state and a low resistance state corresponding to the states of "0" and "1" of the digital signal. The resistive switching layer formed by the metal oxide is the most important and the most studied part of the resistive non-volatile memory devices. However, flexible electronic devices gain more and more popularity. The material and the design of the resistive non-volatile memory devices have to be well selected and well-designed in order to make the resistive switching layer have a good endurance under the circumstances of frequent switches between different resistance states and frequent bending of the devices.

[0007] Accordingly, what is needed is a flexible non-volatile memory and a manufacturing method of the same to accomplish the

SUMMARY

[0008] An aspect of the present invention is to provide a manufacturing method for manufacturing a flexible non-volatile memory. The manufacturing method comprises the steps outlined below. A flexible substrate is provided. A planarization layer is formed on the flexible substrate. A metal bottom electrode layer is deposited on the planarization layer. A mask is formed to define a plurality of patterns. An AZTO (aluminum zinc tin oxide) resistive switching layer having a plurality of electrically independent AZTO resistive switching cells corresponding to the patterns is deposited on the metal bottom electrode layer. The mask is removed and a top electrode layer is deposited on the AZTO resistive switching layer corresponding to the AZTO resistive switching cells to form a plurality of non-volatile memory cells.

[0009] Another aspect of the present invention is to provide a manufacturing method for manufacturing a flexible non-volatile memory. The manufacturing method comprises the steps outlined below. A flexible substrate is provided. A planarization layer is formed on the flexible substrate. A metal bottom electrode layer is deposited on the planarization layer. An AZTO resistive switching layer is deposited on the metal bottom electrode layer. A mask is formed to define a plurality of patterns. A top electrode layer having a plurality of electrically independent top electrode cells corresponding to the patterns is deposited on the AZTO resistive switching layer and removing the mask to form a plurality of non-volatile memory cells.

[0010] Yet another aspect of the present invention is to provide a flexible non-volatile memory. The flexible non-volatile memory comprises a flexible substrate; a planarization layer, a metal bottom electrode layer, an AZTO resistive switching layer and a top electrode layer. The planarization layer is formed on the flexible substrate. The metal bottom electrode layer is deposited on the planarization layer. The AZTO resistive switching layer having a plurality of electrically independent AZTO resistive switching cells is formed on the metal bottom electrode layer. The top electrode layer is formed on the AZTO resistive switching layer corresponding to the AZTO resistive switching cells to form a plurality of non-volatile memory cells.

[0011] Further another aspect of the present invention is to provide a flexible non-volatile memory. The flexible non-volatile memory comprises a flexible substrate; a planarization layer, a metal bottom electrode layer, an AZTO resistive switching layer and a top electrode layer. The planarization layer is formed on the flexible substrate. The metal bottom electrode layer is deposited on the planarization layer. The AZTO resistive switching layer is formed on the metal bottom electrode layer. The top electrode layer having a plurality of electrically independent top electrode cells is formed on the AZTO resistive switching layer to form a plurality of non-volatile memory cells.

[0012] It is to be understood that both the foregoing general description and the following detailed description are by examples, and are intended to provide further explanation of the disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The disclosure can be more fully understood by reading the following detailed description of the embodiment, with reference made to the accompanying drawings as follow

[0014] FIG. **1** is a flow chart of a manufacturing method for manufacturing a flexible non-volatile memory in an embodiment of the present disclosure;

[0015] FIG. **2**A to FIG. **2**G are cross-sectional views of the flexible non-volatile memory corresponding to the steps of the manufacturing method in an embodiment of the present disclosure;

[0016] FIG. **2**H is a 3-D (three dimensional) view of the flexible non-volatile memory in an embodiment of the present disclosure;

[0017] FIG. **3** is a diagram depicting the relation between the voltage and the current when a bias voltage within 2V is applied to the metal bottom electrode layer and the top electrode layer of the flexible non-volatile memory;

[0018] FIG. **4** is a flow chart of a manufacturing method for manufacturing a flexible non-volatile memory in an embodiment of the present disclosure;

[0019] FIG. **5**A to FIG. **5**G are cross-sectional views of the flexible non-volatile memory corresponding to the steps of the manufacturing method in an to embodiment of the present disclosure;

[0020] FIG. **5**H is a 3-D view of the flexible non-volatile memory in an embodiment of the present disclosure;

[0021] FIG. **6** is a diagram depicting the relation between the number of times of continuous switching of the resistance states and the resistance of the flexible non-volatile memory in an embodiment of the present invention;

[0022] FIG. **7** is a diagram depicting the relation between the data retention time and the resistance of the flexible non-volatile memory in an embodiment of the present invention;

[0023] FIG. **8** is a diagram depicting the relation between the radius of curvature and the resistance of the flexible non-volatile memory in an embodiment of the present invention; and

[0024] FIG. **9** is a diagram depicting the relation between the resistance and the cumulative probability of the flexible non-volatile memory in an embodiment of the present invention.

DETAILED DESCRIPTION

[0025] Reference will now be made in detail to the present embodiments of the disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0026] FIG. **1** is a flow chart of a manufacturing method **100** for manufacturing a flexible non-volatile memory in an embodiment of the present disclosure. FIG. **2**A to FIG. **2**G are cross-sectional views of the flexible non-volatile memory corresponding to the steps of the manufacturing method **100** in an embodiment of the present disclosure.

[0027] Please refer to FIG. **1** and FIG. **2**A at the same time. In step **101**, a flexible substrate **201** is provided. In an embodiment, the material of the flexible substrate **201** is stainless steel or plastic. The flexible substrate **201** can be bent to different radius of curvature when different magnitudes of force are applied. Further, the flexible substrate **201** can be bounced back to the original state when there is no force applied and is suitable in the manufacturing of the flexible electronic devices.

[0028] Please refer to FIG. **1** and FIG. **2**B at the same time. In step **102**, a planarization layer **202** is formed on the flexible substrate **201**. In an embodiment, the material of the planarization layer is SiO_2 to guarantee the flatness of the surface of the flexible substrate **201**.

[0029] Please refer to FIG. **1** and FIG. **2**C at the same time. In step **103**, an adhesive layer **203** is formed on the planarization layer **202**. In an embodiment, the material of the adhesive layer **203** is metal oxide such as TiO_2. In some embodiments, the adhesive layer **203** can be directly formed by metal, e.g. Ti. The adhesive layer **203** provides better adhesion to the metal layer formed subsequently. In an embodiment, the memory device can he manufactured without forming the adhesive layer **203** such that the metal layer is formed directly on the planarization layer **202**. However, the adhesion of the metal layer to the planarization layer **202** is worse due to the absence of the adhesive layer **203**.

[0030] Please refer to FIG. **1** and FIG. **2**D at the same time. In step **104**, a metal bottom electrode layer **204** (shown as METAL BOTTOM E. LAYER in FIG. **2**D and subsequent figures) is deposited on the planarization layer **203**. In an embodiment, the material of the metal bottom electrode layer **204** is Au or Pt. The metal bottom electrode layer **204** can be deposited on the planarization layer **203** by physical vapor deposition processes such as the electron beam evaporation process or other possible manufacturing processes.

[0031] Please refer to FIG. **1** and FIG. **2**E at the same time. In step **105**, a mask **205** formed to define a plurality of patterns **205'**.

[0032] Please refer to FIG. **1** and FIG. **2**F at the same time. In step **106**, an AZTO (aluminum zinc tin oxide) resistive switching layer having a plurality of electrically independent AZTO resistive switching cells **206** corresponding to the patterns **205'** is deposited on the metal bottom electrode layer **204**. AZTO is a transparent amorphous oxide semiconductor device that can be deposited at low temperature (under **100** degrees Celsius). Further, AZTO has the characteristic of excellent uniformity. The AZTO resistive switching layer can be deposited on the metal bottom electrode layer **204** by physical vapor deposition processes such as the plasma sputtering process or other possible manufacturing processes.

[0033] Please refer to FIG. **1** and FIG. **2**G at the same time. In step **107**, the mask **205** is removed and a top electrode layer **207** is deposited on the AZTO resistive switching layer corresponding to the AZTO resistive switching cells **206** to form a plurality of non-volatile memory cells **208** to finish the manufacturing process of the flexible non-volatile memory **200**. The final structure is as shown in FIG. **2**H, in which FIG. **2**H is a 3-D (three dimensional) view of the flexible non-volatile memory **200**. In an embodiment, the material of the top electrode layer **207** is Ti, TiN or ITO. The top electrode layer **207** can be deposited on the AZTO resistive switching layer by physical vapor deposition processes such as the plasma sputtering process or other possible manufacturing processes.

[0034] FIG. **3** is a diagram depicting the relation between the voltage and the current when a bias voltage within **2**V is applied to the metal bottom electrode layer **204** and the top electrode layer **207** of the flexible non-volatile memory **200**. It is noted that the curve formed by the diamond-shaped points is generated according to the first time set and reset procedure. The curve formed by the round-shaped points is generated according to the condition of the 100th time of the set and reset procedure. The curve formed by the square-shaped points is generated according to the condition of the 200th set and reset procedure.

[0035] As shown in FIG. **3**, after a positive bias voltage is applied to the metal bottom electrode layer **204** and the top electrode layer **207**, the current that flows through the AZTO resistive switching cells **206** increases rapidly when Vset is applied since the device switches to the low resistance state. After a negative bias voltage is applied to the metal bottom electrode layer **204** and the top electrode layer **207**, the current that flows through the AZTO resistive switching cells **206** decreases rapidly when Vreset is applied since the device switches to the high resistance state. Hence, the AZTO resistive switching cells **206** can switch between the states of "1"

and "0". Since the states is defined according to the resistance of the AZTO resistive switching cells **206**, they are called resistive memory devices.

[0036] Consequently, the steps described above can be used to form the flexible non-volatile memory. The AZTO can be used as the replacement of In and Ga since they are in great demand for use in the manufacturing process of the memory devices. Further, AZTO has great characteristics of the memory and can be fabricated in low temperature circumstance (under 100 degrees Celsius).

[0037] FIG. **4** is a flow chart of a manufacturing method **400** for manufacturing a flexible non-volatile memory in an embodiment of the present disclosure. FIG. **5**A to FIG. **5**G are cross-sectional views of the flexible non-volatile memory corresponding to the steps of the manufacturing method **400** in an embodiment of the present disclosure.

[0038] Please refer to FIG. **4** and FIG. **5**A at the same time. In step **401**, a flexible substrate **501** is provided. In an embodiment, the material of the flexible substrate **501** is stainless steel or plastic. The flexible substrate **501** can be bent to different radius of curvature when different magnitudes of force are applied. Further, the flexible substrate **501** can be bounced back to the original state when there is no force applied and is suitable in the manufacturing of the flexible electronic devices.

[0039] Please refer to FIG. **4** and FIG. **5**B at the same time. In step **402**, a planarization layer **502** is formed on the flexible substrate **501**. In an embodiment, the material of the planarization layer is SiO_2 to guarantee the flatness of the surface of the flexible substrate **501**.

[0040] Please refer to FIG. **4** and FIG. **5**C at the same time. In step **403**, an adhesive layer **503** is formed on the planarization layer **502**. In an embodiment, the material of the adhesive layer **503** is metal oxide such as TiO_2. In some embodiments, the adhesive layer **503** can be directly formed by metal, e.g. Ti The adhesive layer **503** provides better adhesion to the metal layer formed subsequently. In an embodiment, the memory device can be manufactured without forming the adhesive layer **503** such that the metal layer is formed directly on the planarization layer **502**. However, the adhesion of the metal layer to the planarization layer **502** is worse due to the absence of the adhesive layer **503**

[0041] Please refer to FIG. **4** and FIG. **5**D at the same time. In step **404**, a metal bottom electrode layer **504** (shown as METAL BOTTOM E. LAYER in FIG. **2**D and subsequent figures) is deposited on the planarization layer **503**. In an embodiment, the material of the metal bottom electrode layer **504** is Au or Pt. The metal bottom electrode layer **504** can be deposited on the planarization layer **503** by physical vapor deposition processes such as the electron beam evaporation process or other possible manufacturing processes.

[0042] Please refer to FIG. **4** and FIG. **5**E at the same time. In step **405**, an AZTO (aluminum zinc tin oxide) resistive switching layer **505** is deposited on the metal bottom electrode layer **404**. AZTO is a transparent amorphous oxide semiconductor device that can be deposited at low temperature (under 100 degrees Celsius). Further, AZTO has the characteristic of excellent uniformity. The AZTO resistive switching layer **505** can be deposited on the metal bottom electrode layer **504** by physical vapor deposition processes such as the plasma sputtering process or other possible manufacturing processes.

[0043] Please refer to FIG. **4** and FIG. **5**F at the same time. In step **406**, a mask **506** is formed to define a plurality of patterns **506'**.

[0044] Please refer to FIG. **4** and FIG. **5**G at the same time. In step **507**, a top electrode layer having a plurality of electrically independent top electrode cells **507** corresponding to the patterns **506'** on the AZTO resistive switching layer **505** and the mask **506** is removed to form a plurality of non-volatile memory cells to finish the manufacturing process of the flexible non-volatile memory **500**. The final structure is as shown in FIG. **5**H, in which. FIG. **5**H is a 3-D (three dimensional) view of the flexible non-volatile memory **500**. In an embodiment, the material of the top electrode layer is Ti TiN or ITO. The top electrode layer can be deposited on the AZTO resistive switching layer **505** by physical vapor deposition processes such as the plasma sputtering process or other possible manufacturing processes.

[0045] Hence, a flexible non-volatile memory having the similar voltage and current characteristics as shown in FIG. **3** can be manufactured by the manufacturing method **400**. It is noted that in some embodiments, the width of the bottom electrode layer **504** can be slightly larger than the width of the adhesive layer **503** and the AZTO resistive switching layer **505** as shown in FIG. **5**G in order to measure the voltage of the device or apply the voltage on the device.

[0046] FIG. **6** is a diagram depicting the relation between the number of times of continuous switching of the resistance states and the resistance of the flexible non-volatile memory **200** or **500** in an embodiment of the present invention. The continuous switching of the resistance states is applied to the flexible non-volatile memory **200** or **500** for endurance test. As shown in FIG. **6**, the ratio of the average resistance between the high resistance state and the low resistance is over 18 even after at least 256 times of switching. Accordingly, the flexible non-volatile memory **200** or **500** can maintain the characteristic of memory and the performance is not degraded due to the continuous switching.

[0047] FIG. **7** is a diagram depicting the relation between the data retention time and the resistance of the flexible non-volatile memory **200** or **500** in an embodiment of the present invention. As shown in FIG. **7**, an external read voltage of 200 mV is applied continuously to the flexible non-volatile memory **200** or **500** in the high resistance state and in the low resistance state respectively. The device is in a circumstance of 300K temperature for measuring its resistance. It is obvious that the data retention characteristic can be maintained in at least 10^4 seconds.

[0048] FIG. **8** is a diagram depicting the relation between the radius of curvature and the resistance of the flexible non-volatile memory **200** or **500** in an embodiment of the present invention. As shown in FIG. **8**, under the conditions of different radius of curvature including 0 mm (i.e. non-bent), 30 mm and 10 mm (the smaller the radius of curvature is, the more the device is bent), the resistance of the device is measured after 100 times of continuous switching between the high resistance state and the low resistance state. The measured resistance is represented by a maximum, an average and a minimum. It is obvious that the flexible non-volatile memory **200** or **500** can maintain the characteristic of memory and therefore can be used in flexible electronics.

[0049] FIG. **9** is a diagram depicting the relation between the resistance and the cumulative probability of the flexible non-volatile memory **200** or **500** in an embodiment of the present invention. In FIG. **9**, the curve formed by the dia-

mond-shaped points is generated according to the flexible non-volatile memory **200** or **500** that no bending endurance test is applied. The curve formed by the square-shaped points is generated according to the flexible non-volatile memory **200** or **500** after 5000 times of repetitive bending and straightening. It is obvious that the flexible non-volatile memory **200** or **500** can maintain the characteristic of memory even after 5000 times of repetitive bending and straightening.

[0050] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present disclosure without departing from the scope or spirit of the disclosure. In view of the foregoing, it is intended that the present disclosure cover modifications and variations of this disclosure provided they fall within the scope of the following claims.

What is claimed is:

1. A manufacturing method for manufacturing a flexible non-volatile memory comprising:

providing a flexible substrate;

forming a planarization layer on the flexible substrate;

depositing a metal bottom electrode layer on the planarization layer;

forming a mask to define a plurality of patterns;

depositing an AZTO (aluminum zinc tin oxide) resistive switching layer having a plurality of electrically independent AZTO resistive switching cells corresponding to the patterns on the metal bottom electrode layer; and

removing the mask and depositing a top electrode layer on the AZTO resistive switching layer corresponding to the AZTO resistive switching cells to form a plurality of non-volatile memory cells

2. The manufacturing method of claim **1**, wherein a material of the flexible substrate is stainless steel or plastic.

3. The manufacturing method of claim wherein a material of the planarization layer is SiO_2.

4. The manufacturing method of claim further comprising forming an adhesive layer on the planarization layer and the metal bottom electrode layer is actually formed on the adhesive layer.

5. The manufacturing method of claim **4**, wherein a material of the adhesive layer is TiO_2.

6. The manufacturing method of claim **1**, wherein a material of the metal bottom electrode layer is Au or Pt and a material of the top electrode layer is Ti, TiN or ITO.

7. The manufacturing method of claim **1**, wherein the manufacturing method is performed under 100 degrees Celsius.

8. A manufacturing method for manufacturing a flexible non-volatile memory comprising:

providing a flexible substrate;

forming a planarization layer on the flexible substrate;

depositing a metal bottom electrode layer on the planarization layer;

depositing an AZTO resistive switching layer on the metal bottom electrode layer;

forming a mask to define a plurality of patterns; and

depositing a top electrode layer having a plurality of electrically independent top electrode cells corresponding to the patterns on the AZTO resistive switching layer and removing the mask to form a plurality of non-volatile memory cells.

9. The manufacturing method of claim **8**, wherein the manufacturing method is performed under 100 degrees Celsius.

10. The manufacturing method of claim **8**, further comprising forming an adhesive layer on the planarization layer and the metal bottom electrode layer is actually formed on the adhesive layer.

11. A flexible non-volatile memory comprising:

a flexible substrate;

a planarization layer formed on the flexible substrate;

a metal bottom electrode layer deposited on the planarization layer;

to an AZTO resistive switching layer having a plurality of electrically independent AZTO resistive switching cells formed on the metal bottom electrode layer; and

a top electrode layer formed on the AZTO resistive switching layer corresponding to the AZTO resistive switching cells to form a plurality of non-volatile memory cells.

12. The flexible non-volatile memory of claim **11** wherein a material of the flexible substrate is stainless steel or plastic.

13. The flexible non-volatile memory of claim **11**, wherein a material of the planarization layer is SiO_2.

14. The flexible non-volatile memory of claim **11**, further comprising an adhesive layer on the planarization layer and the metal bottom electrode layer is actually formed on the adhesive layer.

15. The flexible non-volatile memory of claim **14**, wherein a material of the adhesive layer is TiO_2.

16. The flexible non-volatile memory of claim **11**, wherein a material of the metal bottom electrode layer s Au or Pt and a material of the top electrode layer is Ti, TiN or ITO.

17. A flexible non-volatile memory comprising:

a flexible substrate:

a planarization layer formed on the flexible substrate:

a metal bottom electrode layer deposited on the planarization layer:

an AZTO resistive switching layer formed on the metal bottom electrode layer; and

a top electrode layer having a plurality of electrically independent top electrode cells on the AZTO resistive switching layer to form a plurality of non-volatile memory cells.

18. The flexible non-volatile memory of claim **17**, further comprising an adhesive layer on the planarization layer and the metal bottom electrode layer is actually formed on the adhesive layer.

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