



US 20130140647A1

(19) **United States**

(12) **Patent Application Publication**
CHANG et al.

(10) **Pub. No.: US 2013/0140647 A1**

(43) **Pub. Date: Jun. 6, 2013**

(54) **III-V METAL-OXIDE-SEMICONDUCTOR
DEVICE**

(22) Filed: **Feb. 4, 2013**

Related U.S. Application Data

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(63) Continuation-in-part of application No. 12/849,025,
filed on Aug. 3, 2010.

Publication Classification

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(51) **Int. Cl.**
H01L 29/78 (2006.01)

(52) **U.S. Cl.**
CPC **H01L 29/78** (2013.01)
USPC **257/411**

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(57) **ABSTRACT**

A hafnium oxide layer, between a III-V semiconductor layer
and a metal oxide layer is used to prevent interaction between
the III-V semiconductor layer and the metal oxide layer.

(21) Appl. No.: **13/757,861**

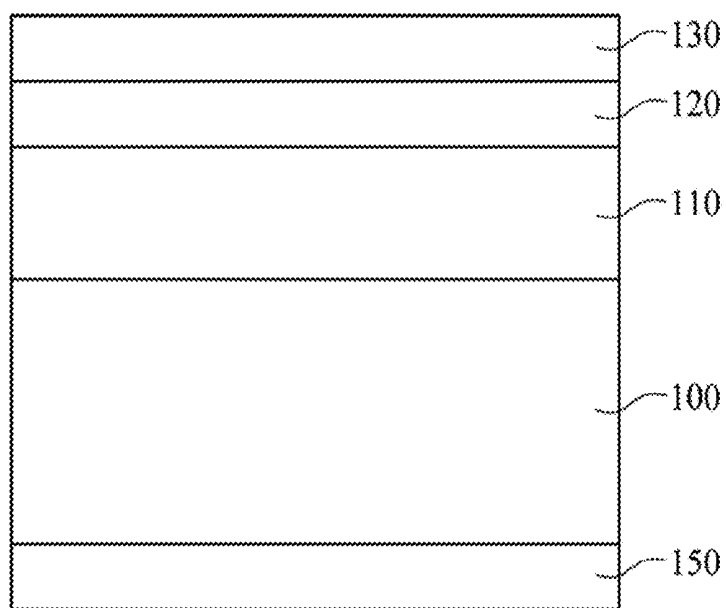


Fig. 1

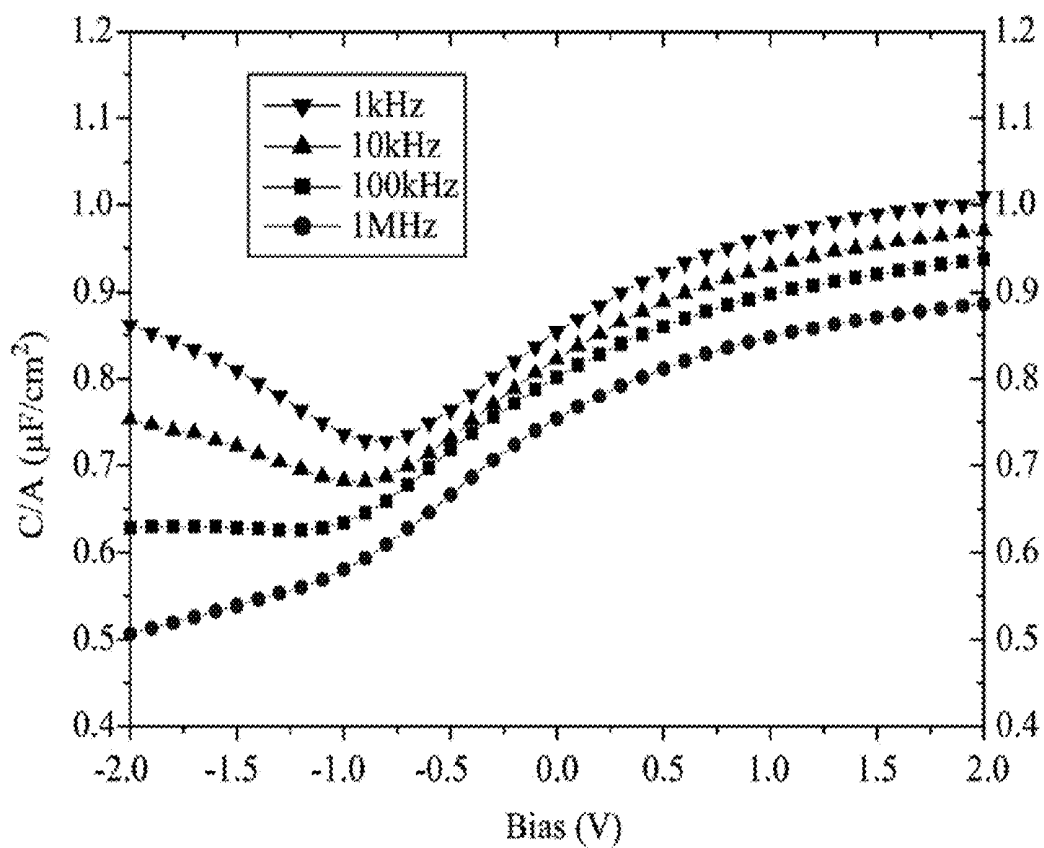


Fig. 2

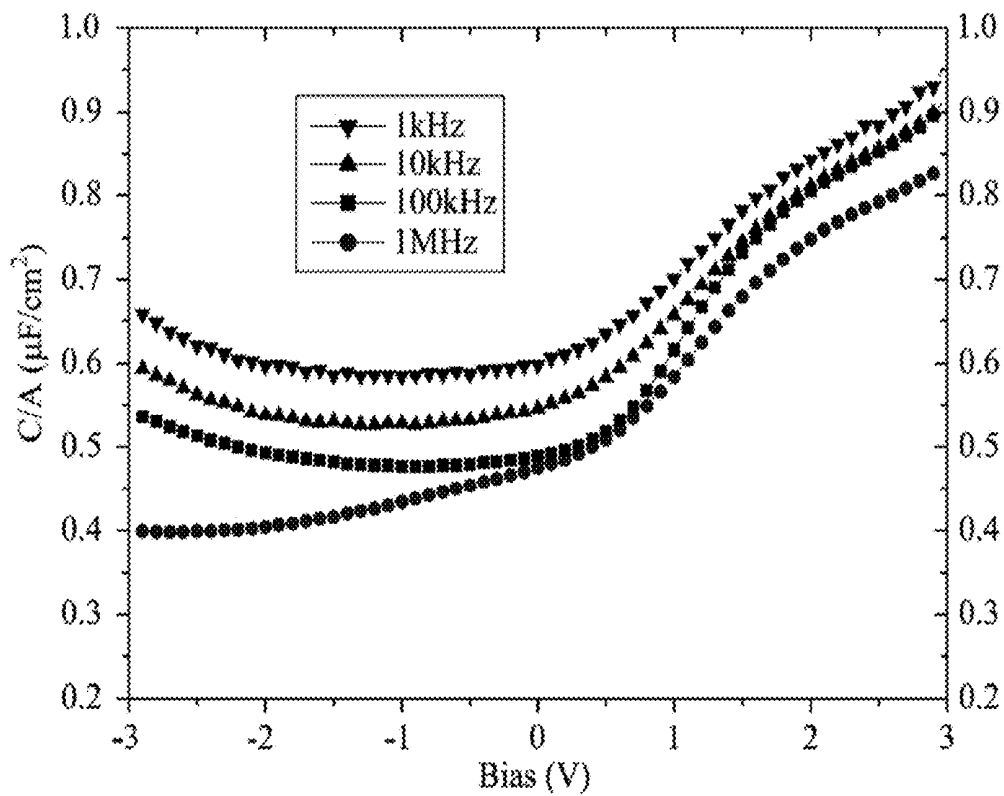


Fig. 3A

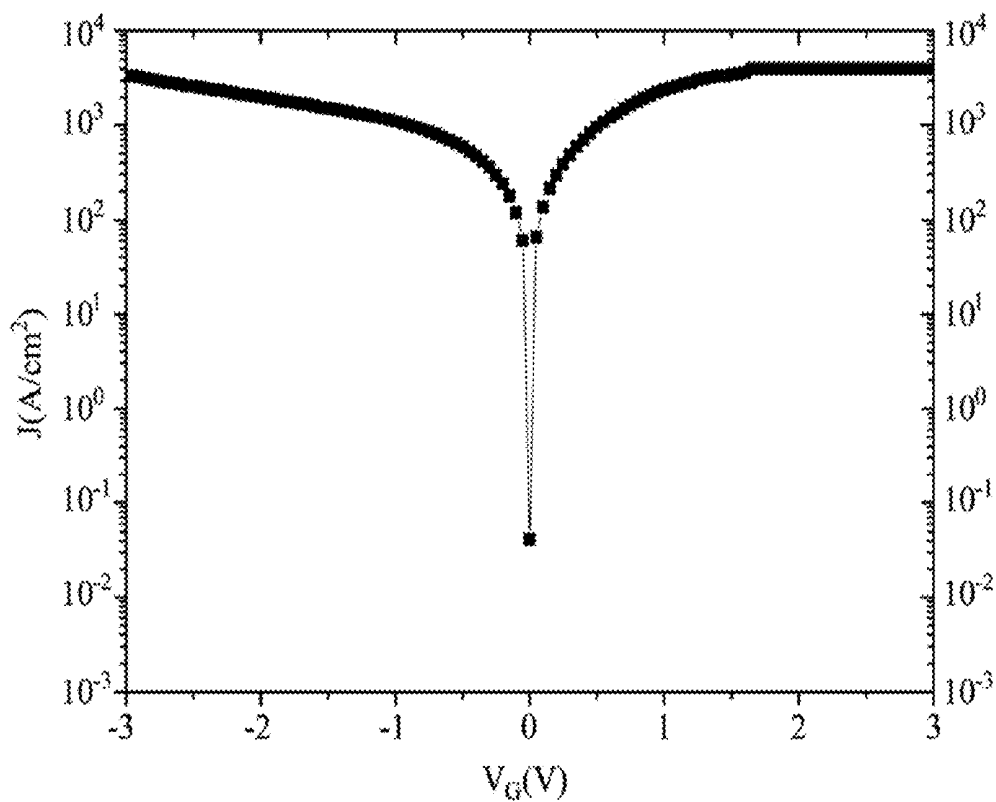


Fig. 3B

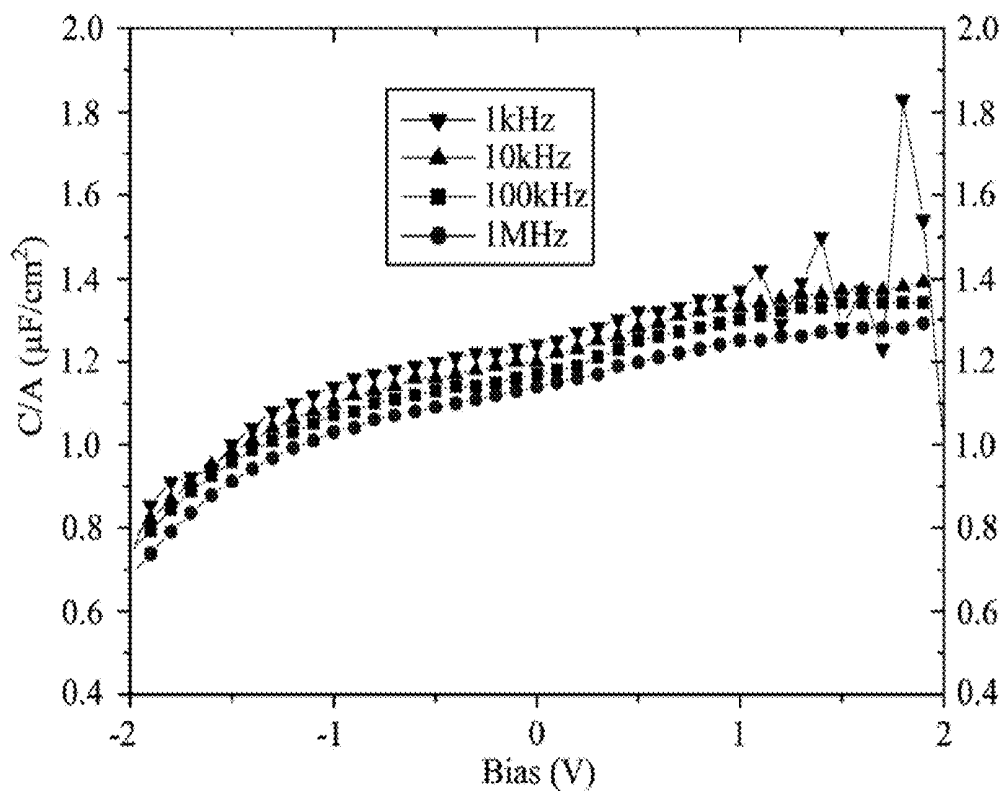


Fig. 4A

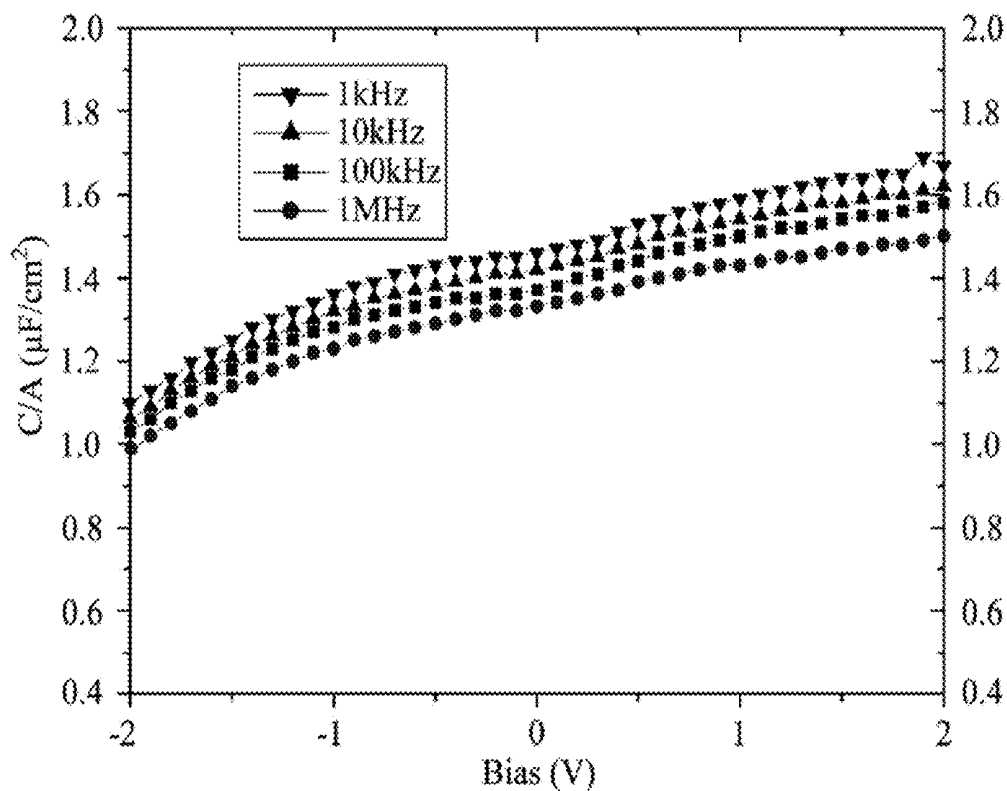


Fig. 4B

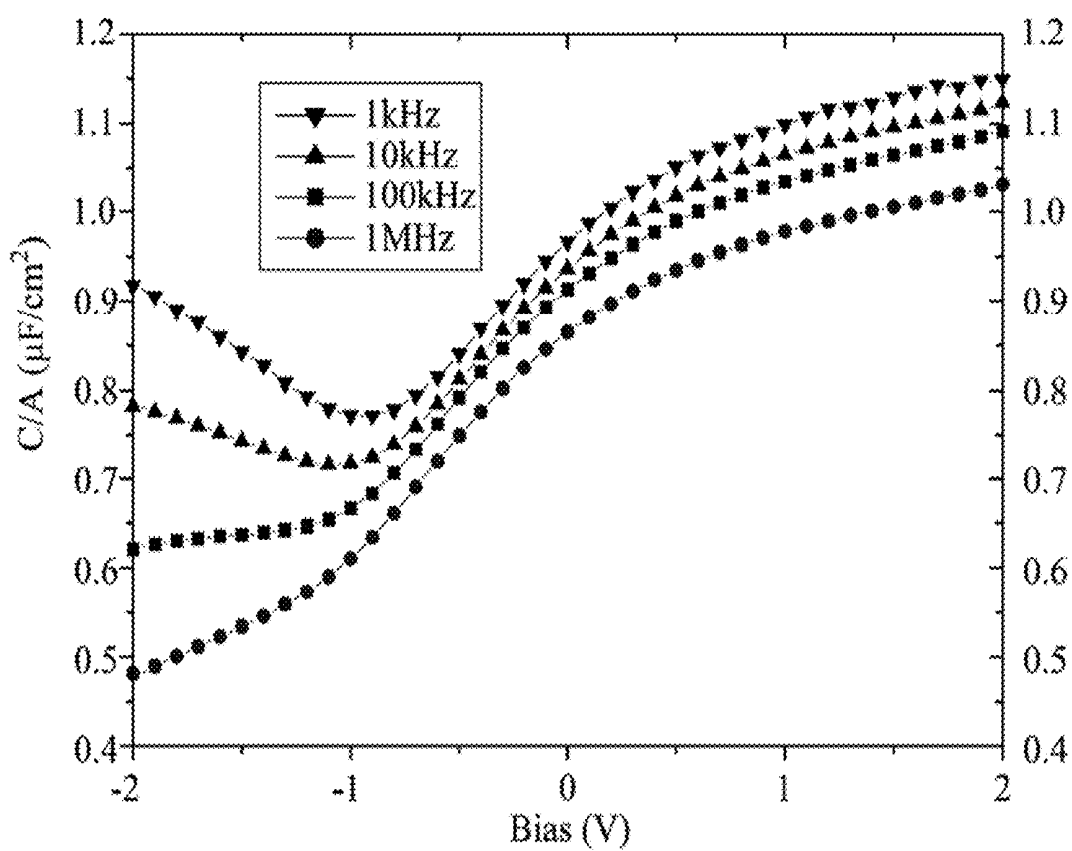


Fig. 4C

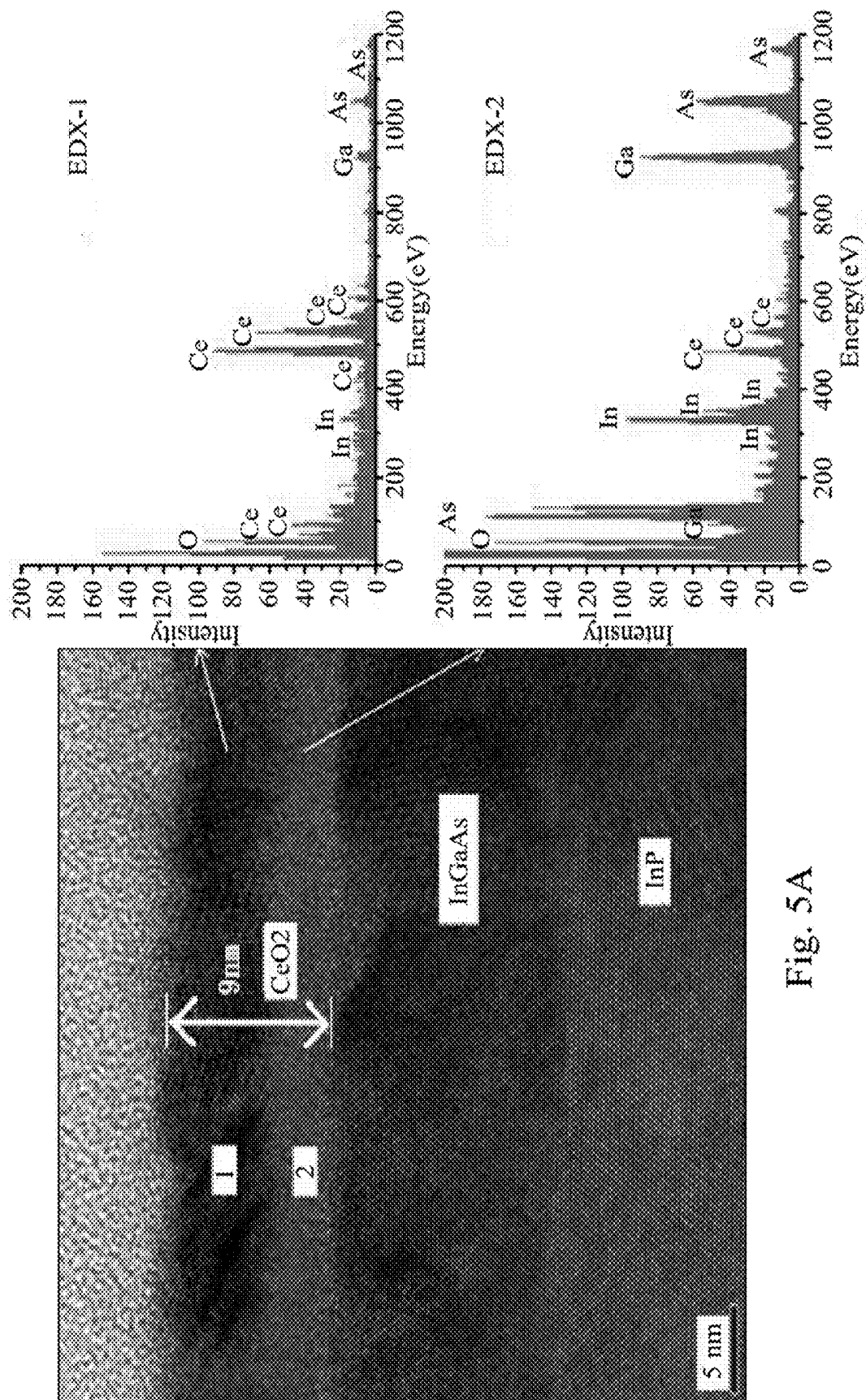


Fig. 5A

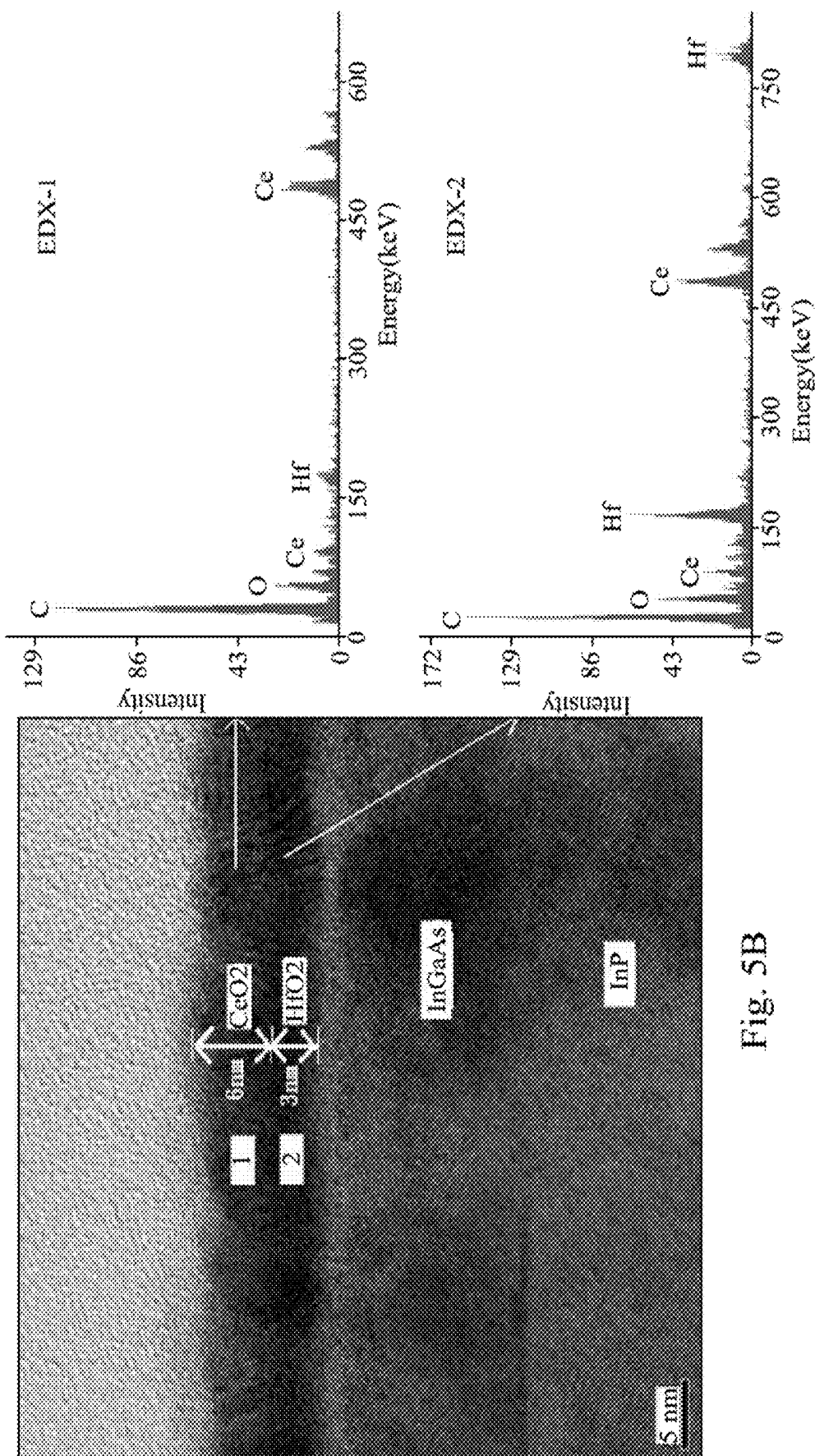


Fig. 5B

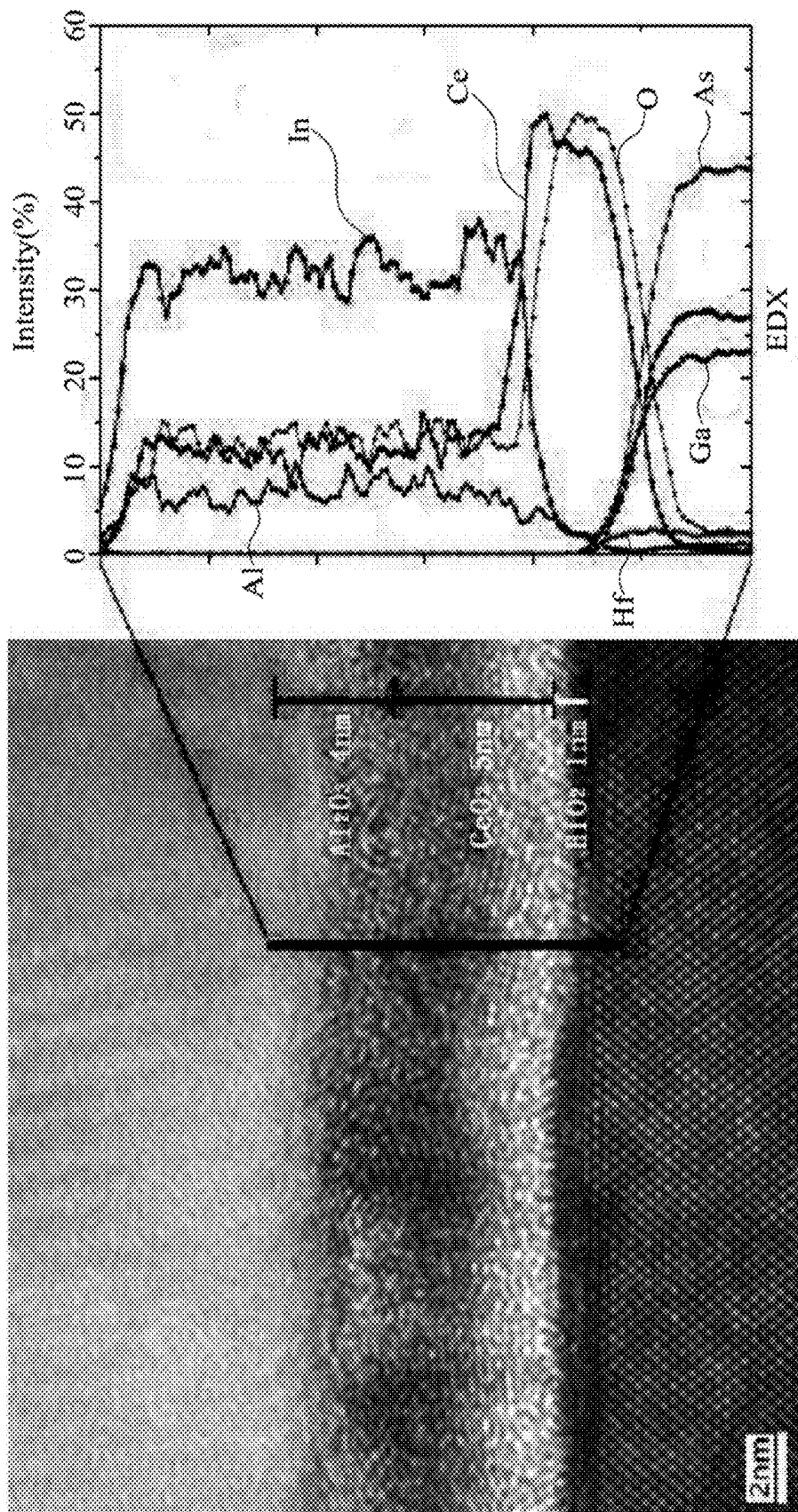


Fig. 5C

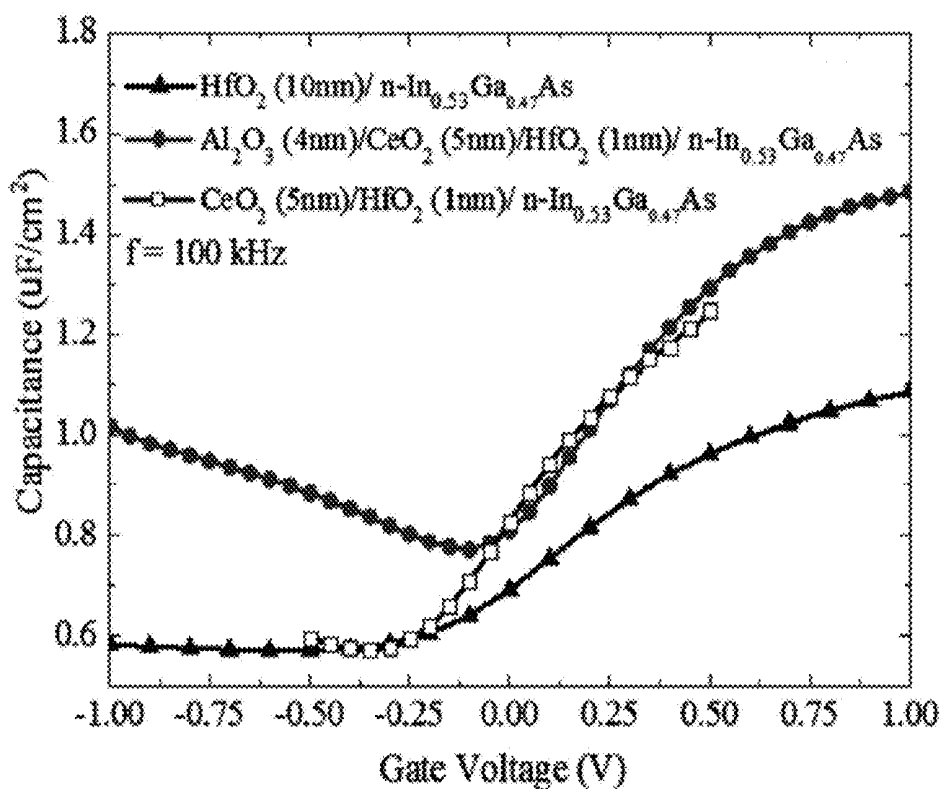


Fig. 6A

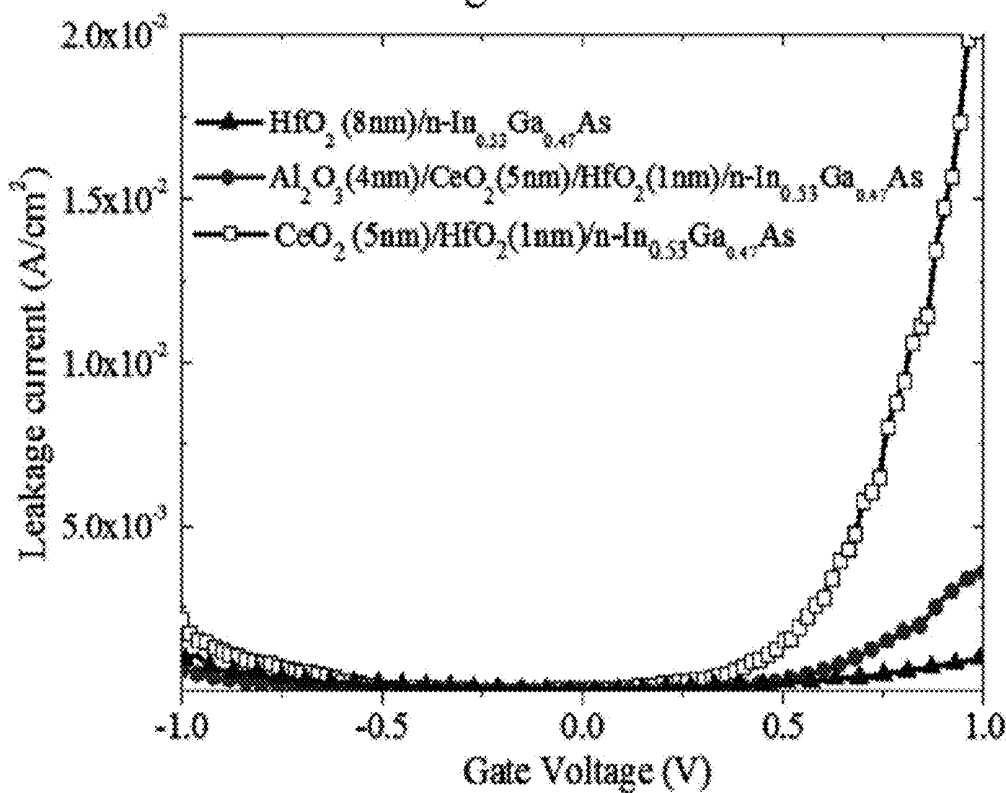


Fig. 6B

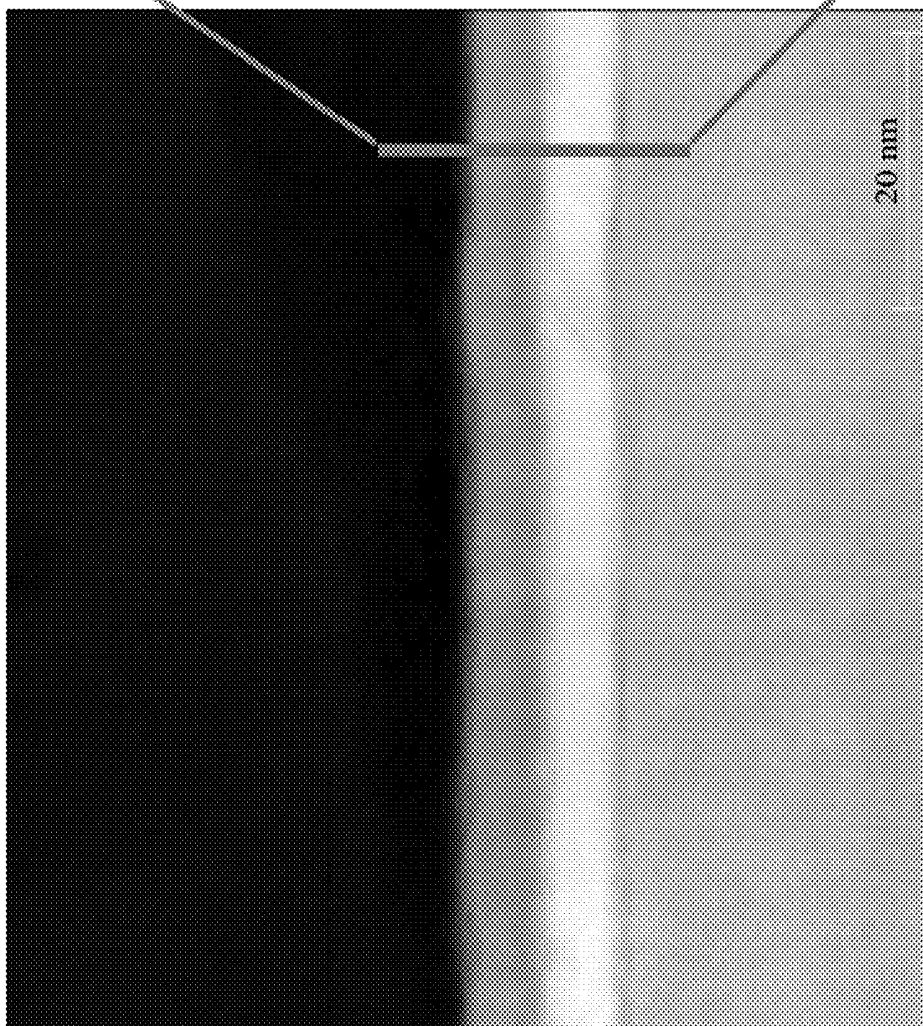
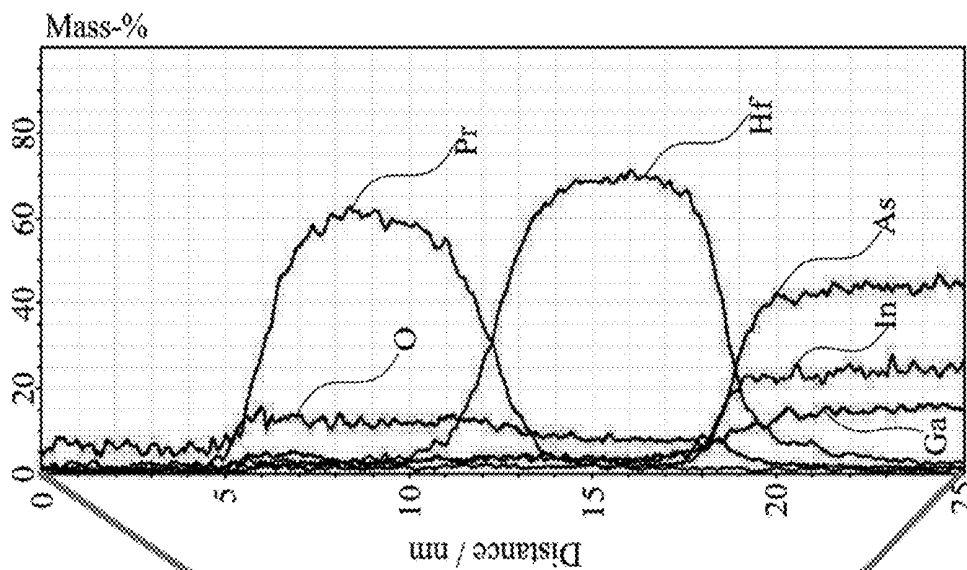


Fig. 7

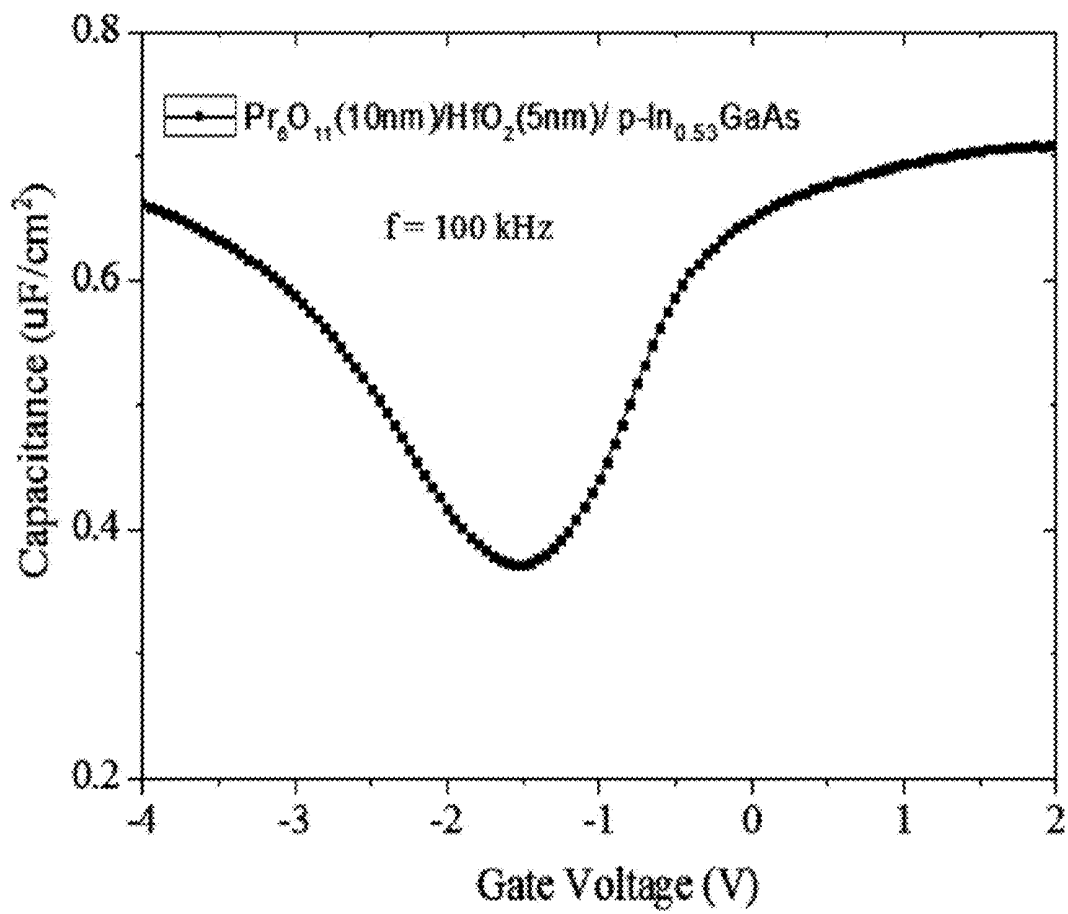


Fig. 8

III-V METAL-OXIDE-SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation-in-part of U.S. application Ser. No. 12/849,025, filed Aug. 3, 2010, currently pending, which is herein incorporated by reference.

BACKGROUND

[0002] 1. Technical Field

[0003] The disclosure relates to a structure of metal-oxide-semiconductor. More particularly, the disclosure relates to a structure of III-V metal-oxide-semiconductor.

[0004] 2. Description of Related Art

[0005] III-V metal-oxide-semiconductor field effect transistors (MOSFETs) have been widely investigated in recent years. $\text{In}_x\text{Ga}_{1-x}\text{As}$ material has high electron mobility and the $\text{In}_x\text{Ga}_{1-x}\text{As}$ based devices have lower turn on voltage than conventional Si devices. Therefore, $\text{In}_x\text{Ga}_{1-x}\text{As}$ material is considered as a potential candidate to replace Si as the channel material for next generation low power, high speed complementary metal-oxide-semiconductor (CMOS) device for logic applications.

[0006] High k materials such as Al_2O_3 , Ga_2O_3 , Gd_2O_3 , ZrO_2 and HfO_2 , were investigated as gate oxides for III-V MOS capacitors. The interface properties of high-k dielectric/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS devices were studied using different surface treatments and even with an inserted Ge or Si thin layers. Recently, the $\text{HfO}_2/\text{Al}_2\text{O}_3$ composite oxide structure was also studied (T. Yang, Y. Xuan, D. Zemlyanov, T. Shen, Y. Q. Wu, J. M. Woodall, and P. D. Ye: Appl. Phys. Lett., 91 (2007) 142122). However, to find a suitable oxide layer that has a really high dielectric constant and really low current leakage for III-V semiconductor is still a difficult task.

SUMMARY

[0007] In one aspect, the present invention is directed to a III-V metal-oxide-semiconductor (MOS) device having a high dielectric constant and low current leakage.

[0008] The III-V MOS device sequentially comprises a III-V semiconductor layer, a hafnium oxide layer, a first metal oxide layer with a high dielectric constant (more than 25), and a metal gate on a substrate. The hafnium oxide layer is in direct contact with the III-V semiconductor layer to form an interfacial layer with the III-V semiconductor layer, such that the hafnium oxide layer can suppress the out-diffusion of the III-V semiconductor layer into the first metal oxide layer to take the advantages of the high dielectric constant of first metal oxide layer.

[0009] According to an embodiment, the first metal oxide layer can be a lanthanum oxide layer, a cerium oxide layer, or a praseodymium oxide layer, for example.

[0010] According to another embodiment, the III-V MOS device further comprises a second metal oxide layer with a wide band gap (more than 6 eV) on the first metal oxide layer to decrease current leakage. For example, the first metal oxide layer is cerium oxide layer, and the second metal oxide layer is aluminum oxide layer.

[0011] The foregoing presents a simplified summary of the disclosure in order to provide a basic understanding to the reader. This summary is not an extensive overview of the disclosure and it does not identify key/critical elements of the

present invention or delineate the scope of the present invention. Its sole purpose is to present some concepts disclosed herein in a simplified form as a prelude to the more detailed description that is presented later. Many of the attendant features will be more readily appreciated as the same becomes better understood by reference to the following detailed description considered in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a cross-sectional diagram of a MOS capacitor.

[0013] FIG. 2 is a diagram of C-V curves of 9 nm HfO_2 — InGaAs MOS capacitor under various operation frequencies.

[0014] FIG. 3A is a diagram of C-V curves of 12 nm La_2O_3 — InGaAs MOS capacitor under various operation frequencies.

[0015] FIG. 3B is a diagram of J-V curve of 12 nm La_2O_3 — InGaAs MOS capacitor.

[0016] FIGS. 4A-4C are diagrams of C-V curves of 8 nm $\text{La}_2\text{O}_3/1$ nm HfO_2 — $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, 7 nm $\text{La}_2\text{O}_3/2$ nm HfO_2 — $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and 6 nm $\text{La}_2\text{O}_3/3$ nm HfO_2 — $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors under various operation frequencies, respectively.

[0017] FIGS. 5A-5C are photographs of tunneling electron microscopy (TEM) and the results of energy dispersive X-ray (EDX) spectrum of 9 nm CeO_2 — $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ MOS capacitor, 6 nm $\text{CeO}_2/3$ nm HfO_2 — $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ MOS capacitor, and 4 nm $\text{Al}_2\text{O}_3/5$ nm $\text{CeO}_2/1$ nm HfO_2 — $\text{In}_{0.47}\text{Ga}_{0.47}\text{As}$ MOS capacitor, respectively.

[0018] FIGS. 6A and 6B are diagrams of C-V curves and leakage current curves at 100 kHz of 4 nm $\text{Al}_2\text{O}_3/5$ nm $\text{CeO}_2/1$ nm HfO_2 — $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, 5 nm $\text{CeO}_2/1$ nm HfO_2 — $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and 10 nm HfO_2 — $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors, respectively.

[0019] FIG. 7 is a photographs of tunneling electron microscopy (TEM) and energy dispersive X-ray (EDX) spectra of 5 nm $\text{Pr}_6\text{O}_{11}/5$ nm HfO_2 — InGaAs MOS capacitor.

[0020] FIG. 8 is a diagram of a C-V curve at 100 kHz of 5 nm $\text{Pr}_6\text{O}_{11}/5$ nm HfO_2 — InGaAs MOS capacitor

DETAILED DESCRIPTION

[0021] In the following detailed description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the disclosed embodiments. It will be apparent, however, that one or more embodiments may be practiced without these specific details. In other instances, well-known structures and devices are schematically shown in order to simplify the drawing.

[0022] Generally, a C-V curve of a MOS capacitor can be divided into three regions. When the applied gate voltage is negative, the MOS capacitor is in the inversion region. In the inversion region, if the capacity of the MOS capacitor is higher, more charge carrier will be generated in the MOS FET. When the applied gate voltage is positive, the MOS capacitor is in the accumulation region. In the accumulation region, if the capacity of the MOS capacitor is higher, the oxide layer of the MOS capacitor has a higher dielectric constant. When the applied gate voltage is about zero, the MOS capacitor is in the depletion region.

[0023] Some MOS capacitors were fabricated to measure the C-V curves thereof. FIG. 1 is a cross-sectional diagram of a MOS capacitor. In FIG. 1, III-V semiconductor layer 210, a

metal oxide layer **220**, and a gate **230** are sequentially disposed on a substrate **200**. In addition, a back metal layer **250** can be further disposed below the substrate **200**. The III-V semiconductor layer **210** above can be an InAs layer or an $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer, for example, and can be formed by epitaxial deposition. The metal oxide layer **220** above can be a single layer made from a single metal oxide, or a composite layer made from at least two metal oxides.

Embodiment 1: $\text{La}_2\text{O}_3/\text{HfO}_2$ —InGaAs MOS Capacitor

[0024] In this embodiment, three $\text{La}_2\text{O}_3/\text{HfO}_2$ —InGaAs MOS capacitors were fabricated, and each layer in the structure of the $\text{La}_2\text{O}_3/\text{HfO}_2$ —InGaAs MOS capacitors is listed in Table 1 below. Two comparative examples, i.e. HfO_2 —InGaAs MOS capacitor and La_2O_3 —InGaAs MOS capacitor were also fabricated, and each layer in the comparative MOS capacitors is also listed in Table 1 below. In this embodiment, the post deposition annealing (PDA) is performed at 500° C. in forming gas (3 H₂ and 97% N₂).

TABLE 1

MOS capacitor	Each layer in the MOS capacitors					
	Examples			Comparative Examples		
	1	2	3	1	2	
Gate	Al (50 nm)					
La_2O_3 layer	8 nm	7 nm	6 nm	—	12 nm	
HfO_2 layer	1 nm	2 nm	3 nm	9 nm	—	
III-V Semiconductor layer	n- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (100 nm) Dopant Si: $5 \times 10^{17} \text{ cm}^{-3}$					
Substrate	n ⁺ -InP					
Back metal	Al (50 nm)					
PDA (° C.)	500	500	500	500	500	

[0025] The C-V curves of the comparative examples 1 and 2 under various operation frequencies were respectively shown in FIGS. 2 and 3A. Comparing FIGS. 2 and 3A, the La_2O_3 —InGaAs MOS capacitor has greater capacitance, since lanthanum oxide has greater dielectric constant (30) than hafnium oxide (25). However, for the La_2O_3 —InGaAs MOS capacitor, a larger dispersion in capacitance and lack of strong inversion in the inversion region were observed. Therefore, it showed that the La_2O_3 —InGaAs MOS capacitor was eclectically failed.

[0026] The J-V curve of the La_2O_3 —InGaAs MOS capacitor above is shown in FIG. 3B. In FIG. 3B, a large gate leakage current (more than 1000 A/cm²) in the investigated range of the applied gate voltage was observed. Accordingly, it seems that some interaction was existed between the lanthanum oxide and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. In the photographs of tunneling electron microscopy (TEM) and the results of energy dispersive X-ray (EDX) spectrum, it was found that $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ diffused into the lanthanum oxide layer, and thus the MOS capacitor failed.

[0027] The C-V curves of examples 1-3 under various operation frequencies are respectively shown in FIGS. 4A-4C. FIGS. 4A and 4B do not show the strong inversion in the inversion region. Therefore, it showed that the 1 nm or 2 nm hafnium oxide layer could not successfully stop the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer diffusing into the lanthanum oxide layer. Since a thin film with relatively low resistivity is often formed between a III-V semiconductor layer and an oxide layer, large

frequency dispersion in the C-V curves is usually observed. However, in FIG. 2C, the frequency dispersion of the C-V curves is quite small. It showed that the 3 nm hafnium oxide layer can successfully inhibit the formation of the thin film between the $\text{In}_{0.5}\text{Ga}_{0.47}\text{As}$ layer and the lanthanum oxide layer.

Embodiment 2: $\text{CeO}_2/\text{HfO}_2$ —InGaAs and $\text{Al}_2\text{O}_3/\text{CeO}_2/\text{HfO}_2$ —InGaAs MOS Capacitors

[0028] In this embodiment, two $\text{CeO}_2/\text{HfO}_2$ —InGaAs MOS capacitors and one $\text{Al}_2\text{O}_3/\text{CeO}_2/\text{HfO}_2$ —InGaAs MOS capacitor were fabricated, and each layer in the structures of the $\text{CeO}_2/\text{HfO}_2$ —InGaAs and $\text{Al}_2\text{O}_3/\text{CeO}_2/\text{HfO}_2$ —InGaAs MOS capacitors is listed in Table 2 below. Two comparative examples, i.e. HfO_2 —InGaAs MOS capacitor and CeO_2 —InGaAs MOS capacitor were also fabricated, and each layer in the comparative MOS capacitors is also listed in Table 2 below. The post deposition annealing (PDA) of each samples are also listed in Table 2 below.

TABLE 2

MOS capacitor	Each layer in the MOS capacitors				
	Examples			Comparative Examples	
	4	5	6	3	4
Gate	Au/Ni				
Al_2O_3 layer	—	—	4 nm	—	—
CeO_2 layer	6 nm	5 nm	5 nm	—	9 nm
HfO_2 layer	3 nm	1 nm	1 nm	10 nm	—
III-V Semiconductor layer	n- $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$	n- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (100 nm)		n- $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$	
Substrate	Dopant Si: $5 \times 10^{17} \text{ cm}^{-3}$				
Back metal	n ⁺ -InP				
PDA (° C.)	500	400	400	500	500

[0029] FIGS. 5A-5C are photographs of tunneling electron microscopy (TEM) and energy dispersive X-ray (EDX) spectrum of the comparative example 4 and the examples 4 and 6, respectively. In FIG. 5A (comparative example 4), it can be clearly seen that In, Ga, and As diffused into the cerium oxide layer to form oxides of In, Ga, and As when cerium oxide layer directly contacted the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ layer. This phenomenon led to the MOS capacitor having higher leakage current. In addition, surface pinning, and irregular and uneven interface between CeO_2 layer and $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ layer were also observed.

[0030] However, in FIG. 5B (example 4), it can be observed that the insertion of the 3 nm hafnium oxide layer between the cerium oxide layer and the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ layer could successfully stop the diffusion of In, Ga, and As into the cerium oxide layer. In light of example 4, an interfacial layer can be formed at the interface of a HfO_2 layer and an InGaAs layer to suppress the out-diffusion of In, Ga and As into a CeO_2 layer. In FIG. 5C (example 6), it can be seen that hafnium oxide layer with 1 nm thick was sufficient to suppress the out-diffusion of Ga and As into a CeO_2 layer. Therefore, the leakage current of the MOS capacitors can be decreased, and the operation voltage and capacitance of the MOS capacitors can be increased.

[0031] FIGS. 6A and 6B are diagrams of C-V curves at 100 kHz and leakage current curves of samples 5-6 and comparative sample 3, respectively. Comparing the capacitances of

example 5 (□) and comparative example 3 (▲) in FIG. 6A, it can be observed that the capacitance of the comparative example 3 was enhanced due to the incorporation of high k material of CeO₂ layer in the example 5. However, comparing the leakage current of example 5 (□) and comparative example 3 (▲) in FIG. 6B, the leakage current of comparative example 3 was also increased due to the lower energy band gap of CeO₂ (3.2 eV) incorporated in the example 5.

[0032] Therefore, an aluminum oxide layer with higher band gap value (6.65 eV) was stacked on the cerium oxide layer in example 6 (●). Comparing the capacitances of the examples 5 and 6 in FIG. 6A, it can be observed that the capacitance of the example 6 was still close to the example 5, although the ϵ (dielectric constant of aluminum oxide (8-11.5) is much lower than the dielectric constant of cerium oxide (39). However, comparing the leakage current of the examples 5 and 6 in FIG. 6B, the leakage current had been greatly decreased.

Embodiment 3: Pr₆O₁₁/HfO₂—InGaAs MOS Capacitors

[0033] In this embodiment, a Pr₆O₁₁/HfO₂—InGaAs MOS capacitor was fabricated. Each layer of the Pr₆O₁₁/HfO₂—InGaAs MOS capacitor structure and post deposition annealing (PDA) temperature are listed in Table 3.

TABLE 3

Each layer in the MOS capacitors		
MOS capacitor	Example 7	Comparative Example 5
Gate		Au/Ni
Pr ₆ O ₁₁ layer	5 nm	—
HfO ₂ layer	5 nm	1 nm
III-V Semiconductor layer	n-In _{0.53} Ga _{0.47} As (100 nm) Dopant Si: $5 \times 10^{17} \text{ cm}^{-3}$	
Substrate	n ⁺ -InP	
Back metal		Au/Ge/Ni/Au
PDA (° C.)		500

[0034] FIG. 7 is a photographs of tunneling electron microscopy (TEM) and energy dispersive X-ray (EDX) spectra of example 7. From FIG. 7, it can be known that 5 nm thick hafnium oxide can successfully suppress the out-diffusion of the In, Ga, and As into the praseodymium oxide layer.

[0035] FIG. 8 is a diagram of a C-V curve at 100 kHz of Example 7. From FIG. 8, it can be known that since the 5 nm thick hafnium oxide can suppress the out-diffusion of the In,

Ga, and As into the praseodymium oxide layer, the leakage current of the MOS capacitors can be decreased, and the operation voltage and capacitance of the MOS capacitors can be increased.

[0036] From the embodiments disclosed above, it can be known that an interfacial layer can be formed at the interface of a hafnium oxide layer and an InGaAs layer, and therefore a hafnium oxide with sufficient thickness can successfully suppress the out-diffusion of the In, Ga, and As into the metal oxide layer above the hafnium oxide layer. Accordingly, leakage current of MOS capacitors can be decreased, and operation voltage and capacitance of the MOS capacitors can be increased.

[0037] All the features disclosed in this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, each feature disclosed is one example only of a generic series of equivalent or similar features.

What is claimed is:

1. A III-V metal-oxide-semiconductor (MOS) device, comprising:
 - a III-V semiconductor layer on a substrate;
 - a hafnium oxide layer disposed on the III-V semiconductor layer to directly contact the III-V semiconductor layer;
 - a first metal oxide layer on the hafnium oxide layer, wherein the first metal oxide layer is a lanthanum oxide layer, a cerium oxide layer, or a praseodymium oxide layer; and
 - a metal gate on the metal oxide layer.
2. The III-V MOS device of claim 1 wherein the III-V semiconductor layer is an InAs layer or an InGaAs layer.
3. The III-V MOS device of claim 1, wherein the thickness of the hafnium oxide layer is at least 3 nm when the first metal oxide layer is the lanthanum oxide layer.
4. The III-V MOS device of claim 1, wherein the thickness of the hafnium oxide layer is at least 1 nm when the first metal oxide layer is the cerium oxide layer.
5. The MOS device of claim 1, wherein the thickness of the hafnium oxide layer is at least 5 nm when the first metal oxide layer is the praseodymium oxide layer.
6. The III-V MOS device of claim 1, further comprising a second metal oxide layer located between the first metal oxide layer and the metal gate.
7. The III-V MOS device of claim 6, wherein the first metal oxide layer is cerium oxide layer and the second metal oxide layer is aluminum oxide layer.

* * * * *