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(54) **III-V METAL-OXIDE-SEMICONDUCTOR DEVICE**

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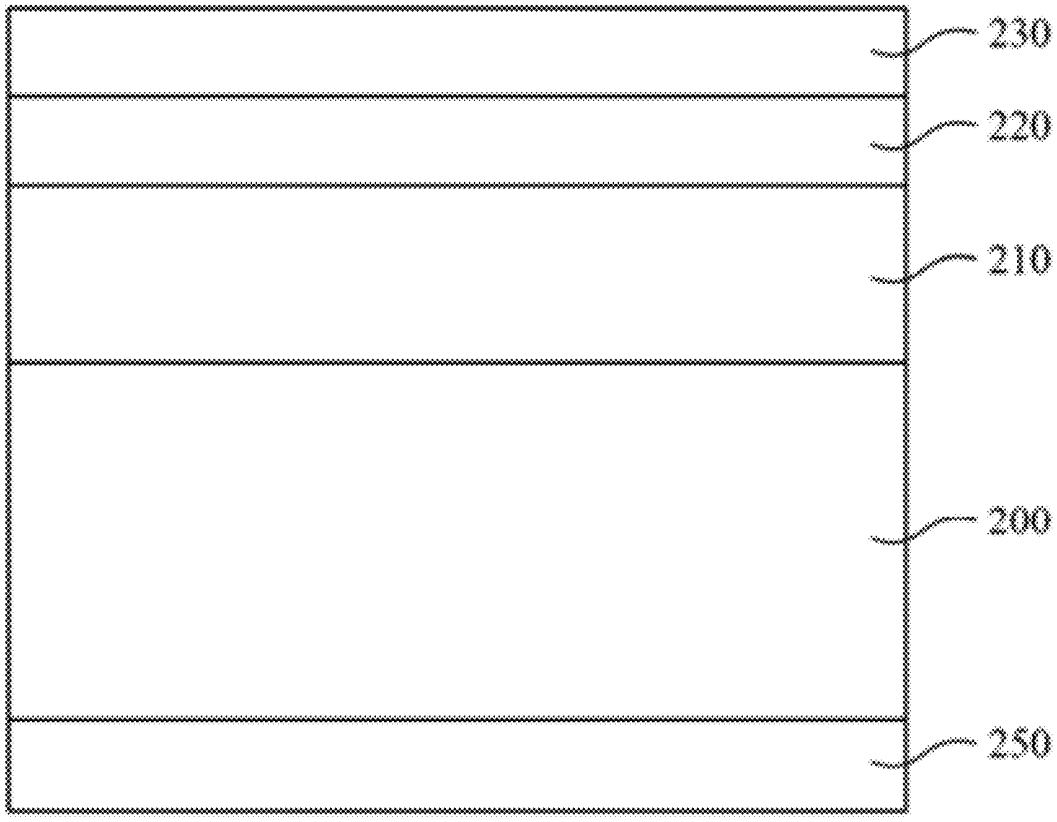
(57) **ABSTRACT**

A barrier layer, hafnium oxide layer, between a III-V semiconductor layer and an lanthanum oxide layer is used to prevent interaction between the III-V semiconductor layer and the lanthanum oxide layer. Meanwhile, the high dielectric constant of the lanthanum oxide can be used to increase the capacitance of the semiconductor device.



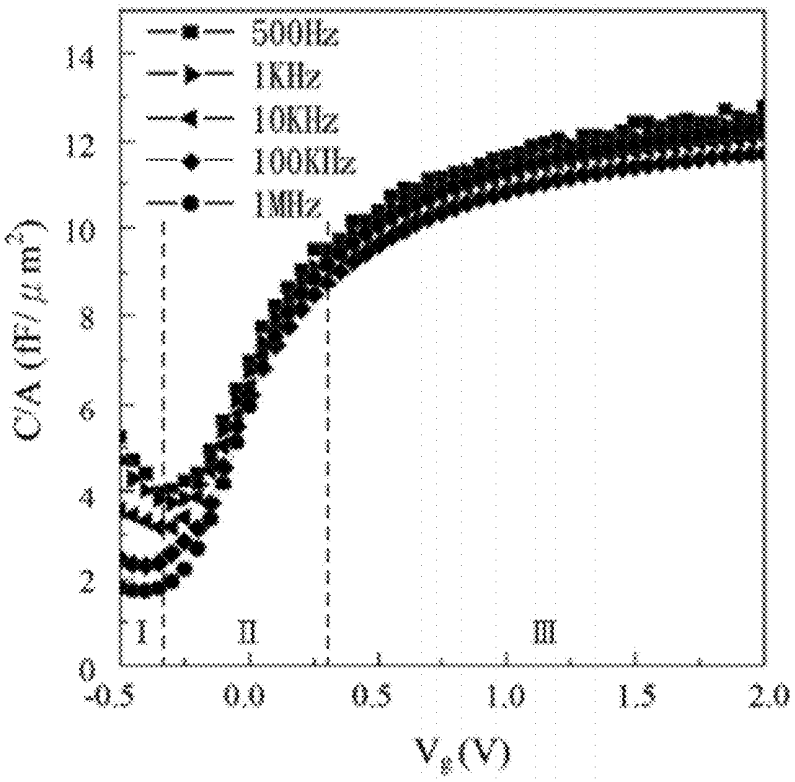
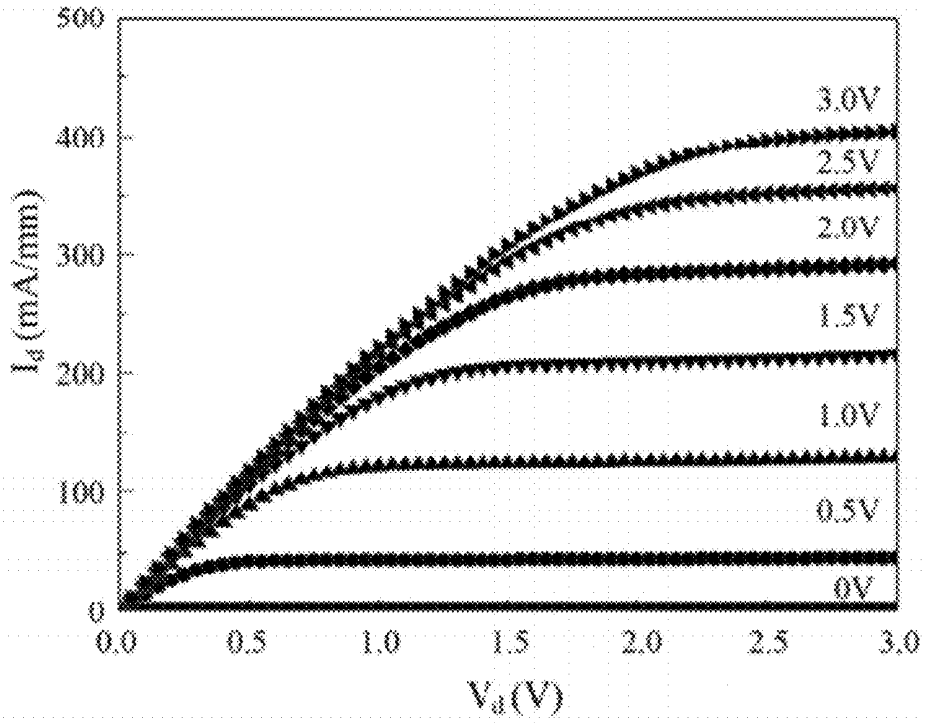

500Hz
1KHz
10KHz
100KHz
1MHz
C/A (fF/μm²)
14
12
10
8
6
4
2
0
I
II
III
-0.5
0.0
0.5
1.0
1.5
2.0
Vg(V)

Fig. 1A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400
300
200
100
0
Id (mA/mm)
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0V
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Vd(V)

Fig. 1B

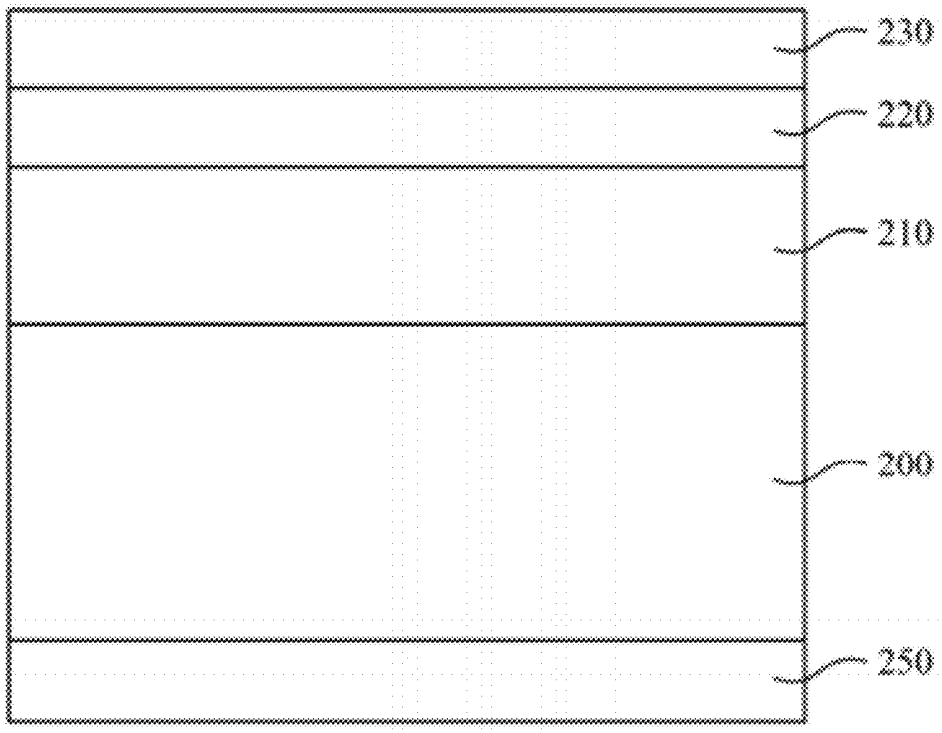


Fig. 2

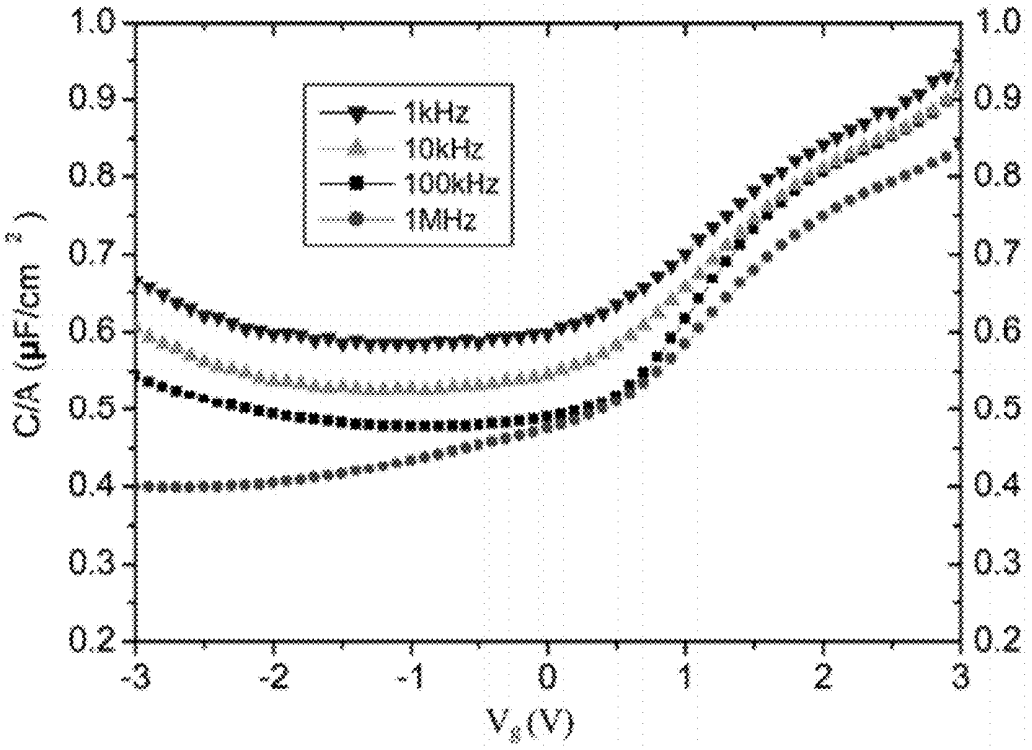


Fig. 3A

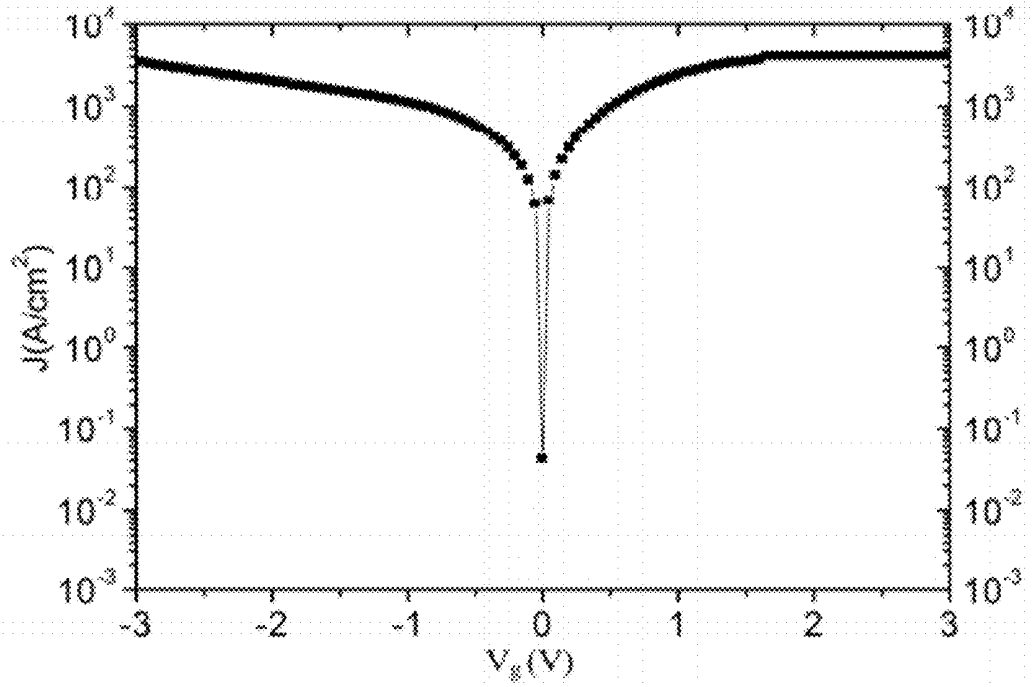
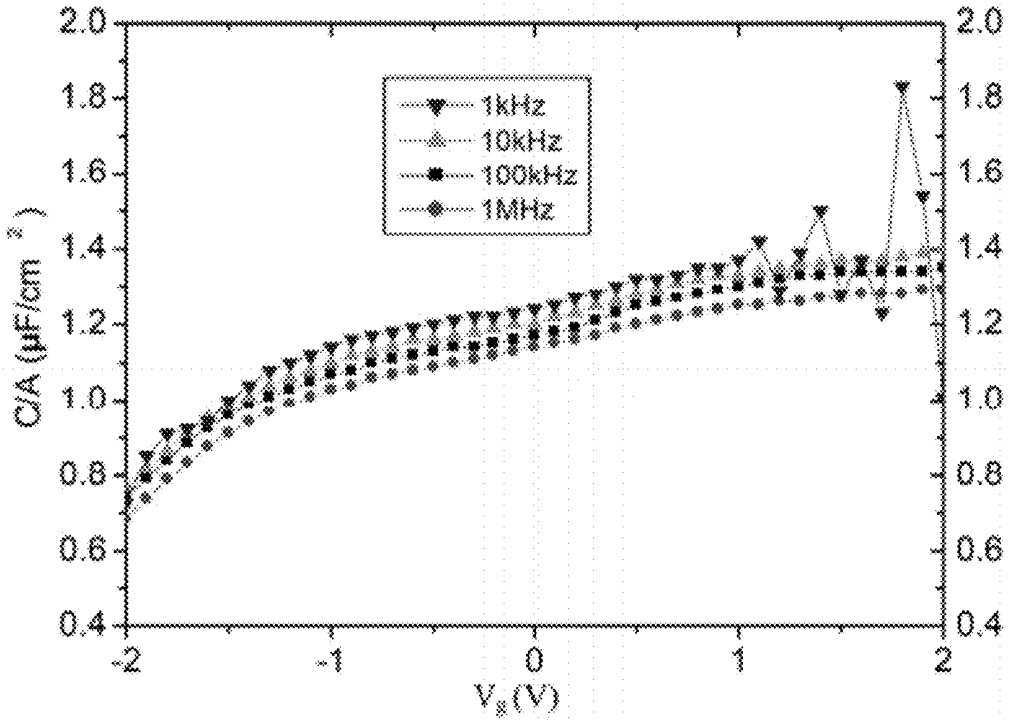


Fig. 3B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10kHz
100kHz
1MHz
C/A (μF/cm²)
V_g(V)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
-2
-1
0
1
2

Fig. 4A

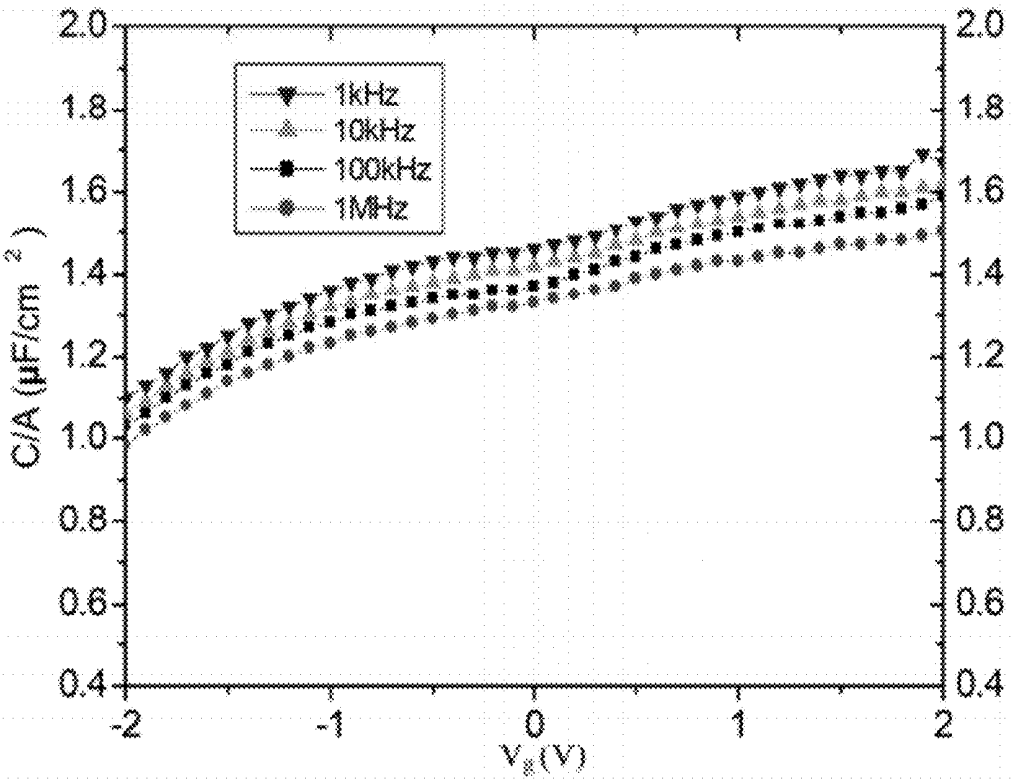
1kHz
10kHz
100kHz
1MHz
C/A (μF/cm²)
V_g(V)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
-2
-1
0
1
2

Fig. 4B

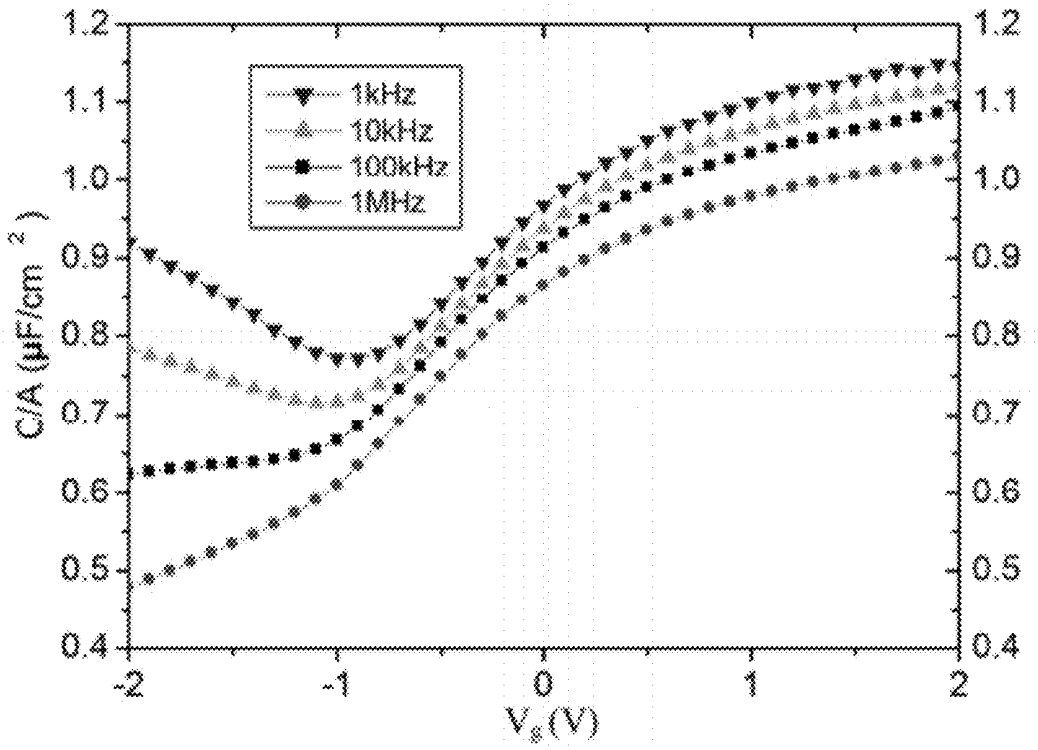
1kHz
10kHz
100kHz
1MHz
C/A (μF/cm²)
V_g (V)
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
-2
-1
0
1
2

Fig. 4C

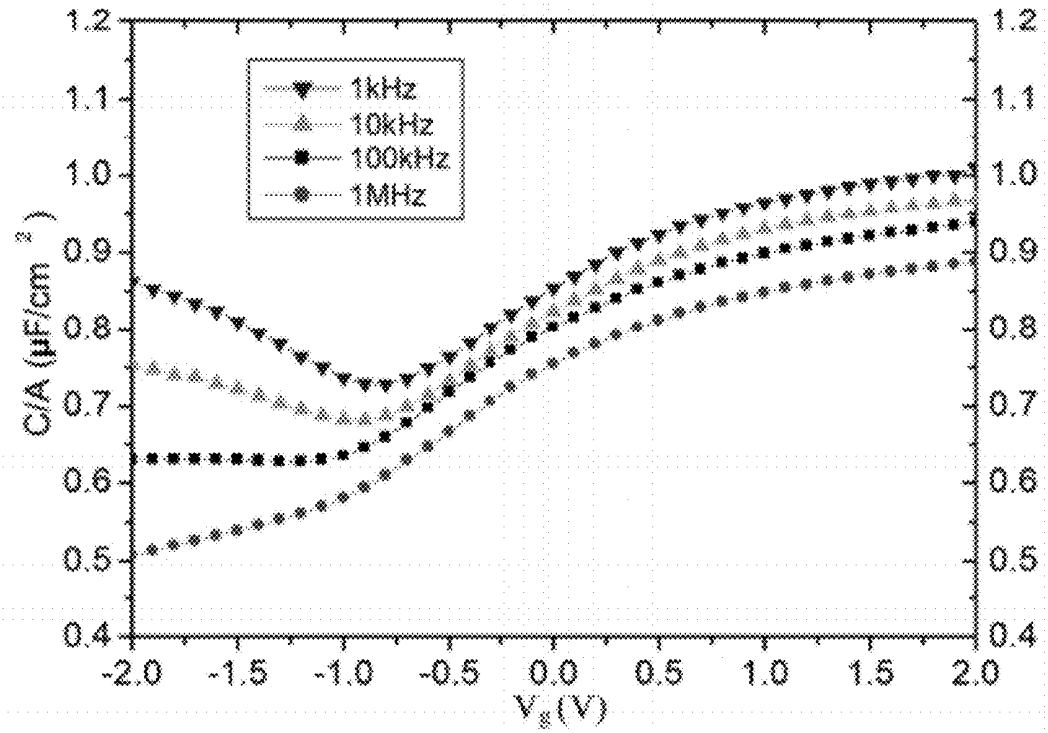
1kHz
10kHz
100kHz
1MHz
C/A (μF/cm²)
V_g (V)
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
-2.0
-1.5
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0

Fig. 5

III-V METAL-OXIDE-SEMICONDUCTOR DEVICE

BACKGROUND

[0001] 1. Technical Field

[0002] The disclosure relates to a structure of metal-oxide-semiconductor. More particularly, the disclosure relates to a structure of III-V metal-oxide-semiconductor.

[0003] 2. Description of Related Art

[0004] With the continuously decrease of the semiconductor device's size, the unit capacitance of a metal-oxide-semiconductor (MOS) structure needs to be continuously increased. For satisfying the requirement of the high unit capacitance, the dielectric constant of the oxide layer in the MOS structure needs to be high enough to avoid current leakage problem and maintain a sufficient thin thickness. However, to find a suitable oxide layer that has a really high dielectric constant and really low current leakage for III-V semiconductor is a difficult task.

SUMMARY

[0005] Accordingly, an oxide layer that has a high dielectric constant and can be used in the III-V MOS structure is provided.

[0006] According to an embodiment, lanthanum oxide which has a really high dielectric constant of about 30 is used to be the oxide layer in the III-V MOS devices. However, the lanthanum oxide was found that it had some interaction with the III-V semiconductor layer to cause large current leakage. Therefore, a hafnium oxide layer was tried to be disposed between the lanthanum oxide layer and the III-V semiconductor layer. It was found that hafnium oxide layer with a thickness not less than 3 nm can successfully separate the lanthanum oxide layer and the III-V semiconductor layer to take the advantages of the high dielectric constant of lanthanum oxide.

[0007] Accordingly, the oxide layer composed of hafnium oxide layer and lanthanum oxide layer can effectively increase the capacity of the III-V devices and solve the current leakage problem at the same time.

[0008] It is to be understood that both the foregoing general description and the following detailed description are by examples, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1**A is a diagram of C-V curves of hafnium oxide-InGaAs MOS capacitor under various operation frequencies.

[0010] FIG. **1**B is a diagram of I-V curves of hafnium oxide-InGaAs MOS FET applied by various gate voltages.

[0011] FIG. **2** is a cross-sectional diagram of the structure of the MOS capacitor.

[0012] FIG. **3**A is a diagram of C-V curves of 12 nm lanthanum oxide-InGaAs MOS capacitor under various operation frequencies.

[0013] FIG. **3**B is a diagram of J-V curve of 12 nm lanthanum oxide-InGaAs MOS capacitor.

[0014] FIGS. **4**A-**4**C are diagrams of C-V curves of 8 nm lanthanum oxide/1 nm hafnium oxide-$In_{0.53}Ga_{0.47}As$, 7 nm lanthanum oxide/2 nm hafnium oxide-$In_{0.53}Ga_{0.47}As$, and 6 nm lanthanum oxide/3 nm hafnium oxide-$In_{0.53}Ga_{0.47}As$ MOS capacitors under various operation frequencies, respectively.

[0015] FIG. **5** is a diagram of C-V curves of 9 nm hafnium oxide-InGaAs MOS capacitor under various operation frequencies.

DETAILED DESCRIPTION

[0016] In the following detailed description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the disclosed embodiments. It will be apparent, however, that one or more embodiments may be practiced without these specific details. In other instances, well-known structures and devices are schematically shown in order to simplify the drawing.

[0017] Conventionally, aluminum oxide, hafnium oxide, or a combination of aluminum oxide and hafnium oxide is used as the gate oxide layer of InGaAs metal-oxide-semiconductor (MOS) field effect transistor (FET). For testing the properties of the oxide and the semiconductor of a MOS FET, a MOS capacitor is usually formed and tested first.

[0018] Typical C-V curves of the hafnium oxide-InGaAs MOS capacitor under various operation frequencies are shown in FIG. **1**A. In the strong inversion region (region I) of FIG. **1**A, if the capacity of the MOS capacitor is higher, more charge carrier will be generated in the MOS FET. In the accumulation region (region III) of FIG. **1**A, if the capacity of the MOS capacitor is higher, the oxide layer of the MOS capacitor has a higher dielectric constant. The region between the strong inversion region (region I) and the accumulation region (region III) in FIG. **1**A is depletion region (region II).

[0019] Later, the MOS FET is formed, and the typical I-V curves of the hafnium oxide-InGaAs MOS FET applied by various gate voltages are shown in FIG. **1**B.

[0020] According to the embodiments of this invention, a lanthanum oxide-InGaAs MOS capacitor and lanthanum oxide/hafnium oxide-InGaAs MOS capacitors were formed and tested for finding a better oxide material. The structure of the MOS capacitor is shown in FIG. **2**. The MOS capacitor is formed by the following method. A 100 nm n-type $In_{0.53}Ga_{0.47}As$ layer **210** was epitaxially grown on a n-type InP substrate **200**, and the Si dopant density in the $In_{0.53}Ga_{0.47}As$ layer **210** was 5×10^{17} cm^{-3}. The $In_{0.53}Ga_{0.47}As$ layer **210** was then chemically cleaned by acetone, ethanol and dipped in HF solution.

[0021] Next, an oxide layer **220** was formed on the $In_{0.53}Ga_{0.47}As$ layer **210** by molecular beam deposition. The oxide layer **220** was lanthanum oxide, hafnium oxide, or a combination of lanthanum oxide and hafnium oxide. Afterwards, the oxide layer **220** was subjected to post deposition annealing (PDA) conducted in forming gas (H_2: 3%, N_2: 97%) at 600° C.

[0022] Subsequently, a 50 nm aluminum metal layer **230** was formed on oxide layer **220** by sputtering and etching. Finally, a 50 nm aluminum back contact **250** was formed on the back side of the InP substrate **200**. The aluminum metal layer **230** and the aluminum back contact **250** can be formed by sputtering and etching.

[0023] Since the dielectric constant of lanthanum oxide is quite high (about 30), the first embodiment used 12 nm lanthanum oxide layer to be the material of the oxide layer **220** in FIG. **2**. However, in FIG. **3**A, the C-V curves of the 12 nm lanthanum oxide-$In_{0.53}Ga_{0.47}As$ MOS capacitor were quite dispersed and lack of strong inversion region as in FIG. **1**A.

Therefore, it showed that the MOS capacitor was eclectically failed. FIG. **3**B is a diagram of J-V curve of 12 nm lanthanum oxide-InGaAs MOS capacitor. In FIG. **3**B, large gate leakage current (more than 1000 A/cm^2) in the investigated range of the applied gate voltage was observed. Accordingly, it seems that some interaction was existed between the lanthanum oxide and $In_{0.53}Ga_{0.47}As$.

[0024] In the photographs of tunneling electron microscopy (TEM) and the results of Energy Dispersive Spectrum (EDS), it was found that $In_{0.53}Ga_{0.47}As$ diffused into the lanthanum oxide layer, and thus the MOS capacitor failed.

[0025] Next, hafnium oxide was used as a barrier layer between lanthanum oxide and $In_{0.53}Ga_{0.47}As$. Although the dielectric constant of hafnium oxide is smaller (about 25) then the dielectric constant of lanthanum oxide (about 30), but hafnium oxide has a wider band gap (about 5.7 eV) than lanthanum oxide (about 4.3 eV). Therefore, the oxide layer **220** in the MOS capacitor structure in FIG. **2** is a combination of 8 nm lanthanum oxide/1 nm hafnium oxide, 7 nm lanthanum oxide/2 nm hafnium oxide, or 6 nm lanthanum oxide/3 nm hafnium oxide in the following embodiments. The C-V curves of the above MOS capacitors are sequentially shown in FIGS. **4**A-**4**C.

[0026] The C-V curves in FIGS. **4**A and **4**B do not show the strong inversion region. Therefore, it showed that the 1 nm or 2 nm hafnium oxide layer cannot successfully stop the $In_{0.53}Ga_{0.47}As$ substrate diffused into the lanthanum oxide layer. Since a thin film with relatively low resistivity is often formed between III-V semiconductor material and oxide layer, large frequency dispersion in the C-V curves is usually observed. However, in FIG. **4**C, the frequency dispersion of the C-V curves is quite small. It showed that the 3 nm hafnium oxide layer can successfully inhibit the formation of the thin film between III-V semiconductor material and oxide layer.

[0027] Next, 9 nm hafnium oxide layer was used to be the oxide layer **220** of the MOS capacitor in FIG. **2**. The C-V curves were shown in FIG. **5**. Comparing the C-V curves in FIG. **4**C and FIG. **5**, it shows that when the oxide layer is 6 nm lanthanum oxide/3 nm hafnium oxide (FIG. **4**C), the MOS capacitor has a larger capacitance and a smaller frequency dispersion. This means that the dielectric constant of the 6 nm lanthanum oxide/3 nm hafnium oxide is greater than the dielectric constant of the 9 nm hafnium oxide layer. Moreover, the calculated equivalent oxide thicknesses (EOTs) of the 6 nm lanthanum oxide/3 nm hafnium oxide and the 9 nm hafnium oxide is about 3.001 and 3.417, respectively. It showed that the 6 nm lanthanum oxide/3 nm hafnium oxide has a smaller EOT, which is consistent with the above result that the 6 nm lanthanum oxide/3 nm hafnium oxide MOS capacitor has a greater capacity.

[0028] From the result above, the combination of a first oxide layer having a higher dielectric constant and a second oxide layer having a wider band gap can meet the requirements of increasing the capacity of the III-V devices and solving the current leakage problem at the same time.

[0029] The reader's attention is directed to all papers and documents which are filed concurrently with this specification and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

[0030] All the features disclosed in this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

What is claimed is:

1. A III-V metal-oxide-semiconductor (MOS) device, comprising:

a III-V semiconductor layer on a substrate;

a hafnium oxide layer on the III-V semiconductor layer;

a lanthanum oxide layer on the hafnium oxide layer; and

a metal layer on the lanthanum oxide layer.

2. The III-V MOS device of claim **1**, wherein the III-V semiconductor layer is InAs layer.

3. The III-V MOS device of claim **1**, wherein the III-V semiconductor layer is InGaAs layer.

4. The III-V MOS device of claim **3**, wherein the III-V semiconductor layer is $In_{0.53}Ga_{0.47}As$ layer.

5. The III-V MOS device of claim **1**, wherein the thickness of the hafnium oxide layer is not less than 3 nm.

6. The III-V MOS device of claim **1**, further comprising a metal back contact on the backside of the substrate.

7. A III-V metal-oxide-semiconductor (MOS) device, comprising:

a barrier layer between a III-V semiconductor layer and an oxide layer for preventing interaction between the III-V semiconductor layer and the oxide layer.

8. The III-V MOS device of claim **7**, wherein the barrier layer is hafnium oxide layer.

9. The III-V MOS device of claim **8**, wherein the III-V semiconductor layer is InGaAs layer and the oxide layer is lanthanum oxide layer.

10. The III-V MOS device of claim **8**, wherein the III-V semiconductor layer is $In_{0.53}Ga_{0.47}As$ layer and the oxide layer is lanthanum oxide layer.

* * * * *