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(54) **APPARATUS AND METHOD OF PROCESSING CYCLIC CODES**

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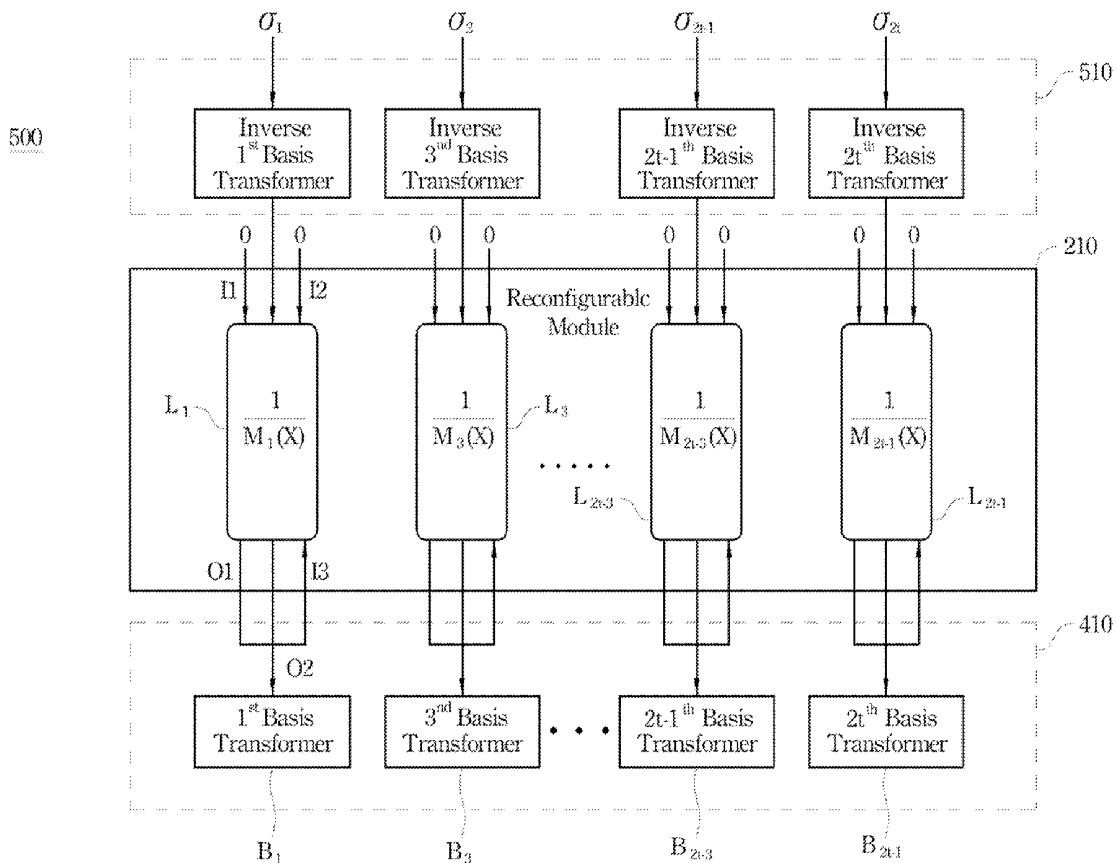
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(57) **ABSTRACT**

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An apparatus and a method of processing cyclic codes are disclosed herein, where the apparatus includes at least one reconfigurable module and an encoder controller. The reconfigurable module includes a plurality of linear feedback shift registers. The encoder controller can control the reconfigurable module to factor a generator polynomial into a factorial polynomial. In the reconfigurable module, the linear feedback shift registers can register a plurality of factors of the factorial polynomial respectively.

(22) Filed: **May 31, 2010**



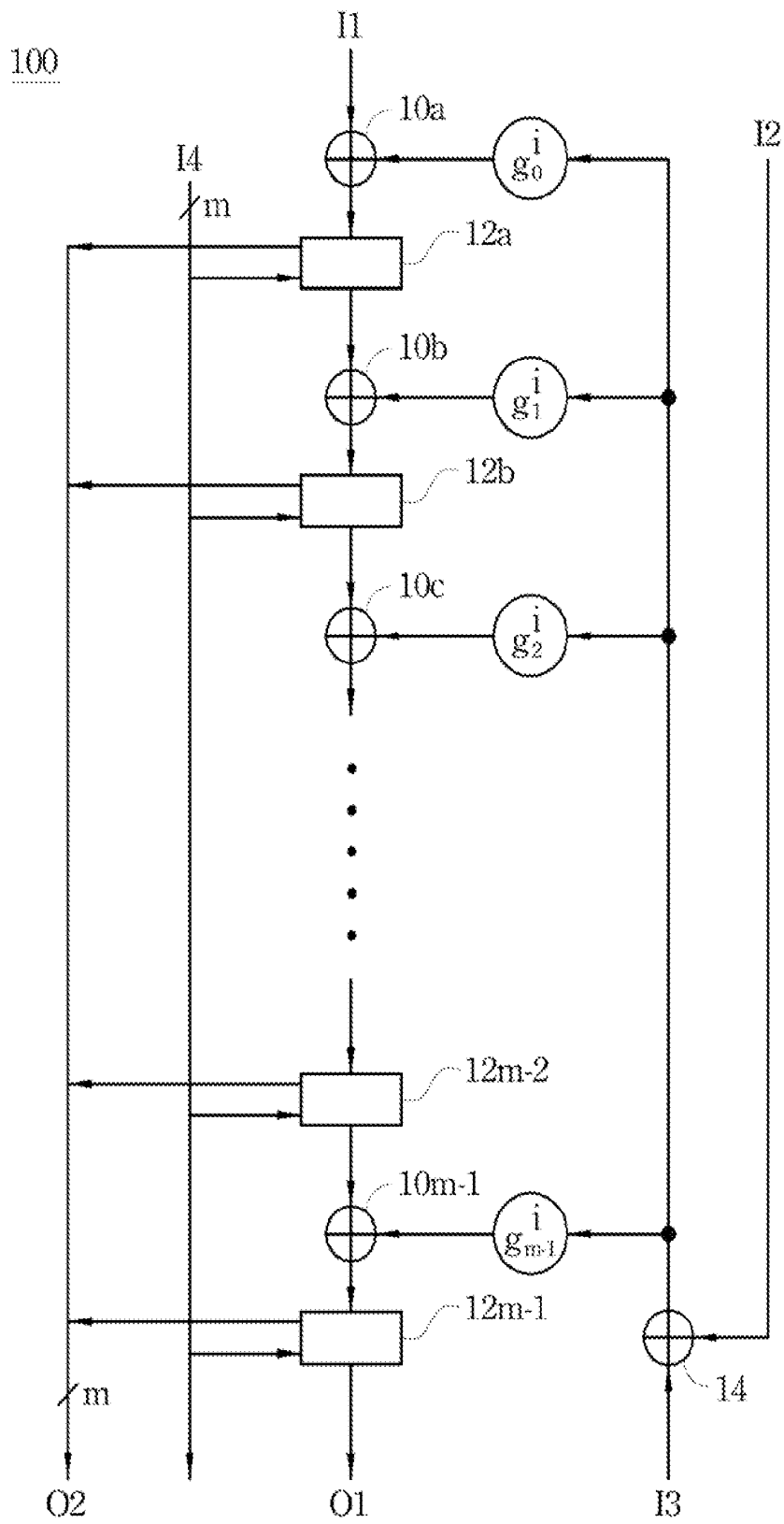


Fig. 1

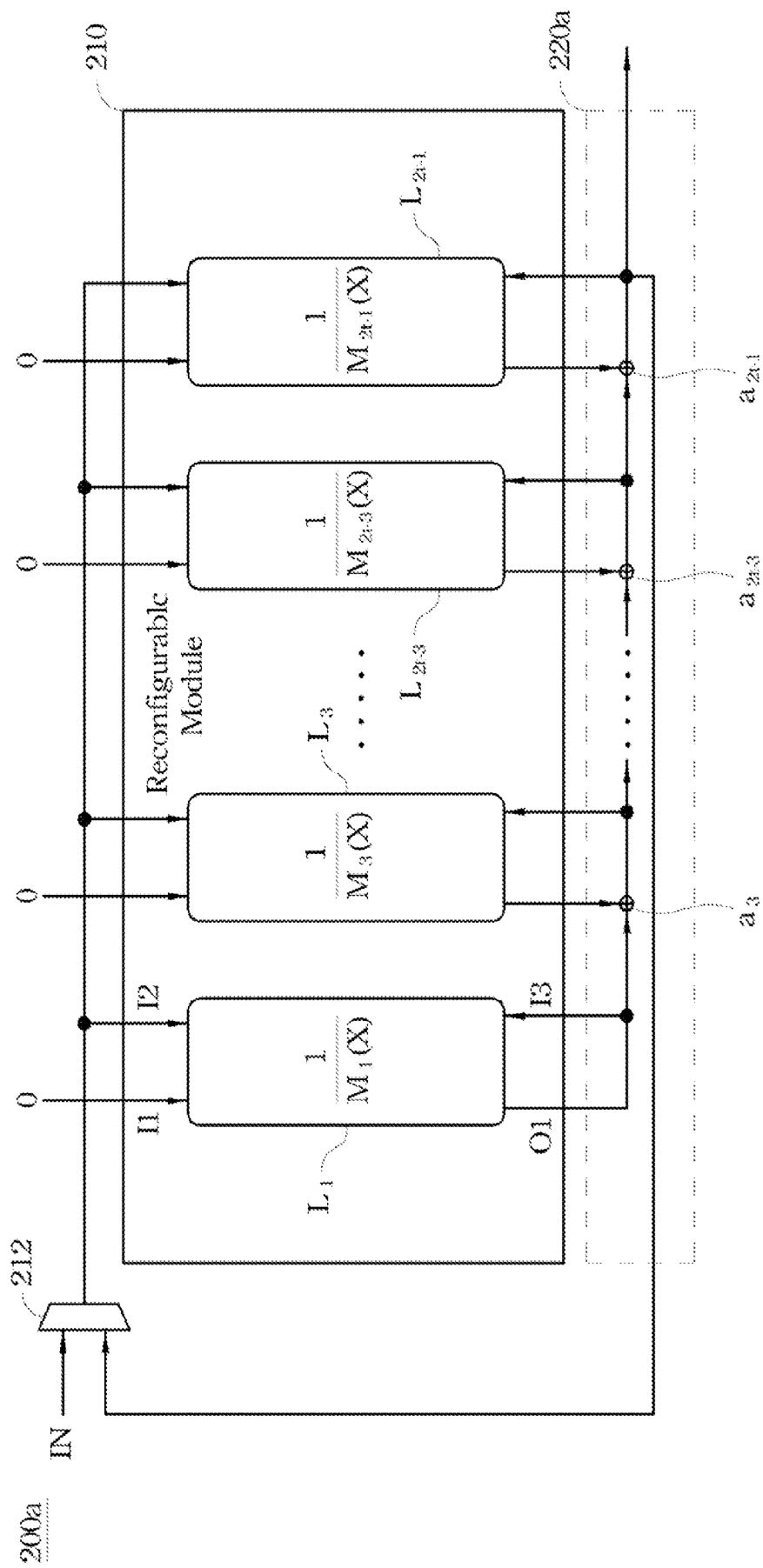


Fig. 2

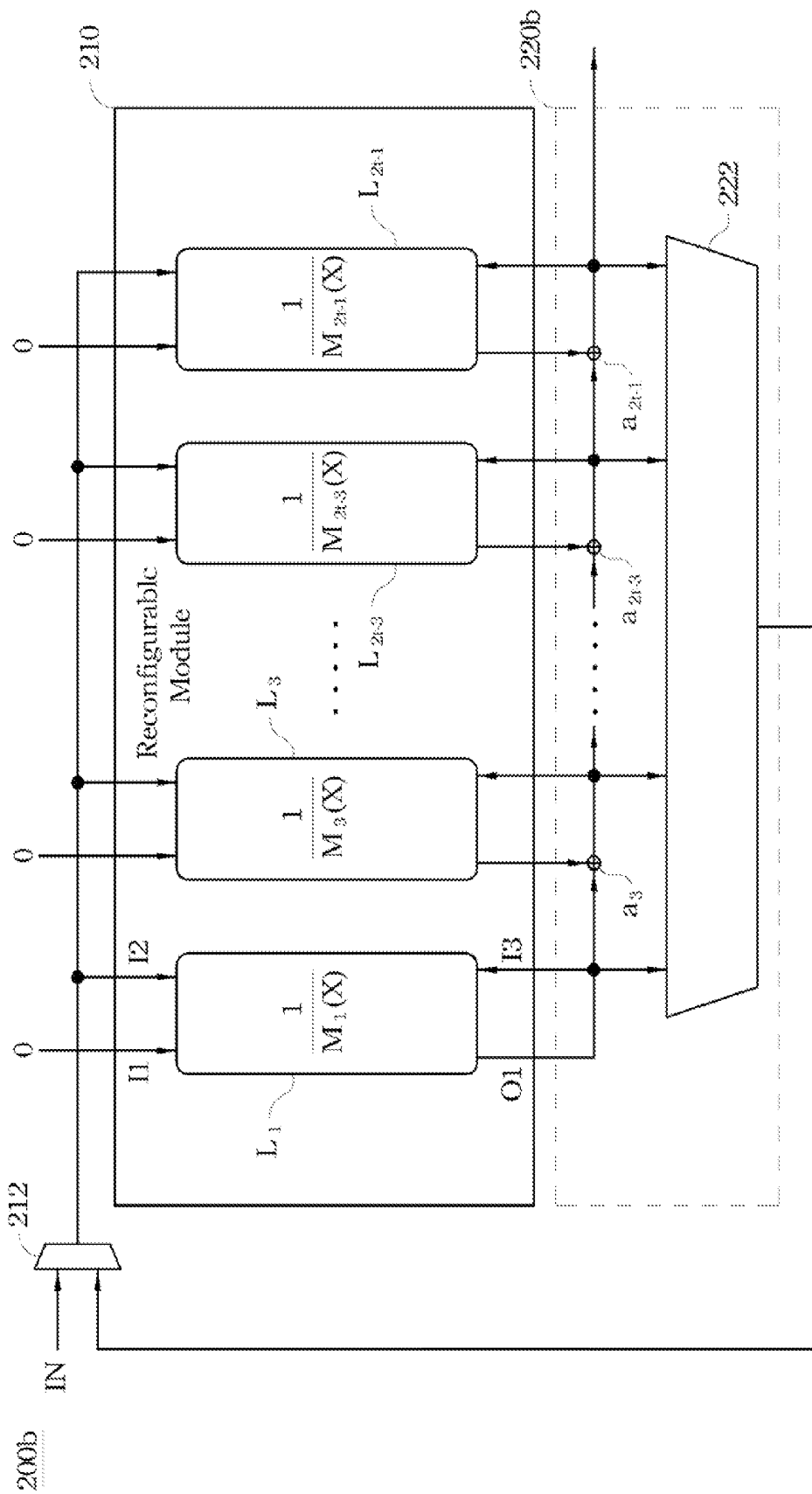


Fig. 3

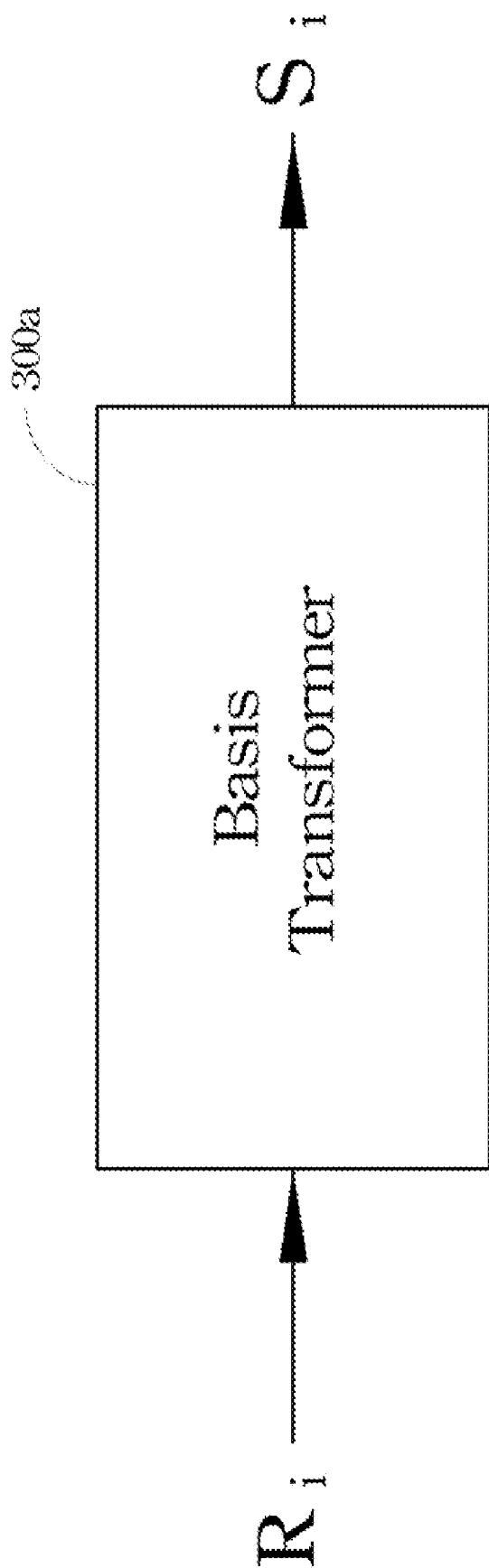


Fig. 4

300a

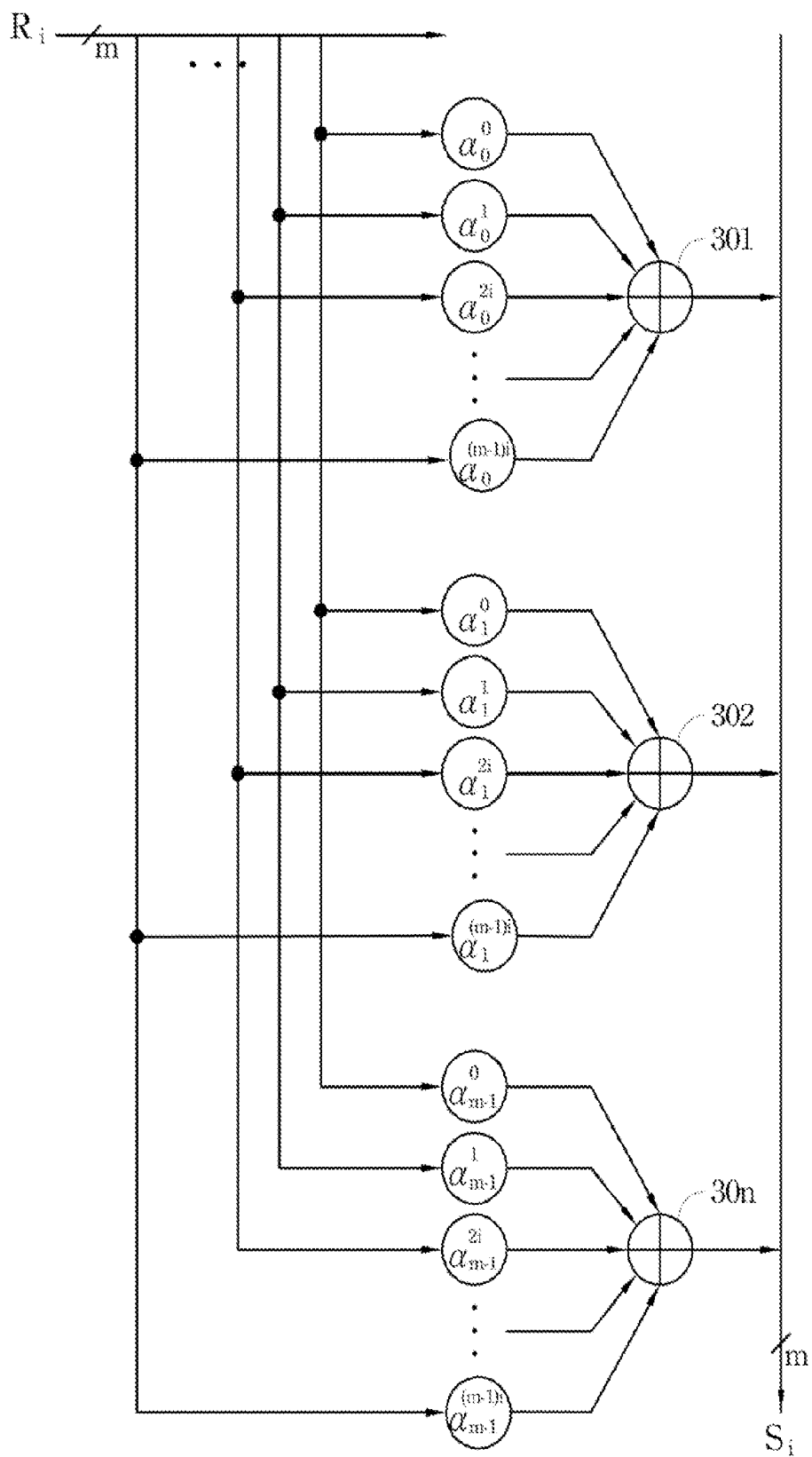


Fig. 5

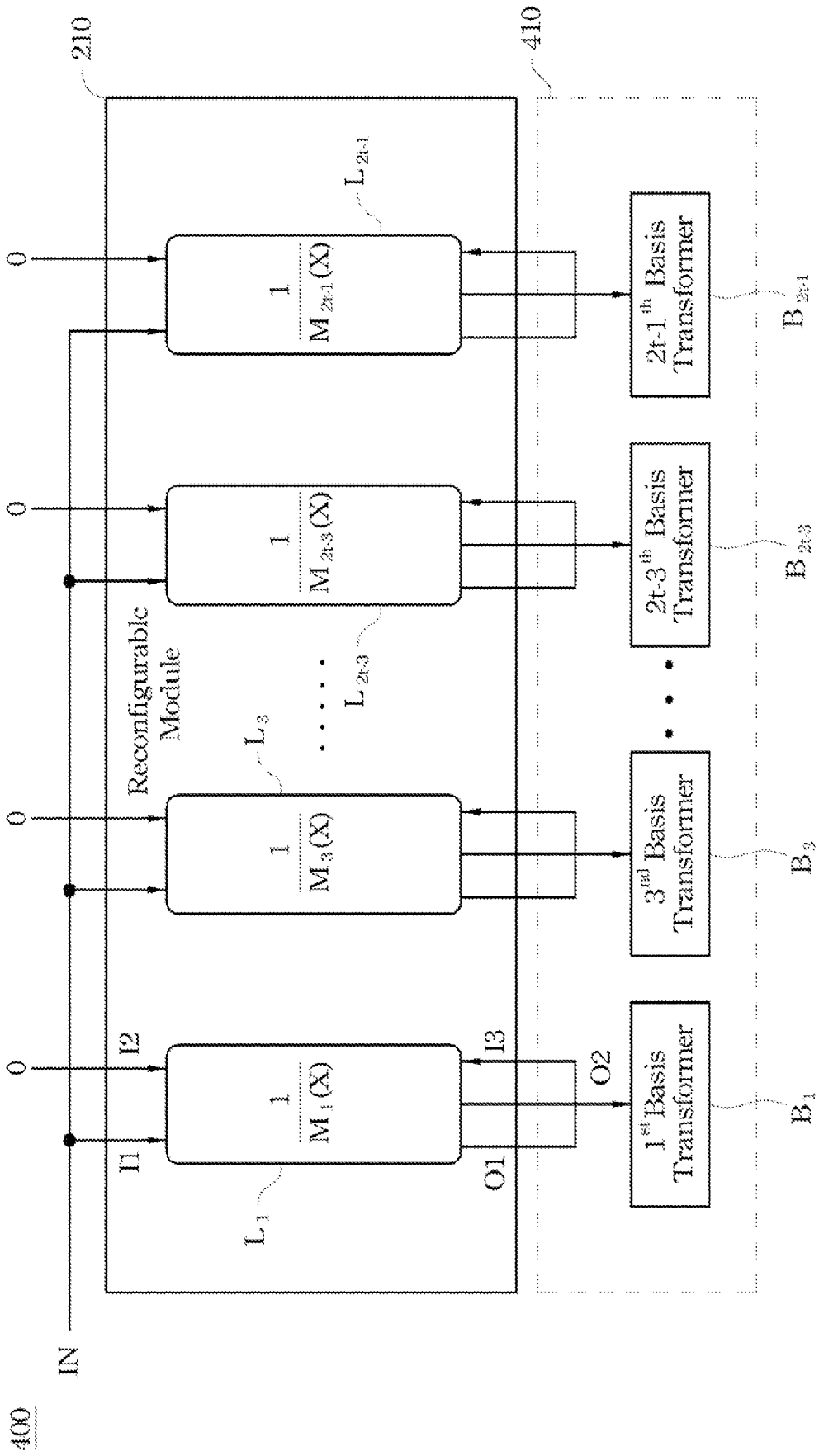


Fig. 6

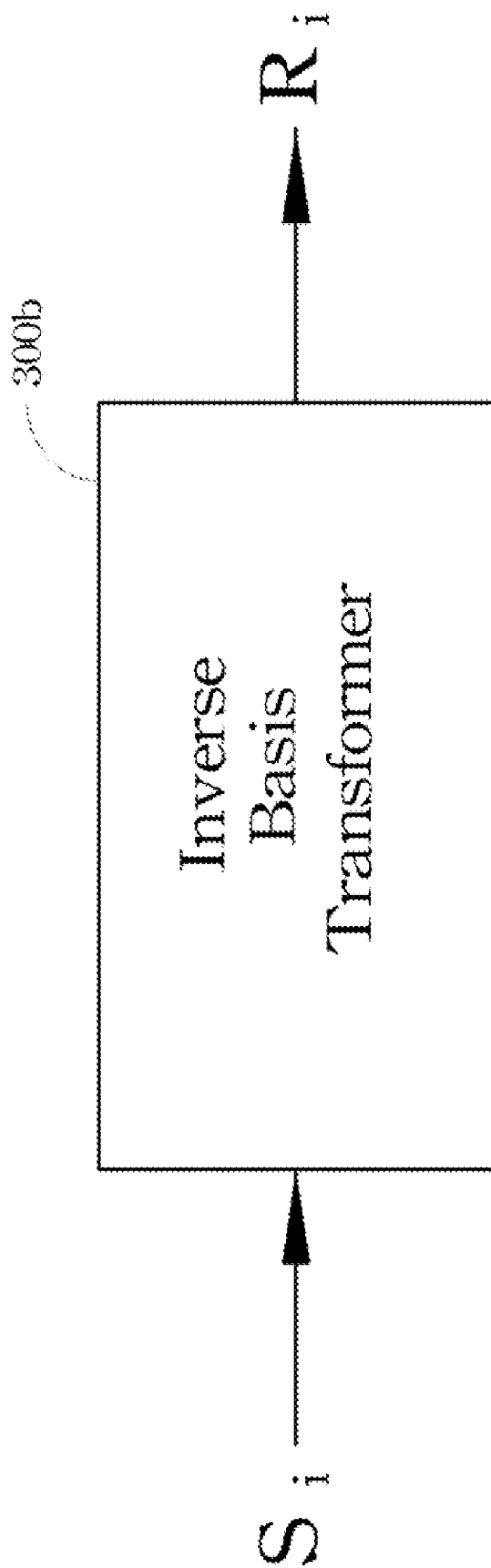


Fig. 7



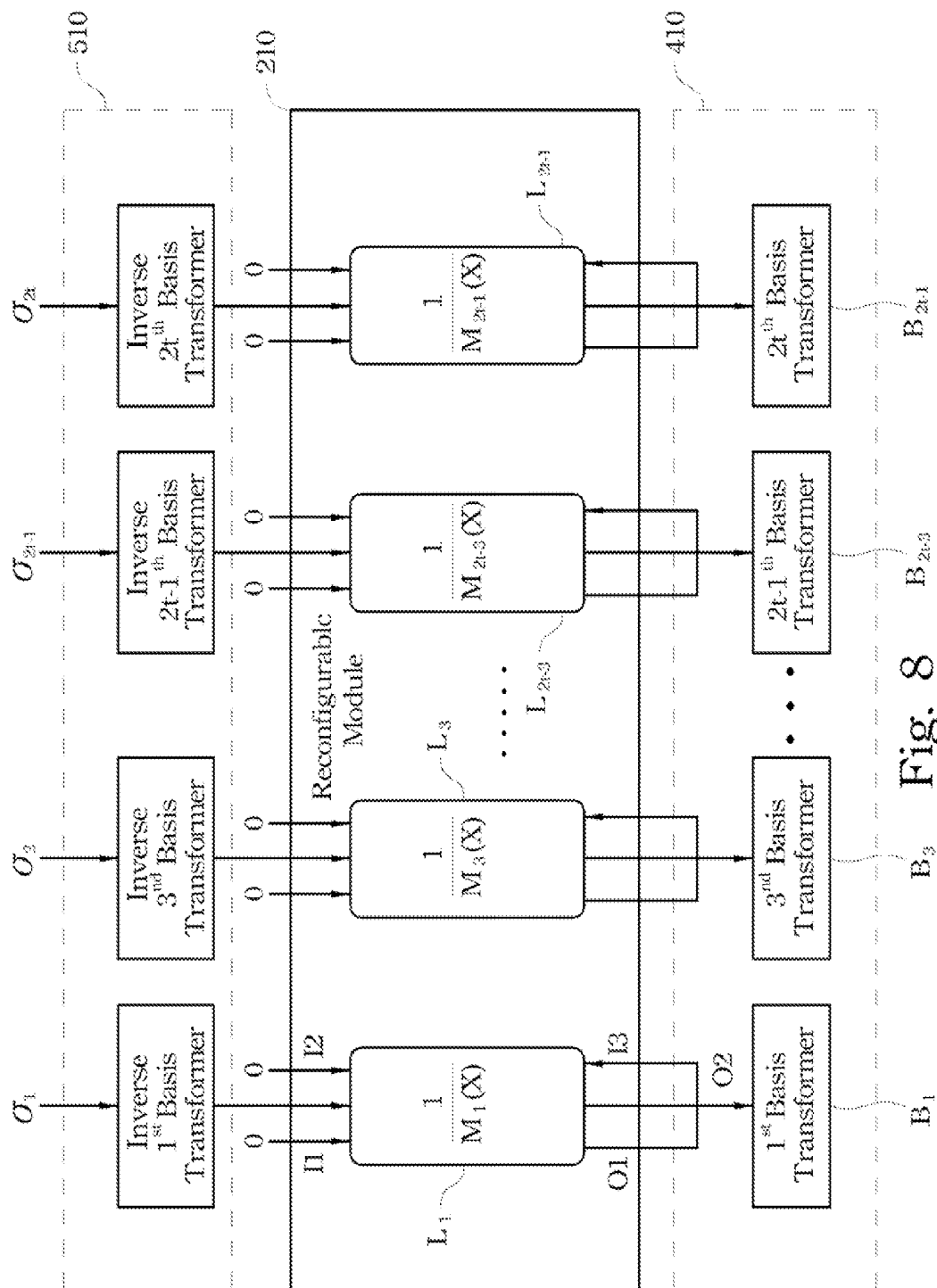


Fig. 8

## APPARATUS AND METHOD OF PROCESSING CYCLIC CODES

### BACKGROUND

**[0001]** 1. Technical Field

**[0002]** The present disclosure relates to electronic technology, and more particularly, an apparatus and method of processing cyclic codes.

**[0003]** 2. Description of Related Art

**[0004]** An error-correcting code (ECC) or forward error correction (FEC) code is a system of adding redundant data, or parity data, to a message, such that it can be recovered by a receiver even when a number of errors (up to the capability of the code being used) were introduced, either during the process of transmission, or on storage. Since the receiver does not have to ask the sender for retransmission of the data, a back-channel is not required in forward error correction, and it is therefore suitable for simplex communication such as broadcasting. Error-correcting codes are frequently used in lower-layer communication, as well as for reliable storage in media such as CDs, DVDs, and dynamic RAM.

**[0005]** Error-correcting codes are usually distinguished between convolutional codes and block codes:

**[0006]** Convolutional codes are processed on a bit-by-bit basis. They are particularly suitable for implementation in hardware, and the Viterbi decoder allows optimal decoding.

**[0007]** Block codes are processed on a block-by-block basis. Early examples of block codes are repetition codes, Hamming codes and multidimensional parity-check codes. They were followed by a number of efficient codes, of which Reed-Solomon codes and BCH codes are the most notable ones due to their widespread use these days. Turbo codes and low-density parity-check codes (LDPC) are relatively new constructions that can provide almost optimal efficiency.

**[0008]** All in all, any error-correcting code can be used for error detection. A code with minimum Hamming distance  $d$  can detect up to  $d-1$  errors in a code word. Using error-correcting codes for error correction can be favorable if strict integrity guarantees are desired, and the capacity of the transmission channel can be modeled.

### SUMMARY

**[0009]** The following presents a simplified summary of the disclosure in order to provide a basic understanding of the reader. This summary is not an extensive overview of the disclosure and it does not identify key/critical elements of the present invention or delineate the scope of the present invention. Its sole purpose is to present some concepts disclosed herein in a simplified form as a prelude to the more detailed description that is presented later.

**[0010]** According to one or more embodiments of the present invention, an apparatus of processing cyclic codes is disclosed, where the cyclic codes may be Reed-Solomon codes, BCH codes or the like. The apparatus includes at least one reconfigurable module and an encoder controller. The reconfigurable module includes a plurality of linear feedback shift registers. The encoder controller can control the reconfigurable module to factor a generator polynomial into a factorial polynomial. In the reconfigurable module, the linear feedback shift registers can register a plurality of factors of the factorial polynomial respectively.

**[0011]** In one embodiment, the encoder controller may essentially consist of a plurality of adders associated with the linear feedback shift registers. The adders and the reconfigurable module constitute a single mode encoder.

**[0012]** In an alternative embodiment, the encoder controller may essentially consist of a plurality of adders and a multiplexer. The adders are associated with the linear feedback shift registers. The multiplexer is configured to select any one of the linear feedback shift registers to control varied modes of an encoding process depending on the desired application. The adders, the multiplexer and the reconfigurable module constitute a multi-mode encoder.

**[0013]** The apparatus may further include a plurality of basis transformers. The basis transformers are electrically coupled with the linear feedback shift registers respectively. In use, the basis transformers can assist the linear feedback shift registers in using the factors of the factorial polynomial to calculate syndromes.

**[0014]** The apparatus may further include a key equation solver. In use, the key equation solver can generate an error location polynomial based on the syndromes.

**[0015]** The apparatus may further include a plurality of inverse basis transformers. The inverse basis transformers are electrically coupled with the linear feedback shift registers respectively. In use, the inverse basis transformers can assist the reconfigurable module and the basis transformers in executing a Chien search for searching all roots of the error location polynomial according to the factors, so as to find an error location.

**[0016]** Moreover, the apparatus may comprise a plurality of foresaid reconfigurable modules in parallelism for supporting varied encoding/decoding speed.

**[0017]** According to one or more embodiments of the present invention, a method of processing cyclic codes in a computer system is disclosed, where the computer system may be a storage element, a communications system or the like. The method includes steps as follows (The steps are not recited in the sequence in which the steps are performed. That is, unless the sequence of the steps is expressly indicated, the sequence of the steps is interchangeable, and all or part of the steps may be simultaneously, partially simultaneously, or sequentially performed). In the encoding process, (a) at least one reconfigurable module is provided, which includes a plurality of linear feedback shift registers; (b) The reconfigurable module is controlled to factor a generator polynomial into a factorial polynomial, so as to register a plurality of factors of the factorial polynomial in the linear feedback shift registers, respectively.

**[0018]** In one embodiment, two or more foresaid reconfigurable modules in parallelism are provided in the step (a) for supporting varied encoding/decoding speed.

**[0019]** In one embodiment, a single mode of the encoding process is performed in the step (b) by means of using the reconfigurable module; in an alternative embodiment, any one of the linear feedback shift registers can be selected in the step (b) to control varied modes of the encoding process depending on the desired application.

**[0020]** The method further includes a decoding process. In the decoding process, (c) syndromes based on the factors of the factorial polynomial are calculated; (d) an error location polynomial based on the syndrome is generated; (e) all roots of the error location polynomial are searched by using the factors, so as to find an error location.

**[0021]** In one embodiment, a plurality of basis transformers, electrically coupled with the linear feedback shift registers respectively, are utilized in the step (c) to for using the factors of the factorial polynomial to calculate syndromes.

**[0022]** In one embodiment, a plurality of inverse basis transformers electrically coupled with the linear feedback shift registers respectively, the reconfigurable module and the basis transformers are utilized in the step (e) to execute a Chien search for searching said all roots of the error location polynomial is according to the factors, so as to find the error location.

**[0023]** Many of the attendant features will be more readily appreciated, as the same becomes better understood by reference to the following detailed description considered in connection with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0024]** The present description will be better understood from the following detailed description read in light of the accompanying drawing, wherein:

**[0025]** FIG. 1 is a schematic diagram illustrating a linear feedback shift register according to one embodiment of the present invention;

**[0026]** FIG. 2 is a schematic diagram illustrating a single mode encoder according to one embodiment of the present invention;

**[0027]** FIG. 3 is a schematic diagram illustrating a multi-mode encoder according to one embodiment of the present invention;

**[0028]** FIG. 4 is a block diagram illustrating a basis transformer according to one embodiment of the present invention;

**[0029]** FIG. 5 depicts the basis transformer of FIG. 4;

**[0030]** FIG. 6 is a schematic diagram illustrating a syndrome calculator according to one embodiment of the present invention;

**[0031]** FIG. 7 is a block diagram illustrating an inverse basis transformer according to one embodiment of the present invention; and

**[0032]** FIG. 8 is a schematic diagram illustrating a Chien search unit according to one embodiment of the present invention.

#### DETAILED DESCRIPTION

**[0033]** In the following detailed description, for purposes of explanation, numerous specific details are set forth in order to attain a thorough understanding of the disclosed embodiments. It will be apparent, however, that one or more embodiments may be practiced without these specific details. In other instances, well-known structures and devices are schematically shown in order to simplify the drawing.

**[0034]** Those having skill in the art will recognize that the state of the art has progressed to the point where there is little distinction left between hardware and software implementations of aspects of systems; the use of hardware or software is generally (but not always, in that in certain contexts the choice between hardware and software can become significant) a design choice representing cost vs. efficiency tradeoffs. Those having skill in the art will appreciate that there are various vehicles by which processes and/or systems and/or other technologies described herein can be effected (e.g., hardware, software, and/or firmware), and that the preferred vehicle will vary with the context in which the pro-

cesses and/or systems and/or other technologies are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a mainly hardware and/or firmware vehicle; alternatively, if flexibility is paramount, the implementer may opt for a mainly software implementation; or, yet again alternatively, the implementer may opt for some combination of hardware, software, and/or firmware. Hence, there are several possible vehicles by which the processes and/or devices and/or other technologies described herein may be effected, none of which is inherently superior to the other in that any vehicle to be utilized is a choice dependent upon the context in which the vehicle, will be deployed and the specific concerns (e.g., speed, flexibility, or predictability) of the implementer, any of which may vary.

**[0035]** As used in the description herein and throughout the claims that follow, the meaning of “a”, “an”, and “the” includes reference to the plural unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the terms “comprise or comprising”, “include or including”, “have or having”, “contain or containing” and the like are to be understood to be open-ended, i.e., to mean including but not limited to. As used in the description herein and throughout the claims that follow, the meaning of “in” includes “in” and “on” unless the context clearly dictates otherwise.

**[0036]** It will be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

**[0037]** Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which example embodiments belong. It will be further understood that terms, such as those defined in commonly used dictionaries, should be, interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

**[0038]** As shown in FIG. 1, the linear feedback shift register **100** comprises a plurality of fixed multipliers  $g_0^i, g_1^i, g_2^i, \dots, g_{m-1}^i$ , latches **12a, 12b, 12c . . . 12m-2, 12m-1**, and adders **10a, 102b, 10c . . . 12m-1** and **14**, where  $g_j^i$  represents the  $j^{\text{th}}$  coefficient of the  $i^{\text{th}}$  minimal polynomial  $M_i(x)$ . For input, the nodes **I1, I2, I3**, each receive 1-bit data, and the node **I4** receives m-bit. For output, the node **O1** outputs 1-bit data, and the node **O2** outputs m-bit data.

**[0039]** As shown in FIG. 2, the single mode encoder **200a** comprises at least one reconfigurable module **210** and an encoder controller **220a**. The reconfigurable module **110** includes a plurality of linear feedback shift registers **L1, L3 . . . L2t-3** and **L2t-1**, where each of these linear feedback shift registers in structure is substantially the same as the above linear feedback shift register **100**.

**[0040]** In the single mode encoder **200a**, data is inputted through the multiplier **212**. The encoder controller **220a** can control the reconfigurable module **210** to factor a generator polynomial into the factorial polynomial  $M_i(x)$ . In the reconfigurable module **210**, the linear feedback shift registers **L1, L3 . . . L2t-3** and **L2t-1** can register a plurality of factors

$$\frac{1}{M_1(x)}, \frac{1}{M_3(x)}, \dots, \frac{1}{M_{2t-3}(x)}, \frac{1}{M_{st-1}(x)}$$

of the factorial polynomial respectively.

**[0041]** For example, The single mode encoder **200a** for encoding BCH codes satisfies the relationship of:  $c(x)=x^{n-k}M(x)+r(x)$ , where  $c(x)$  respects codeword,  $m(x)$  respects transmitted information, and  $r(x)=x^{n-k}M(x) \bmod g(x)$ .  $g(x)$  is a generator polynomial that satisfies the relationship of:  $g(x)=\text{LCM}\{M_1(x), M_3(x), \dots, M_{2t-3}(x), M_{st-1}(x)\}$ , where  $M_i(x)$  is a minimal polynomial and its root is  $\alpha^i$ .

**[0042]** In FIG. 2, the encoder controller **200a** includes a plurality of adders  $a_1 \dots a_{2t-3}, a_{2t-1}$ . These adders are associated with the linear feedback shift registers **L1, L3 . . . L2t-3** and **L2t-1**. In use, the adders and the reconfigurable module **210** perform a single mode of the encoding process.

**[0043]** As shown in FIG. 3, the multi-mode encoder **200b** is essentially the same as the single mode encoder **200a**, expect that an additional multiplexer **222** associated with the linear feedback shift registers **L1, L3 . . . L2t-3** and **L2t-1** is added. The multiplexer **222** can select one of the nodes **13** of the reconfigurable module **210** services as a feedback signal to control varied modes of the encoding process depending on the desired application.

**[0044]** It should be appreciated that single one reconfigurable module **210** illustrated in FIGS. 3-4 is only examples and should not be regarded as limitations of the present invention. In another embodiment, a plurality of said reconfigurable modules are provided in parallelism for supporting varied encoding/decoding speed.

**[0045]** As shown in FIG. 4, the basis transformer **300a** transform input data into output data. In use, the basis transformer **300a** can receive m-bit data  $R_i$  and then can output m-bit data  $S_0$ .

**[0046]** For a more complete understanding of the basis transformer **300a**, please refer to FIG. 5. FIG. 5 depicts the  $i^{\text{th}}$  basis transformer for generating data  $S_i$ , where a  $\alpha_j^i$  represents the  $j^{\text{th}}$  coefficient of  $\alpha^i$ , in which  $\alpha$  is the primitive element of GF ( $2^m$ ). In this basis transformer, a plurality of fixed multipliers  $\alpha_0^0, \alpha_0^1 \dots \alpha_0^{2i}, \alpha_0^{(m-1)1}$  are associated with the adder **301**; a plurality of fixed multipliers  $\alpha_1^0, \alpha_1^1 \dots \alpha_1^{2i}, \alpha_1^{(m-1)1}$  are associated with the adder **302**; a plurality of fixed multipliers  $\alpha_{m-1}^0, \alpha_{m-1}^1 \dots \alpha_{m-1}^{2i}, \alpha_{m-1}^{(m-1)1}$  are associated with the adder **30n**.

**[0047]** As shown in FIG. 6, the syndrome calculator **400** includes a plurality of basis transformers **410** and the foresaid the reconfigurable module **210**, where each of these basis transformers  $B_1, B_3 \dots a_{2t-3}, a_{2t-1}$  is substantially the same as the above basis transformer **300a**. The basis transformers  $B_1, B_3 \dots a_{2t-3}, a_{2t-1}$  are electrically coupled with the linear feedback shift registers **L1, L3 . . . L2t-3** and **L2t-1** respectively for using the factors of the factorial polynomial to calculate syndromes. Moreover, the key equation solver (not shown) can be configured to generate an error location polynomial based on the syndromes.

**[0048]** As shown in FIG. 7, the inverse basis transformer **300b** performs matrix operation to the basis transformer **300a**. In use, the inverse basis transformer **300b** can receive m-bit data  $S_i$  and then can output m-bit data  $R_i$ .

**[0049]** As shown in FIG. 8, the Chien search unit **500** includes a plurality of inverse basis transformers **510**, the reconfigurable module **210** and the basis transformers **410**,

where each of these basis transformers is substantially the same as the above inverse basis transformer **300b**. The inverse basis transformers are electrically coupled with the linear feedback shift registers  $B_1, B_3 \dots a_{2t-3}, a_{2t-1}$ , respectively. In use, the Chien search unit **500** is configured to execute a Chien search for searching all roots of the error location polynomial according to the factors, so as to find an error location.

**[0050]** In view of above, the encoder and the syndrome calculator **400** can share the same reconfigurable module **120**, and furthermore the syndrome calculator **400** and the Chien search unit **500** can share the same reconfigurable module **120** and the same basis transformers **410**. It should be noted that the number of logic gates in the present apparatus for processing cyclic codes is reduced, so as to simplify the complexity of encoding/decoding process. In practice, about 27.5% logic gates are reduced in 0.18 um CMOS process.

**[0051]** In another aspect, the present disclosure is directed to a method of processing cyclic codes. This method may be easily applied to existing computer systems and may be applicable or readily adaptable to various technologies. The more detail of the method is disclosed in the above embodiments and, thus, is not repeated herein.

**[0052]** It will be understood that the above description of embodiments is given by way of example only and that those with ordinary skill in the art may make various modifications. The above specification, examples and data provide a complete description of the structure and use of exemplary embodiments of the invention. Although various embodiments of the invention have been described above with a certain degree of particularity, or with reference to one or more individual embodiments, those with ordinary skill in the art could make numerous alterations to the disclosed embodiments without departing from the spirit or scope of this invention.

**[0053]** Any element in a claim that does not explicitly state "means for" performing a specified function, or "step for" performing a specific function, is not to be interpreted as a "means" or "step" clause as specified in 35 U.S.C. §112, 6th paragraph. In particular, the use of "step of" in the claims herein is not intended to invoke the provisions of 35 U.S.C. §112, 6th paragraph.

What is claimed is:

1. An apparatus of processing cyclic codes, the apparatus comprising:

at least one reconfigurable module including a plurality of linear feedback shift registers; and

an encoder controller for controlling the reconfigurable module to factor a generator polynomial into a factorial polynomial, the linear feedback shift registers for registering a plurality of factors of the factorial polynomial respectively.

2. The apparatus of claim 1, wherein the encoder controller essentially consists of a plurality of adders associated with the linear feedback shift registers, wherein the adders and the reconfigurable module constitute a single mode encoder.

3. The apparatus of claim 1, wherein the encoder controller essentially consists of a plurality of adders associated with the linear feedback shift registers and a multiplexer configured to select one of the linear feedback shift registers to control varied modes of an encoding process, wherein the adders, the multiplexer and the reconfigurable module constitute a multi-mode encoder.

4. The apparatus of claim 1, further comprising:  
 means for assisting the linear feedback shift registers in using the factors of the factorial polynomial to calculate syndromes;  
 a key equation solver for generating an error location polynomial based on the syndromes; and  
 means for assisting the reconfigurable module and the means for assisting the linear feedback shift registers in executing a Chien search for searching all roots of the error location polynomial according to the factors, so as to find an error location.
5. The apparatus of claim 4, wherein the apparatus comprises a plurality of said reconfigurable modules in parallelism for supporting varied encoding/decoding speed.
6. An apparatus of processing cyclic codes, the apparatus comprising:  
 at least one reconfigurable module including a plurality of linear feedback shift registers; and  
 means for controlling the reconfigurable module to factor a generator polynomial into a factorial polynomial, the linear feedback shift registers for registering a plurality of factors of the factorial polynomial respectively.
7. The apparatus of claim 6, wherein the controlling means includes means for using the reconfigurable module to perform a single mode of the encoding process.
8. The apparatus of claim 6, wherein the controlling means includes means for selecting one of the linear feedback shift registers to control varied modes of an encoding process.
9. The apparatus of claim 6, further comprising:  
 means for assisting the linear feedback shift registers in using the factors of the factorial polynomial to calculate syndromes;  
 a key equation solver for generating an error location polynomial based on the syndromes; and  
 means for assisting the reconfigurable module and the means for assisting the linear feedback shift registers in executing a Chien search for searching all roots of the error location polynomial according to the factors, so as to find an error location.
10. The apparatus of claim 9, wherein the apparatus comprises a plurality of said reconfigurable modules in parallelism for supporting varied encoding/decoding speed.
11. A method of processing cyclic codes in a computer system, the method comprising:  
 (a) providing at least one reconfigurable module including a plurality of linear feedback shift registers; and  
 (b) controlling the reconfigurable module to factor a generator polynomial into a factorial polynomial, so as to register a plurality of factors of the factorial polynomial in the linear feedback shift registers, respectively.
12. The method of claim 11, wherein the step (b) comprises:  
 using the reconfigurable module to perform a single mode of the encoding process.
13. The method of claim 11, wherein the step (b) comprises:  
 selecting one of the linear feedback shift registers to control varied modes of an encoding process.
14. The method of claim 11, further comprising:  
 (c) calculating syndromes based on the factors of the factorial polynomial;  
 (d) generating an error location polynomial based on the syndromes; and  
 (e) using the factors to search all roots of the error location polynomial, so as to find an error location.
15. The method of claim 14, wherein the step (c) comprises:  
 utilizing a plurality of basis transformers electrically coupled with the linear feedback shift registers respectively for using the factors of the factorial polynomial to calculate syndromes.
16. The method of claim 15, wherein the step (e) comprises:  
 utilizing a plurality of inverse basis transformers electrically coupled with the linear feedback shift registers respectively, the reconfigurable module and the basis transformers to execute a Chien search for searching said all roots of the error location polynomial according to the factors, so as to find the error location.
17. The method of claim 14, wherein the step (e) comprises:  
 utilizing a plurality of inverse basis transformers electrically coupled with the linear feedback shift registers respectively, the reconfigurable module and the basis transformers to execute a Chien search for searching said all roots of the error location polynomial according to the factors, so as to find the error location.
18. The method of any of claims 11-17, wherein the step (a) comprises:  
 providing a plurality of said reconfigurable modules in parallelism for supporting varied encoding/decoding speed.
19. The method of claim 11 in which the computer system is a storage element or a communications system.

\* \* \* \* \*