Transient-Induced Latchup Dependence on Power-Pin Damping Frequency and Damping Factor in CMOS Integrated Circuits

Sheng-Fu Hsu, *Student Member, IEEE*, and Ming-Dou Ker, *Senior Member, IEEE*

***Abstract*—The bipolar (underdamped sinusoidal) transient noise on power pins of CMOS integrated circuits (ICs) can trigger latchup in CMOS ICs under system-level electrostatic-discharge test. Two dominant parameters of bipolar transient noise—damping frequency and damping factor—strongly depend on system shielding, board-level noise filter, chip-/board-level layout, etc. The transient-induced-latchup (TLU) dependence on power-pin damping frequency and damping factor was characterized by device simulation and verified by experimental measurement. From the simulation results, bipolar-trigger waveforms with damping frequencies of several tens of megahertz can trigger the TLU most easily. However, TLU is less sensitive to the bipolar-trigger waveforms with an excessively large damping factor or an excessively low/high damping frequency. The simulation results have been experimentally verified with the silicon-controlled-rectifier (SCR) test structures that are fabricated in a 0.25-μm CMOS technology.**

***Index Terms*—Bipolar-trigger voltage, latchup, silicon-controlled rectifier (SCR), system-level electrostatic-discharge (ESD) test, transient-induced latchup (TLU).**

NOMENCLATURE

D_{Freq}	Damping frequency of bipolar-trigger voltage on power pins of CMOS ICs.
D_{Factor}	Damping factor of bipolar-trigger voltage on power pins of CMOS ICs.
$+V_{\mathrm{Peak}}$	Transient positive peak voltage of bipolar-trigger voltage on power pins of CMOS ICs.
$+I_{\mathrm{Peak}}$	Transient positive peak current of bipolar-trigger voltage on power pins of CMOS ICs.
$-V_{\mathrm{Peak}}$	Transient negative peak voltage of bipolar-trigger voltage on power pins of CMOS ICs.
$-I_{\mathrm{Peak}}$	Transient negative peak current of bipolar-trigger voltage on power pins of CMOS ICs.
I_{Sb}	Sweep-back current caused by the bipolar-trigger voltage on power pins of CMOS ICs.
D	Distance between well edge and well (substrate) contact in the p-n-p-n latchup path.
S	Distance between anode and cathode in the p-n-p-n latchup path.
W	Distance between the two adjacent well (substrate) contacts in the p-n-p-n latchup path.
$V_{\mathrm{DD}}(t)$	Time-dependent voltage function used in device simulation to simulate the bipolar-trigger voltage on power pins of CMOS ICs $V_{\mathrm{DD}}(t) = V_0 + V_P \cdot \exp\left(-(t-t_d)D_{\mathrm{Factor}}\right) \cdot \sin\left(2\pi D_{\mathrm{Freq}}(t-t_d)\right)$. V_0 is the initial voltage, t_d is the time delay, V_P is the applied voltage amplitude.
I_{Ds}	Transient displacement current of p-n junction.
$V_{\mathrm{P}+}$	Magnitude of minimum positive V_P to initiate TLU.
$V_{\mathrm{P}-}$	Magnitude of minimum negative V_P to initiate TLU.
t_P	Time period needed for V_{DD} increasing from $-V_{\mathrm{Peak}}$ to the normal circuit operating voltage.
$D_{\mathrm{Freq(min)}}$	Minimum D_{Freq} to initiate TLU.
$D_{\mathrm{Freq(max)}}$	Maximum D_{Freq} to initiate TLU.
V_{Charge}	Applied voltage on charged capacitor (200 pF) in the component-level TLU measurement setup.

I. INTRODUCTION

RECENTLY, transient-induced latchup (TLU) has attracted more attention in the CMOS technology [1]–[7]. The test standard to verify the TLU immunity of CMOS ICs has been also announced [8]. This tendency results from not only the progress of circuitry functionality but also the strict requirements of the system-level electrostatic-discharge (ESD) test [9] for electromagnetic-compatibility (EMC) regulation. During the system-level ESD test, the electrical/electronic products are usually requested to sustain the ESD level of $\pm$8 kV ($\pm$15 kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4." Fig. 1 shows the measurement setup of the system-level ESD test with an indirect contact-discharge test mode [9]. When the ESD gun zaps to

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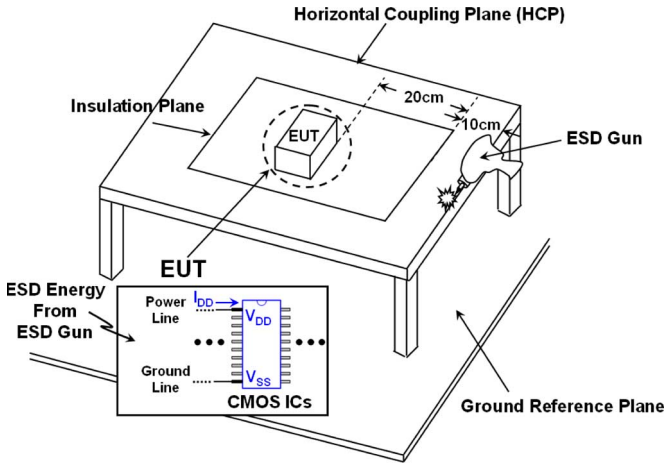


Fig. 1. Measurement setup of the system-level ESD test with an indirect contact-discharge test mode [9]. The ESD-gun zapping on the HCP could cause TLU on all CMOS ICs inside the EUT.

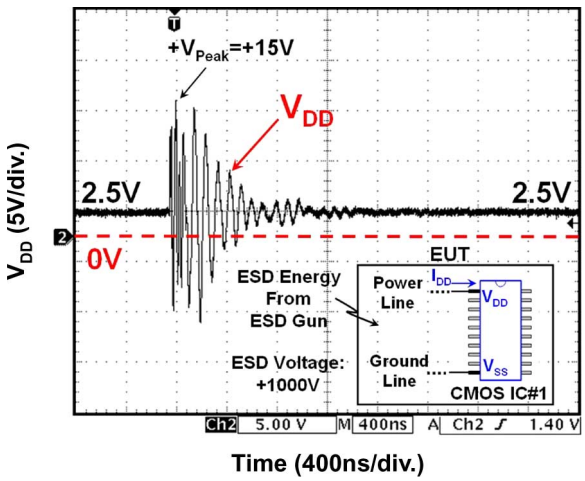


Fig. 2. With an ESD voltage of +1000 V, zapping on the HCP, the measured $V_{\rm DD}$ transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT. $V_{\rm DD}$ waveform is a bipolar voltage due to the disturbance of high ESD-coupled energy.

the horizontal coupling plane (HCP), all CMOS ICs inside the equipment under test (EUT) will be disturbed due to the high ESD-coupled energy, as shown in the inset figure of Fig. 1. With an ESD voltage of +1000 V, zapping on the HCP, the measured $V_{\rm DD}$ transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT is shown in Fig. 2. The $V_{\rm DD}$ power line of CMOS IC#1 no longer maintains its normal dc voltage level of +2.5 V but acts as a bipolar (underdamped sinusoidal) voltage with a $+V_{\rm Peak}$ of +15 V. Such bipolar voltage on power pins of CMOS ICs can easily trigger TLU [10], even though such TLU-sensitive CMOS ICs have already met the quasi-static latchup test standard [11].

The previous work [10] proved that the bipolar-trigger voltage on power pins of CMOS ICs is the major stimulus to initiate TLU under the system-level ESD test. Such bipolar trigger can generate the TLU-triggering current—sweep-back current $(I_{\rm Sb})$. Three dominant parameters to determine $I_{\rm Sb}$ are $D_{\rm Freq}$, $D_{\rm Factor}$, and $+V_{\rm Peak}$ $(-V_{\rm Peak})$ [10]. Thus, it is important to investigate the TLU dependence on $D_{\rm Freq}$, $D_{\rm Factor}$, and $+V_{\rm Peak}$ $(-V_{\rm Peak})$. In real situations, these parameters depend on the charged voltage of the ESD gun, the adopted TLU test mode, and the board-level noise-decoupling filters, etc. Furthermore, the transient noise coupled into chips also strongly depends on the parasitic capacitance, inductance, and resistance of metal traces in the board-/chip-level layout. It is straightforward that a larger voltage amplitude of $+V_{\rm Peak}$ $(-V_{\rm Peak})$ (i.e., larger transient noise) can initiate the TLU more easily. However, so far, it has not been investigated yet how $D_{\rm Freq}$ and $D_{\rm Factor}$ impact the TLU immunity under the system-level ESD test.

In this paper, the TLU dependence on $D_{\rm Freq}$ and $D_{\rm Factor}$ of bipolar-trigger voltage will be investigated in time domain by device simulation. Based on the comprehensive simulation results, the board-level noise filters can be properly developed to efficiently eliminate the ESD-coupled noise for the TLU prevention. The simulation results on TLU have been verified with silicon test chips that are fabricated in a 0.25-μm CMOS process.

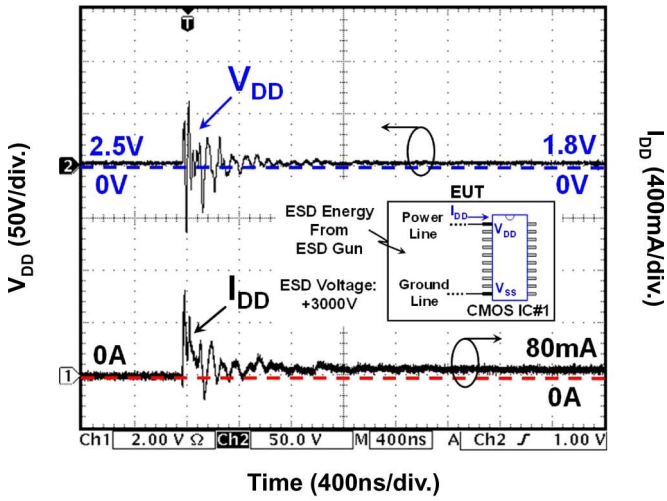
II. Bipolar-Trigger Waveforms Under System-Level ESD Test

During the system-level ESD test, $D_{\rm Freq}$, $D_{\rm Factor}$, and $+V_{\rm Peak}$ $(-V_{\rm Peak})$ depend on many factors. Specifically, the board-level noise-decoupling filter is a dominant factor to determine these parameters. With an ESD voltage of +3000 V, zapping on the HCP, the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms on CMOS IC#1 without and with the noise-decoupling filter are shown in Fig. 3(a) and (b), respectively. Clearly, $D_{\rm Freq}$, $D_{\rm Factor}$, and $+V_{\rm Peak}$ $(-V_{\rm Peak})$ of $V_{\rm DD}$ waveforms are all different in Fig. 3(a) and (b) because of the decoupling capacitance (0.1 μF). As a result, $D_{\rm Freq}$, $D_{\rm Factor}$, and $+V_{\rm Peak}$ $(-V_{\rm Peak})$ can be altered by the noise-decoupling filter, thus strongly dominating the occurrence of TLU under the system-level ESD test.

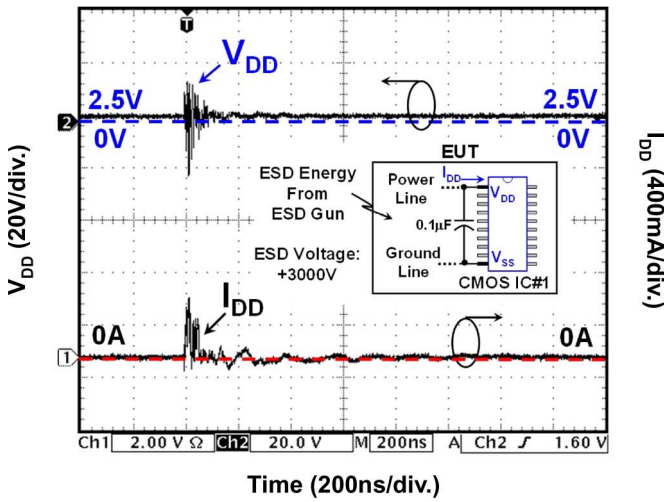
To clarify this issue, the TLU can be initiated with an instantaneously increasing $I_{\rm DD}$ if there is no decoupling capacitance, as shown in Fig. 3(a). After the ESD-induced disturbance on $V_{\rm DD}$, $I_{\rm DD}$ is kept at a high current of 80 mA, while $V_{\rm DD}$ is pulled down to the latchup holding voltage of 1.8 V. However, TLU does not occur if an additional decoupling capacitance of 0.1 μF is added between $V_{\rm DD}$ and $V_{\rm SS}$ of this TLU-sensitive CMOS IC#1, as shown in Fig. 3(b). Thus, $I_{\rm DD}$ does not increase after the ESD-induced disturbance on $V_{\rm DD}$. From the measured TLU transient waveforms in Fig. 3(a) and (b), the occurrence of TLU strongly depends on $D_{\rm Freq}$, $D_{\rm Factor}$, and $+V_{\rm Peak}$ $(-V_{\rm Peak})$ of the bipolar-trigger waveforms on power pins of CMOS ICs. The board-level noise filters dominate these parameters, which have strong impacts on TLU.

III. TLU Simulation

The TLU dependence on both $D_{\rm Freq}$ and $D_{\rm Factor}$ can be investigated by device simulation. Silicon-controlled rectifier (SCR) is used as the test structure for TLU simulation because the occurrence of latchup results from the parasitic SCR in



(a)



(b)

Fig. 3. Measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms, with an ESD voltage of +3000 V zapping on the HCP, on CMOS IC#1 (a) without and (b) with the noise-decoupling filter (decoupling capacitance of 0.1 μF).

CMOS ICs. The SCR structure with specified layout parameters of $D = 6.7$ μm and S = 1.2 μm is used for the TLU simulation in this paper, as shown in Fig. 4. To apply a bipolar trigger on $V_{\rm DD}$ of the defined SCR structure, a specific time-dependent voltage source function in the following is used

$$V_{\rm DD}(t) = V_0 + V_P \cdot \exp\left(-(t - t_d)D_{\rm Factor}\right) \cdot \sin\left(2\pi D_{\rm Freq}(t - t_d)\right). \quad (1)$$

An intended bipolar trigger can be constructed by choosing proper parameters such as initial voltage V_0, time delay t_d, applied voltage amplitude V_P, damping factor $D_{\rm Factor}$, and damping frequency $D_{\rm Freq}$. In this paper, both V_0 and t_d are the fixed values of 2.5 V and 50 ns, respectively. To demonstrate how bipolar trigger initiate TLU, Fig. 5 shows the simulated $V_{\rm DD}$ and $I_{\rm DD}$ transient responses for the bipolar trigger [$V_{\rm DD}(t)$ in (1)] with $D_{\rm Factor}$, $D_{\rm Freq}$, and V_P of 2×10^7 s^{-1}, 20 MHz, and +14.6 V, respectively. During the time period of 50 ns $\leq t \leq$ 75 ns, the N-well/P-substrate junction is reverse biased ($V_{\rm DD} > 0$), and thus, only transient displacement current ($I_{\rm Ds}$) or junction leakage current can be found within the p-n-p-n latchup path. Because such $I_{\rm Ds}$ or junction leakage current is too small to initiate TLU, $I_{\rm DD}$ is negligible within this time period. During the time period of 75 ns $\leq t \leq$ 87.5 ns, the N-well/P-substrate junction is forward biased when $V_{\rm DD}$ drops below 0 V, leading to a large number of minority carriers stored in the N-well/P-substrate region. Afterwards, during the time period of 87.5 ns $\leq t \leq$ 100 ns, when $V_{\rm DD}$ returns from $-V_{\rm Peak}$ to its normal operating voltage of +2.5 V, these stored minority holes (electrons) will be "swept-back" to the P-substrate (N-well) region where they originally come from. As a result, the so-called "sweep-back" current $I_{\rm Sb}$ is formed to initiate TLU, leading $I_{\rm DD}$ to significantly increase.

The corresponding simulated 2-D current flow lines with respect to the various transient timing points are shown in Fig. 6. At timing point C, the N-well/P-substrate junction is forward biased due to a negative $V_{\rm DD}$. Afterwards, during the transition from timing point C to E, the N-well/P-substrate junction returns from the forward-biased state ($V_{\rm DD} < 0$, timing points C and D) to the reverse-biased state ($V_{\rm DD} > 0$, timing point E), while $I_{\rm Sb}$ is formed to initiate TLU. The simulation

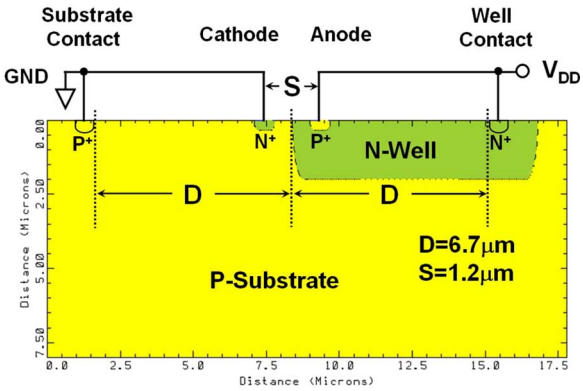


Fig. 4. SCR structure used for the TLU simulation.

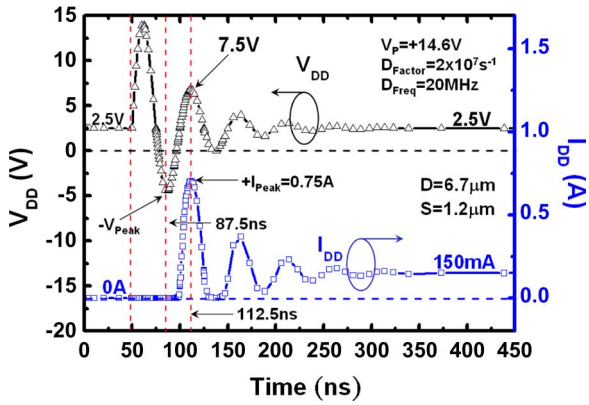


Fig. 5. Simulated $V_{\rm DD}$ and $I_{\rm DD}$ transient responses for the bipolar-trigger voltage ($V_{\rm DD}$) with $D_{\rm Factor}$, $D_{\rm Freq}$, and V_P of 2×10^7 s^{-1}, 20 MHz, and +14.6 V, respectively. The TLU is initiated by $I_{\rm Sb}$ when $V_{\rm DD}$ returns from $-V_{\rm Peak}$ to the normal operating voltage of +2.5 V (87.5 ns $< t <$ 112.5 ns).

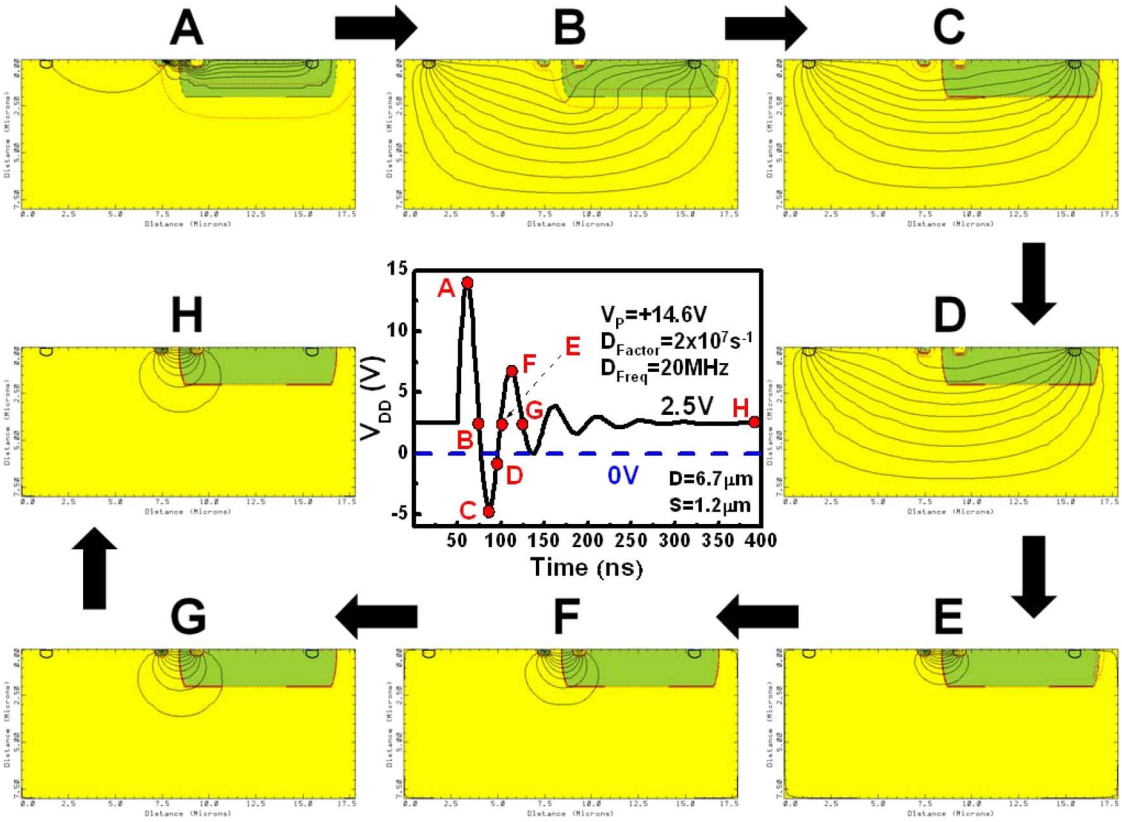


Fig. 6. Corresponding simulated 2-D current flow lines with respect to the various transient timing points. When $V_{\rm DD}$ returns from $-V_{\rm Peak}$ (timing point C) to the normal operating voltage of +2.5 V (timing point E), the TLU can be initiated by $I_{\rm Sb}$ (timing points E–H).

results in Figs. 5 and 6 are consistent with the experimental verifications [10]. Thus, the device simulation proposed in this paper can be used to investigate the TLU dependence on $D_{\rm Freq}$ and $D_{\rm Factor}$.

A. Relations Between $D_{\rm Factor}$ and Minimum Positive (Negative) V_P to Initiate TLU

With a fixed $D_{\rm Freq}$ of 8 MHz, the relations between $D_{\rm Factor}$ and $V_{\rm P+}$ ($V_{\rm P-}$) are shown in Fig. 7(a). $V_{\rm P+}$ ($V_{\rm P-}$) is defined as the magnitude of minimum positive (negative) V_P to initiate TLU. TLU cannot be initiated if the magnitude of the applied positive (negative) V_P is smaller than $V_{\rm P+}$ ($V_{\rm P-}$), because a too small V_P cannot provide a large enough $-V_{\rm Peak}$ (i.e., large enough $I_{\rm Sb}$) to initiate TLU. In addition, because $D_{\rm Factor}$ determines how fast the bipolar-trigger voltage will be attenuated in time domain, so the magnitude of $-V_{\rm Peak}$ strongly depends on $D_{\rm Factor}$. For example, larger $D_{\rm Factor}$ causes larger voltage attenuation within the first cycle of the bipolar-trigger waveforms. Thus, the relations between $D_{\rm Factor}$ and $V_{\rm P+}$ ($V_{\rm P-}$) are very important for the TLU characterization.

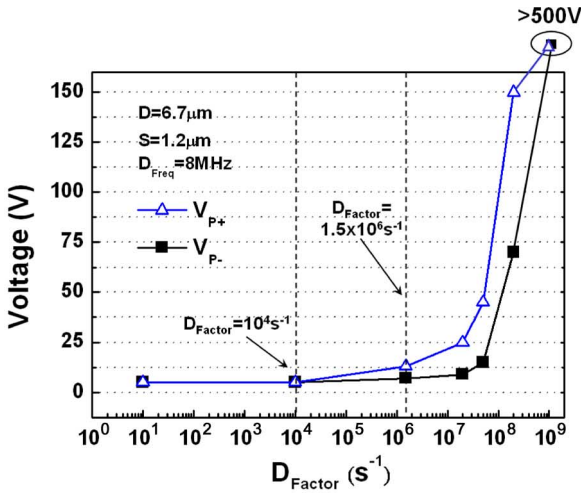
For $D_{\rm Factor} < 10^4$ s^{-1}, both $V_{\rm P+}$ and $V_{\rm P-}$ are independent of $D_{\rm Factor}$ and equal to 6 V. From (1), for the given $D_{\rm Freq}$ of 8 MHz, such small $D_{\rm Factor}$ does not result in an obvious voltage attenuation within the first cycle of bipolar-trigger waveforms (i.e., $-V_{\rm Peak}$ is not obviously attenuated). Thus, for such a small $D_{\rm Factor}$, if a known minimum $-V_{\rm Peak}$ to initiate the TLU is fixed, both $V_{\rm P+}$ and $V_{\rm P-}$ are the same and independent of $D_{\rm Factor}$.

For $D_{\rm Factor} > 10^4$ s^{-1}, both $V_{\rm P+}$ and $V_{\rm P-}$ increase with $D_{\rm Factor}$ because a larger $V_{\rm P+}$ ($V_{\rm P-}$) is necessary for a larger $D_{\rm Factor}$ to provide a known fixed $-V_{\rm Peak}$ (i.e., fixed $I_{\rm Sb}$) which can initiate TLU. Additionally, compared with the negative-going ($V_P < 0$) bipolar voltage, the positive-going ($V_P > 0$) bipolar voltage needs to take an additional half duration for decaying before reaching to $-V_{\rm Peak}$. Thus, $V_{\rm P+}$ that is larger than $V_{\rm P-}$ is necessary to compensate this additional voltage attenuation within the half duration.

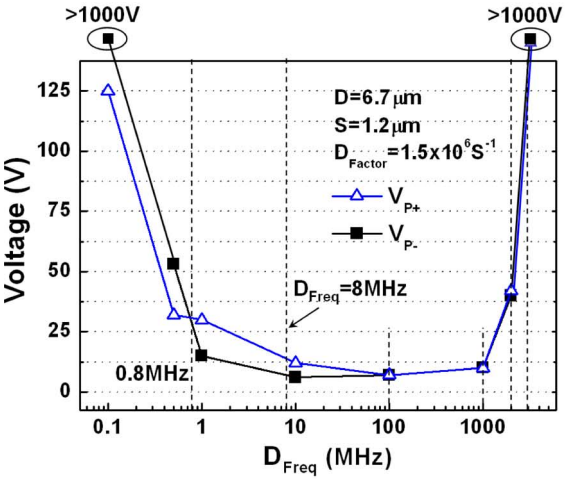
B. Relations Between $D_{\rm Freq}$ and Minimum Positive (Negative) V_P to Initiate TLU

With a fixed $D_{\rm Factor}$ of 1.5×10^6 s^{-1}, the relations between $D_{\rm Freq}$ and $V_{\rm P+}$ ($V_{\rm P-}$) are shown in Fig. 7(b). $D_{\rm Freq}$ is inversely proportional to the duration of bipolar-trigger waveforms. Thus, $D_{\rm Freq}$ determines how fast the bipolar-trigger waveform will be attenuated within its first duration. For example, for a fixed V_P and $D_{\rm Factor}$, higher $D_{\rm Freq}$ (shorter duration) means that the bipolar-trigger voltage takes less time for decaying before reaching to $-V_{\rm Peak}$ (i.e., larger $-V_{\rm Peak}$).

For $D_{\rm Freq} < 0.8$ MHz, $V_{\rm P+}$ is smaller than $V_{\rm P-}$. Such simulation results are different with those in Fig. 7(a) where $V_{\rm P+}$ is larger than $V_{\rm P-}$. For the $V_{\rm P-}$ case, Fig. 8 shows the simulated $V_{\rm DD}$ and $I_{\rm DD}$ transient responses for a bipolar trigger with $D_{\rm Factor}$, $D_{\rm Freq}$, and V_P of 1.5×10^6 s^{-1}, 0.1 MHz, and -200 V, respectively. Clearly, the given $D_{\rm Factor}$ of 1.5×10^6 s^{-1} is too large for such a low-frequency bipolar trigger



(a)



(b)

Fig. 7. Relations between (a) D_{Factor} and $V_{\mathrm{P}+}$ ($V_{\mathrm{P}-}$), and (b) D_{Freq} and $V_{\mathrm{P}+}$ ($V_{\mathrm{P}-}$). $V_{\mathrm{P}+}$ ($V_{\mathrm{P}-}$) is defined as the magnitude of minimum positive (negative) V_P to initiate TLU.

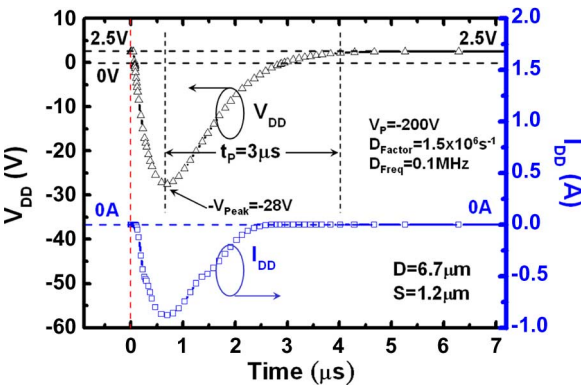


Fig. 8. Simulated V_{DD} and I_{DD} transient responses for the bipolar-trigger voltage with D_{Factor}, D_{Freq}, and V_P of 1.5×10^6 s^{-1}, 0.1 MHz, and -200 V, respectively. The TLU does not occur because t_P is too long (~ 3 μs) to generate a sufficient I_{Sb} [10].

to perform a negative-going bipolar voltage but a negative-going unipolar overdamped voltage instead. TLU does not occur because t_P is too long (~ 3 μs) to generate a sufficient

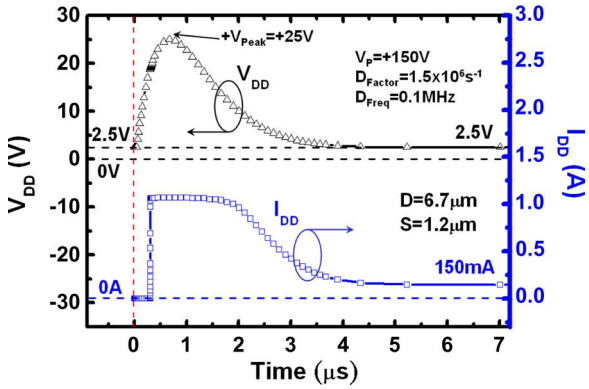


Fig. 9. Simulated V_{DD} and I_{DD} transient responses for bipolar-trigger voltage with the same parameters as those in Fig. 8 but with V_P of $+150$ V. TLU can be initiated by I_{Ds}, while V_{DD} initially increases from the normal operating voltage ($+2.5$ V) to $+V_{\mathrm{Peak}}$.

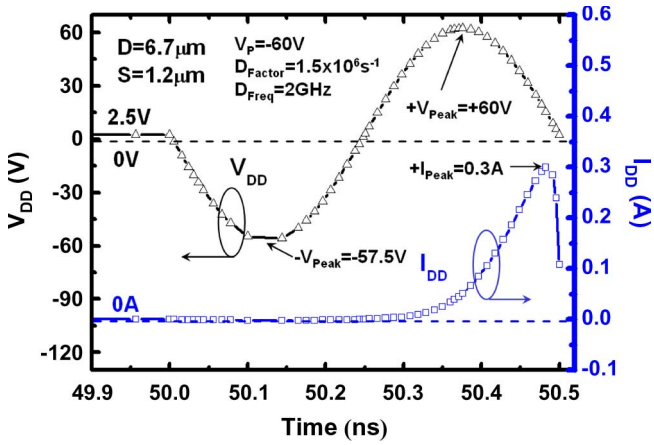


Fig. 10. Simulated V_{DD} and I_{DD} transient responses for the bipolar-trigger voltage with D_{Factor}, D_{Freq}, and V_P of 1.5×10^6 s^{-1}, 2 GHz, and -60 V, respectively. I_{DD} cannot follow the V_{DD} variation in time for such a high-D_{Freq} (> 1 GHz) bipolar trigger, because $+I_{\mathrm{Peak}}$ does not simultaneously appear with $+V_{\mathrm{Peak}}$ but at the end of the first duration ($\sim$50.5 ns).

I_{Sb} [10], even though the magnitude of $-V_{\mathrm{Peak}}$ is as high as 28 V. For the $V_{\mathrm{P}+}$ case, Fig. 9 shows the simulated V_{DD} and I_{DD} transient responses for a bipolar trigger with the same parameters as those in Fig. 8 but with V_P of $+150$ V. Similarly, a positive-going unipolar overdamped voltage is formed due to the given D_{Factor}. However, TLU could be initiated by I_{Ds}, while V_{DD} initially increases from the normal operating voltage ($+2.5$ V) to $+V_{\mathrm{Peak}}$, even though the magnitudes of both V_P and $+V_{\mathrm{Peak}}$ (150 V and 25 V) are smaller than those (200 and 28 V) in Fig. 8. Two different TLU-triggering currents have been mentioned: I_{Ds} [12] and I_{Sb} [10]. It has been clarified that I_{Sb} can initiate TLU more easily than I_{Ds} [13]. From the simulation results in Figs. 8 and 9, however, I_{Ds} (Fig. 9) can initiate TLU more easily than I_{Sb} (Fig. 8) due to a very low D_{Freq}.

For $D_{\mathrm{Freq}} > 1000$ MHz, both $V_{\mathrm{P}+}$ and $V_{\mathrm{P}-}$ significantly increase, as shown in Fig. 7(b). Fig. 10 shows the simulated V_{DD} and I_{DD} transient responses for a bipolar trigger with D_{Factor}, D_{Freq}, and V_P of 1.5×10^6 s^{-1}, 2 GHz, and -60 V, respectively. $+I_{\mathrm{Peak}}$ does not simultaneously appear with

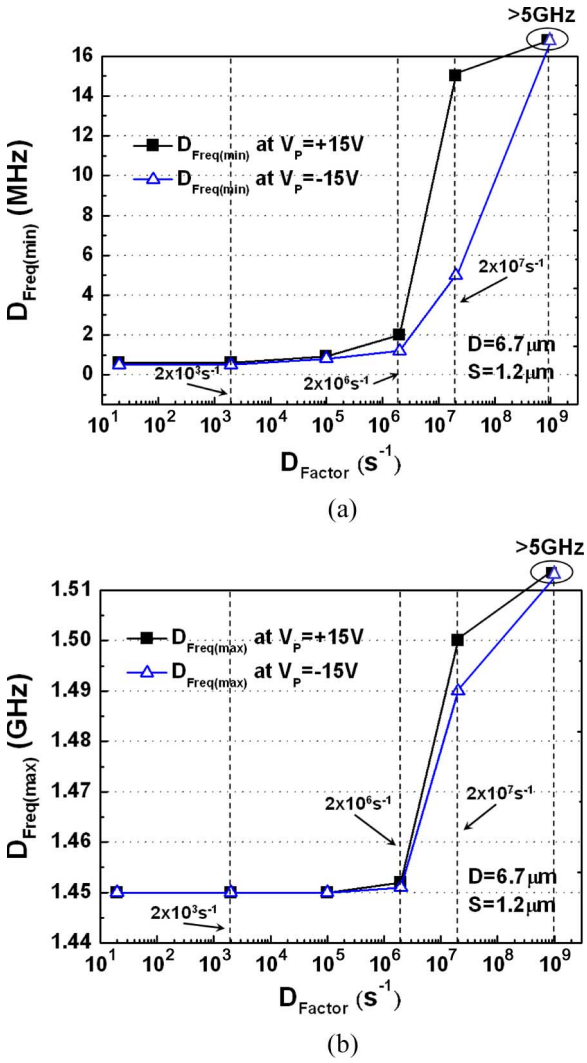


Fig. 11. Relations between (a) D_{Factor} and $D_{\mathrm{Freq(min)}}$, and (b) D_{Factor} and $D_{\mathrm{Freq(max)}}$. $D_{\mathrm{Freq(min)}}$ ($D_{\mathrm{Freq(max)}}$) is defined as the minimum (maximum) D_{Freq} to initiate the TLU under a fixed V_P of +15V or −15V.

$+V_{\mathrm{Peak}}$ but at the end of the first duration (~50.5 ns), because I_{DD} cannot follow the V_{DD} variation in time for such a high-D_{Freq} (> 1 GHz) bipolar trigger. Thus, $+I_{\mathrm{Peak}}$ of 0.3 A is smaller than that (0.75 A) under the low-D_{Freq} (20 MHz) case in Fig. 5, even though $+V_{\mathrm{Peak}}$ of +60 V is much larger than that (+7.5 V) in Fig. 5. If D_{Freq} further increases to above 3 GHz, TLU does not occur (both $V_{\mathrm{P+}}$ and $V_{\mathrm{P-}}$ larger than 1000 V), because the duration of bipolar trigger is not long enough to sustain a positive-feedback latchup event [14].

C. Relations Between D_{Factor} and Minimum (Maximum) D_{Freq} to Initiate TLU

With a fixed V_P of both +15 V and −15 V, the relations between D_{Factor} and $D_{\mathrm{Freq(min)}}$ ($D_{\mathrm{Freq(max)}}$) are shown in Fig. 11(a) and (b). $D_{\mathrm{Freq(min)}}$ ($D_{\mathrm{Freq(max)}}$) is defined as the minimum (maximum) D_{Freq} to initiate TLU under a fixed V_P of +15 V or −15 V. A bipolar trigger with $D_{\mathrm{Freq}} < D_{\mathrm{Freq(min)}}$ ($D_{\mathrm{Freq}} > D_{\mathrm{Freq(max)}}$) cannot trigger TLU due to an insufficient I_{Sb}. For D_{Freq} lower than $D_{\mathrm{Freq(min)}}$, the voltage attenuation on $-V_{\mathrm{Peak}}$ is too large to produce a sufficient I_{Sb} for initiating TLU. For D_{Freq} higher than $D_{\mathrm{Freq(max)}}$, I_{DD} cannot follow the V_{DD} variation in time to generate enough I_{Sb} for initiating TLU.

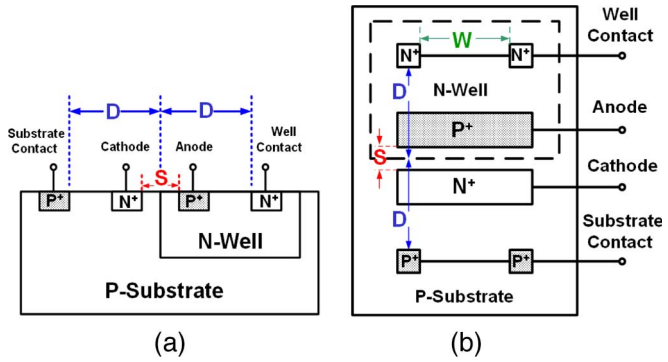


Fig. 12. (a) Device cross-sectional view and (b) layout top view of the SCR structure used for the TLU measurements.

The simulation results are consistent with those shown in Fig. 7(a). For the small-D_{Factor} cases, $D_{\mathrm{Freq(min)}}$ ($D_{\mathrm{Freq(max)}}$) is independent of the D_{Factor} because of the little voltage attenuation within the first cycle of bipolar trigger. For the large-D_{Factor} cases, $D_{\mathrm{Freq(min)}}$ ($D_{\mathrm{Freq(max)}}$) increases with D_{Factor}. In addition, a higher $D_{\mathrm{Freq(min)}}$ or $D_{\mathrm{Freq(max)}}$ is necessary for the positive-going bipolar voltage to initiate TLU, because it takes an additional half duration for decaying before reaching to $-V_{\mathrm{Peak}}$.

From the aforementioned comprehensive simulation results, the bipolar trigger with D_{Freq} of several tens of megahertz can initiate TLU most easily due to the smallest $V_{\mathrm{P+}}$ ($V_{\mathrm{P-}}$) under 10 MHz < D_{Freq} < 100 MHz, as shown in Fig. 7(b). Otherwise, the TLU is less sensitive to the bipolar trigger with an excessively large D_{Factor} [Fig. 7(a)] or an excessively high/low D_{Freq} [Fig. 7(b)].

IV. Experimental Verification

A. TLU Measurement Setup

SCR is used as the test structure for the TLU measurement. The device cross-sectional view and layout top view of the SCR structure are shown in Fig. 12(a) and (b), respectively. The geometrical parameters such as D, S, and W represent the distances between well edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively. All the SCR structures are fabricated in a 0.25-μm salicided CMOS technology.

The component-level TLU measurement setup with a bipolar trigger is used for the experimental verifications of TLU [13], [15], as shown in Fig. 13. An ESD simulator is used to generate the bipolar-trigger source V_{Charge}. A capacitor with a capacitance of 200 pF that is used in the machine model (MM) ESD test is employed as the charged capacitor. The devise under test (DUT) is the SCR test structure shown in Fig. 12. The P^+ anode (N^+ cathode) and the N^+ well contact (P^+ substrate contact) are connected together to V_{DD} (ground).

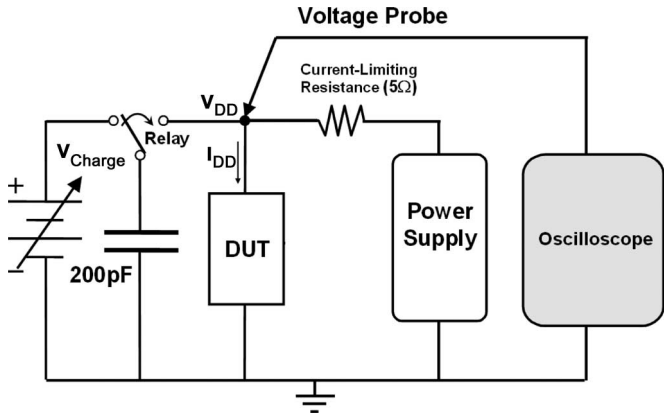


Fig. 13. Component-level TLU measurement setup with a bipolar trigger [13], [15].

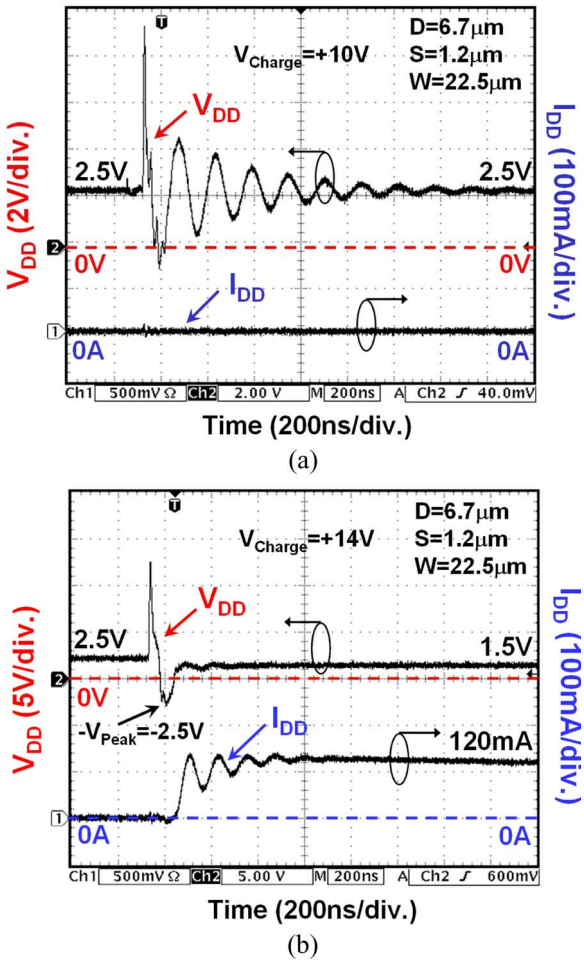


Fig. 14. Measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses of the SCR with $V_{\rm Charge}$ of (a) +10 V and (b) +14 V.

The measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses with $V_{\rm Charge}$ of +10 V and +14 V are shown in Fig. 14(a) and (b), respectively. The DUT (SCR) has layout parameters of $D = 6.7\ \mu$m, $S = 1.2\ \mu$m, and $W = 22.5\ \mu$m. With a smaller $V_{\rm Charge}$ of +10 V, $V_{\rm DD}$ is the intended bipolar trigger that is just similar to that under the system-level ESD test [16].

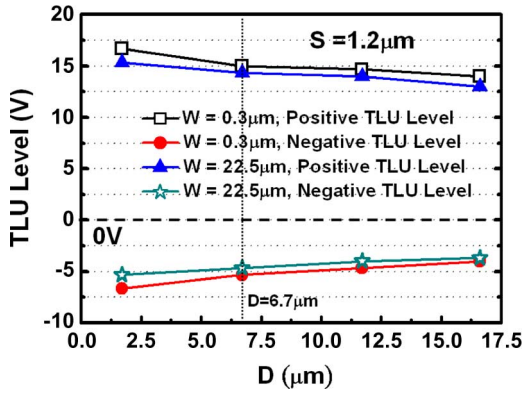


Fig. 15. Measured TLU levels of the SCR structures with various D's and W's but a fixed S of 1.2 μm. The magnitudes of negative TLU level ($<$ 9 V) of all the SCR structures are smaller than those of the positive TLU level ($>$ 13 V).

In addition, TLU does not occur because $I_{\rm DD}$ does not increase after applying the bipolar trigger on $V_{\rm DD}$, as shown in Fig. 14(a). TLU still does not occur until $V_{\rm Charge}$ increases up to +14 V. Once TLU is initiated, $I_{\rm DD}$ significantly increases up to 120 mA, and $V_{\rm DD}$ is pulled down to the latchup holding voltage of 1.5 V, as shown in Fig. 14(b). The measured waveforms in Fig. 14 can simulate the occurrence of TLU (or the voltage disturbance on $V_{\rm DD}$) in Figs. 2 and 3(a) under the system-level ESD test. Thus, this measurement setup can be used to evaluate the TLU dependence on $D_{\rm Factor}$ and $D_{\rm Freq}$ under the system-level ESD test.

B. Experimental Verification on TLU

The TLU levels of the fabricated SCR test structures with various geometrical parameters are shown in Fig. 15. The TLU level is defined as the minimum positive (negative) $V_{\rm Charge}$ which can initiate TLU. The magnitudes of negative TLU level ($<$ 9 V) of all the SCR structures are smaller than those of the positive TLU level ($>$ 13 V). With the measured bipolar-trigger waveform in Fig. 14(a), it can be extracted from (1) that $D_{\rm Freq}$ is about 8 MHz (duration is about 125 ns) and $D_{\rm Factor}$ is about $1.5 \times 10^6\ {\rm s}^{-1}$. From the simulation results in Fig. 7(a) and (b), $V_{\rm P-}$ is smaller than $V_{\rm P+}$ for a bipolar trigger with such $D_{\rm Freq}$ (8 MHz) and $D_{\rm Factor}$ ($1.5 \times 10^6\ {\rm s}^{-1}$). Thus, the experimental verifications in Fig. 15 are consistent with the device simulation results in Fig. 7.

The explanations of simulated TLU characteristics in Figs. 7 and 11 are based on the assumption that the minimum $-V_{\rm Peak}$ to initiate TLU is fixed for the same SCR structure. To experimentally verify this, a discharge resistor with a resistance of 1.5 kΩ is placed between the relay and the $V_{\rm DD}$ node in the TLU measurement setup. As a result, another bipolar trigger with a higher $D_{\rm Freq}$ and a larger $D_{\rm Factor}$ can be generated, as shown in Fig. 16. Fig. 16(a) shows the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses with $V_{\rm Charge}$ of +120 V. Compared with the measured $V_{\rm DD}$ waveform in Fig. 14(a), a higher $D_{\rm Freq}$ of 12.5 MHz (larger $D_{\rm Factor}$ of $1.5 \times 10^7\ {\rm s}^{-1}$) can be extracted from (1). In addition, TLU does not occur due to a larger $D_{\rm Factor}$, even though $V_{\rm Charge}$ is as high as +120 V.

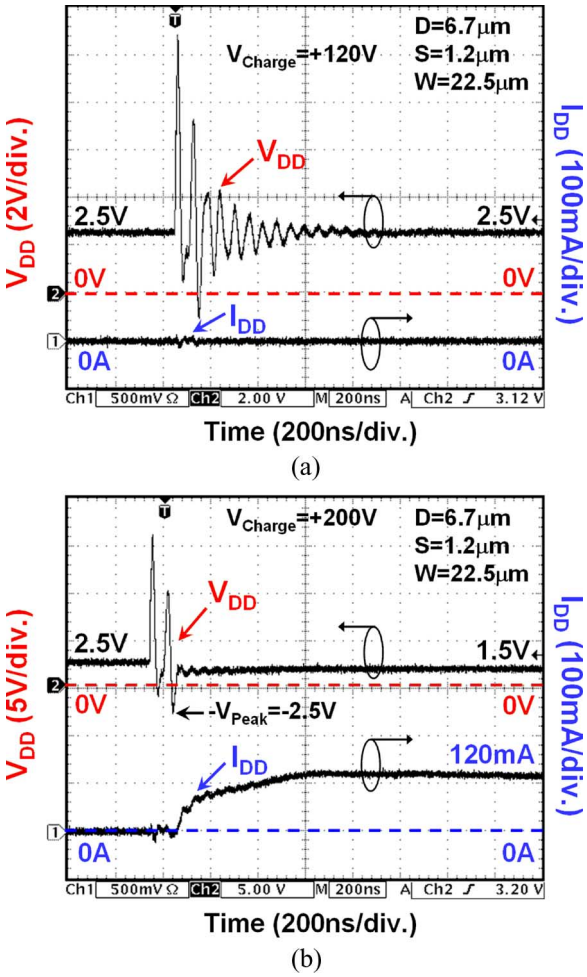


Fig. 16. Measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses, with a discharge resistor with a resistance of 1.5 kΩ between the relay and the $V_{\rm DD}$ node in the TLU measurement setup and also with a $V_{\rm Charge}$ of (a) +120 V and (b) +200 V. In Figs. 14(b) and 16(b), the minimum $-V_{\rm Peak}$ to initiate the TLU is fixed (−2.5 V) for the same SCR structure.

If $V_{\rm Charge}$ further increases, TLU still does not occur until $V_{\rm Charge}$ increases up to +200 V. Fig. 16(b) shows the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses with $V_{\rm Charge}$ of +200 V. In Figs. 14(b) and 16(b), the minimum $-V_{\rm Peak}$ to initiate TLU is fixed (−2.5 V) for the same SCR structure ($D = 6.7$ μm, $S = 1.2$ μm, and $W = 22.5$ μm), even though there are different $D_{\rm Freq}$'s and $D_{\rm Factor}$'s. Based on this result, the explanations of simulated TLU characteristics in this paper are indeed developed on a reasonable assumption.

The simulated TLU characteristics in Fig. 7(a) that $V_{\rm P+}$ increases with $D_{\rm Factor}$ can be also experimentally verified by the TLU measurements shown in Figs. 14(b) and 16(b). For the bipolar trigger with a larger $D_{\rm Factor}$ in Fig. 16(b), in order to compensate a larger voltage attenuation within the first cycle, a larger $V_{\rm Charge}$ (+200 V) is necessary to produce the same minimum $-V_{\rm Peak}$ (−2.5 V) to initiate TLU. As a result, the positive TLU level of +200 V in Fig. 16(b) is much larger than that of +14 V in Fig. 14(b), which is consistent with the simulation result in Fig. 7(a).

V. Conclusion

To clarify the correlations between TLU and bipolar-trigger noise, two dominant parameters of bipolar trigger—$D_{\rm Freq}$ and $D_{\rm Factor}$—have been characterized by device simulation to find their impacts on TLU. With the simulated TLU dependence on $D_{\rm Freq}$ and $D_{\rm Factor}$, the bipolar-trigger waveforms with $D_{\rm Freq}$ of several tens of megahertz can initiate TLU most easily. However, TLU is less sensitive to the bipolar-trigger waveforms with an excessively large $D_{\rm Factor}$ or an excessively low/high $D_{\rm Freq}$. The simulated TLU characteristics are useful to optimize the bipolar trigger in evaluating the TLU immunity of CMOS ICs without overestimation. Furthermore, the board-/chip-level noise filters can be properly designed to efficiently eliminate the ESD-coupled noise for the TLU prevention.

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