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Statistical study on the temperature dependence of the turn-on characteristics for p-type LTPS TFTs

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Abstract

In recent years, low temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) has been widely investigated for various applications to system-on-panel (SOP) technology. However, due to the complexity of grain boundary trap properties, the conducting behaviors of various LTPS TFTs are difficult to be analyzed systematically. In this paper, the common and device-dependent thermal effects are studied to understand the conduction mechanism in the LTPS TFTs.
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Keywords: LTPS TFT; Temperature dependence; Variation; Scattering mechanism

Low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted much attention for the higher mobility and better reliability compared to amorphous silicon thin-film transistors [1]. However, even the devices fabricated under the identical process, LTPS TFTs still have different electrical characteristics due to the influence from different numbers of the inter-grain and intra-grain defects [2,3]. The defects in polysilicon can severely limit the device performance and cause device variation, which make difficulty to design the circuit with LTPS TFTs [4]. The variation is intrinsically introduced by statistical fluctuations in manufacturing processes. However, for a single device, the defects do not change, and thus the thermal effects can be distinctively considered. In this paper, the device variation and temperature dependence are crosschecked to analyze the turn-on characteristics of LTPS TFTs statistically. The investigation into the common and device-dependent thermal behaviors is helpful to develop the LTPS TFT model with temperature effects.

The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a 50 nm thick a-Si:H film were deposited on glass substrates with plasma-enhanced chemical vapor deposition (PECVD). The samples were then put into the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 80 nm SiO_2 and 40 SiN_x films were deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. Then, the interlayer of SiN_x was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work. In this study, the p-type TFTs with a channel width of 20 μm and a channel length of 6 μm are fabricated. The average grain size and interface roughness of the

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polysilicon layers are about 330–380 nm and 10–15 nm. The mobility of the investigated TFTs are about 92 cm^2/V s. The experiments were measured using an HP 4156 semiconductor parameter analyzer at different temperatures.

The turn-on characteristics of one p-type LTPS TFT at different temperatures are shown in Fig. 1. A common cross point of the I_d–V_g curves at the cross voltage V_x is firstly noticed. At the gate voltage (V_{gs}) below V_x, the drain current increases with the temperature, while the opposite temperature dependence is observed at higher V_{gs}. The temperature dependence of the transconductance also changes from positive to negative at even lower gate voltage. It indicates that the superior conducting mechanisms at high and low V_{gs} are different. At low voltages, the carrier number increase with temperature since more holes can overcome the defect induced potential barriers. In addition, when the temperature gets up, the carriers pass through the area near the trap centers more frequency because the holes move faster. On the contrary, at high V_{gs}, the decrease of the holes mobility at risen temperature is attributed to the more significant lattice scattering [5]. This phonon scattering is so important that the increase owing to the less Coulomb scattering for higher carrier velocity and more carriers induced is overwhelmed. The activation-energy can be extracted from the slope of the Arrhenius plot and the curve of activation-energy and V_{gs} is shown in Fig. 2. This figure shows that the Arrhenius plot of the drain current has positive activation-energy Ea decreasing with increasing the gate voltage in low mobility TFTs, whereas in high mobility TFTs the Arrhenius plot has negative activation-energy increasing with V_{gs}.

It is believed that the phonon scattering for various TFTs is similar since the lattice structure of polysilicon is alike. However, the defects in the grain boundary are different from device to device. Thus, many TFTs are measured to investigate the thermal effect statistically. Fig. 3 shows the temperature dependences of maximum field effect mobility μ_{max}. The relative standard deviation of mobility

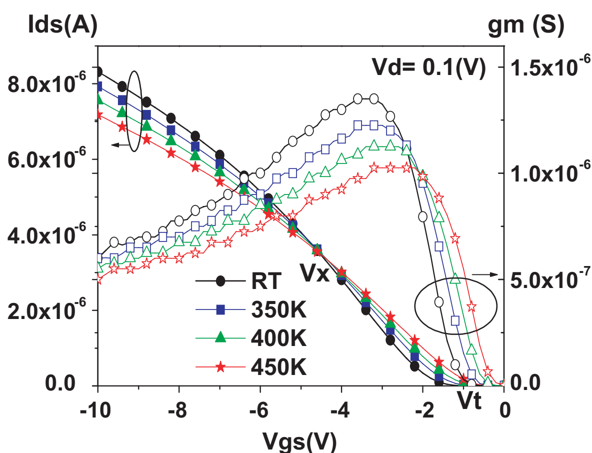

Fig. 1. The gate voltage dependences of drain current and transconductance for a p-type LTPS TFT at different temperatures.

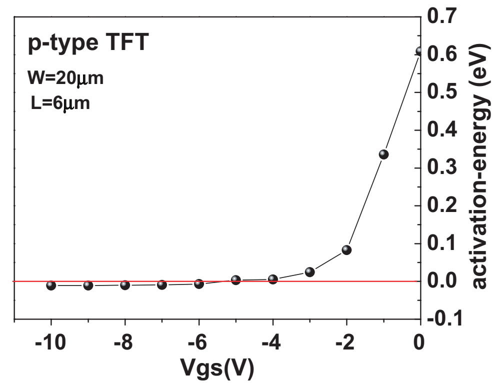

Fig. 2. Curves of activation-energy as a function of the gate voltage.

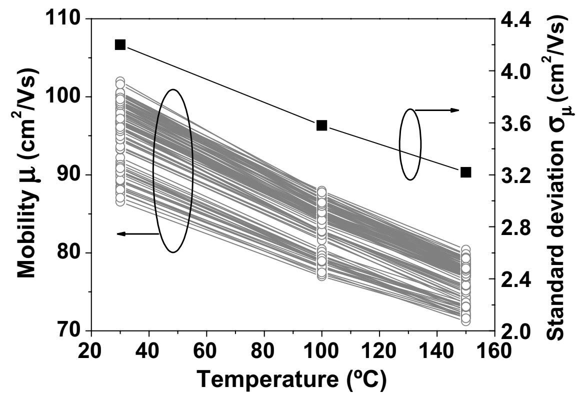

Fig. 3. The temperature dependences of effective mobility μ_{ave} for the individual TFTs with their average μ_{ave} and standard deviation σ_{μ}.

μ_{max} is also plotted. For all the devices, negative temperature dependence is observed. Furthermore, the variation of diverse devices decreases with the rise of temperature. By the thermionic emission, most of the carriers can jump over the defect induced potential barriers. In the mean time, the thermal energy can help the holes to run over the scattering of charged traps. Therefore, less Coulomb influence of the traps and the similar lattice structures in the grains lead to the dominance of the phonon scattering [6], and thus the variation range decreases. Even though the lattice scattering thermally prevails, the temperature dependences for the distinct devices are not exactly the same, which reveals the existence of other mechanisms such as Coulomb one.

The cross voltage V_x is a good indication about the balance of invariant phonon scattering and defect-related conducting mechanism. Since both V_x and V_t of the TFTs vary with devices, the relative gate voltage is used instead of the real V_{gs} value to analyze the behavior of the field effect mobility. Fig. 4 illustrates the average mobility μ_{ave} and the relative mobility deviation σ_{μ}/μ_{ave} in the region between the cross voltage V_x and the threshold voltage V_t in accordance with the relative V_{gs}. As can be seen, the trend of average mobility is the same as that of a single device, which reflects the common behaviors of the TFTs. Moreover, the relative mobility deviation is large at the voltage close to V_t and at lower temperature where

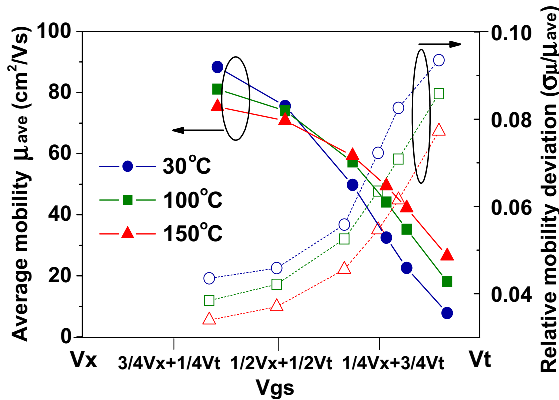

Fig. 4. The average mobility μ_{ave} and the relative mobility deviation σ_{μ}/μ_{ave} in accordance with the relative V_{gs} in the region between V_x and V_t.

the characteristics of TFTs are profoundly affected by the defects.

The Fig. 5 shows the relationship of $|V_x–V_t|$ verse mobility extracted where the transconductance gives maximum for the poly-Si TFTs. It is clear that for the device having absolute lower $V_x–V_t$ value, its mobility is relative large, because the carriers is not easily occluded by potential barrier. It indicates that $|V_x–V_t|$ can be declared whether the LTPS TFT conductance characteristics are better or not. This range can describe the number of traps in the TFT device, too. On the contrary, for the device with the crossing voltage at more negative gate bias, the phonon scattering effect prevails later because of the larger number of defects, which results in the lower mobility.

The balance of scattering mechanism is reviewed by changing the drain voltage. Fig. 6 shows cross voltages shift with different drain voltage. When the drain voltage increases, owing to drain induced grain barrier lower (DIGBL) [7], the influence of the defects is reduced. The carriers which originally are retarded by the phonon vibration centers, gain energy from higher electrical field to accelerate and meanwhile the reduction of change ratio for the drain current with different temperatures, thus the increase of $|V_x–V_t|$ is observed.

The cross voltages shift with different drain voltage is shown in Fig. 7. At the quite high drain voltage, e.g.

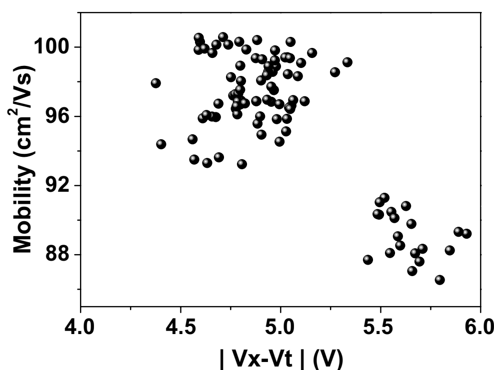

Fig. 5. The comparisons of $|V_x–V_t|$ verse mobility for much p-type poly-Si TFTs at room temperature.

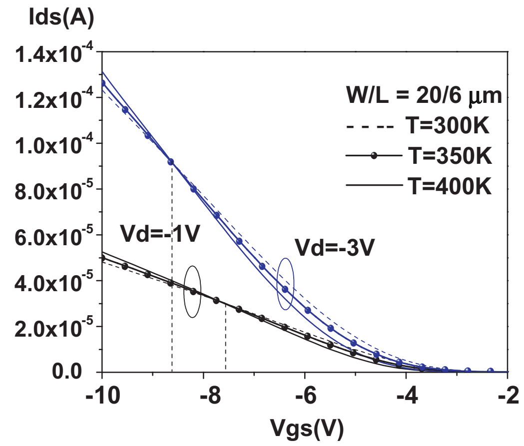

Fig. 6. Variation of current with gate voltage at $V_d = -1$ and -3 for $W/L = 20/6$ µm dimensions at various temperature.

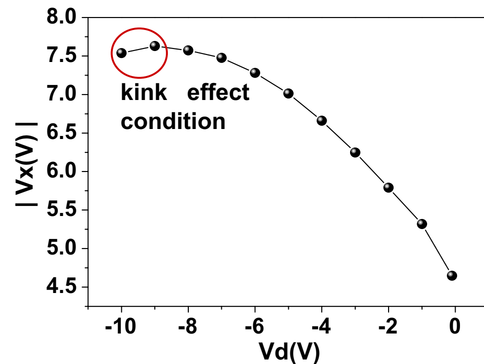

Fig. 7. The cross voltages shift with different drain voltage.

-10 V, where the effect of defects becomes minor, the V_x swerves to shift positively. It is because the impact ionization is strongly enhanced. In the p-channel TFT, the kink effect is increased as the temperature is increased. The cross voltage inverse with drain voltage is also observed.

Conclusion: LTPS TFTs suffer from serious device characteristic variation due to the number and behavior of defects of the polysilicon film. This paper has reported the temperature dependence and the cross voltage concerning the conduction mechanisms of poly-Si TFTs. The difference between the cross voltage and threshold voltage may also be an index for the turn-on characteristics of the LTPS TFTs. This investigation for thermal behaviors statistically are helpful us to develop the accurate LTPS TFT model with temperature effects. We performed numerical simulations quite well can be adjusted by fitting the device transfer characteristics and the method to predict kink effect of poly-Si TFT.

Acknowledgements

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References

[1] Lee JW. In: Electron devices meeting, 1998. IEDM 98 Technical Digest, International, 1998.
[2] Bhat GA, Kowk HS, Wong M. Solid-State Electron 2000;44:1321–4.
[3] Chan VWC, Chan PCH, Yin C. IEEE Electron Dev 2002;49:1384–91.
[4] Wang AW, Saraswat KC. IEEE Electron Devices 2000;47:1035–43.
[5] Sehgal A, Mangla T, Gupta M. Solid-State Electron 2005;49:301–9.
[6] Mori H, Hata K, Hsahimoto T, Wu I-W, Lewis AG. Ja J Appl Phys 1990;30:3710–4.
[7] Lin PS, Guo J-Y, Wu C-Y. IEEE Trans Electron Dev 1990;37(3):666.