Design of a DVB-T/H COFDM Receiver for Portable Video Applications

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ABSTRACT

Mobile video services have generated a lot of interest recently. To reach a cost-effective solution, design trade-offs among system performance, hardware complexity, and power consumption must be considered in the early design phase of such applications. In this article, we present a system overview, simulation platform, and hardware design of a DVB-T/H baseband receiver. Starting with a design platform, several algorithms on both inner and outer receivers are developed to meet target system performance under different channels. Then, system architecture and related key modules are explored, taking into account both silicon area and power consumption. Finally, several design issues related to the integration of the proposed DVB-T/H inner and outer receivers are addressed.

INTRODUCTION

To provide digital video services on handheld terminals in a mobile environment, the terminal devices must be customized for better mobility and battery-life usage. Nowadays, several orthogonal frequency-division multiplexing (OFDM)-based standards are designed for such applications and will share this market. These standards are terrestrial digital multimedia broadcasting (T-DMB), integrated services digital broadcasting-terrestrial (ISDB-T), digital video broadcast-handheld (DVB-H), and mediaFLO. The T-DMB is based on a digital audio broadcasting (DAB) system and improves the error correction part of a DAB system. The ISDB-T is a band-segmented transmission (BST) OFDM-based system that consists of a set of common basic frequency blocks. The mediaFLO and DVB-H use the coded orthogonal frequency division multiplexing (COFDM) modulation method. Some comparisons and survey work were recently reported in [1]. The DVB-H [2] system, enhanced from the digital video broadcasting-terrestrial (DVB-T) [3] broadcasting system, is proposed for such environments. In addition, because of provided data rates in DVB-H services and the small-size displays of typical handheld devices, video coding methods, such as H.264/AVC (advanced video coding) and other high-efficiency video-coding standards are proposed [4].

In this article, we present a design case of DVB-T/H baseband receiver design. We focus on algorithm development, architecture design, and system-level integration for the receiver. In addition to meeting system performance requirements, we also consider reducing power consumption at different design phases. In the initial phase, we construct a *MATLAB* [5] simulation-based platform, where we can concentrate on algorithm development, to meet performance requirements under different specified channel environments. Each algorithm/functional module is verified by the proposed platform via performance evaluation. In the architecture design phase, we check both data flow and computational loads among all functional modules to achieve a cost-effective solution. For system-level integration, several silicon IP for both inner and outer receiver parts are developed and integrated in 0.18 μm complementary metal-oxide semiconductor (CMOS) process. This test chip occupies 6.9×5.8 mm^2 and consumes 250 mW at the highest data rate specified in a DVB-T/H system.

The rest of this article is organized as follows. First, an overview of the DVB-T/H baseband processing is given, where the major differences between DVB-T and DVB-H are highlighted. Then, we introduce our design flow including algorithm development, architecture design, and system-level integration. Several memory-efficient methods and low-power techniques are described and discussed. Then a test chip with measurement results is presented.

OVERVIEW OF DVB-T/H BASEBAND SYSTEM

A block diagram of the DVB-T transmitter is shown in Fig. 1a [3]. The input transport stream is mainly from MPEG-2 artworks. There are two steps in the channel coding: one is the outer coder, a Reed-Solomon (RS 204,188) coder; the other is a punctured convolutional coder. In addition, the corresponding interleaving methods (i.e., outer and inner interleaver) are adopted. If required, the inner interleaver can integrate two channel-coded streams into a single slot when the transmitter is working in hierarchical mode. The mapper module is using three constellation schemes: quadrature phase-

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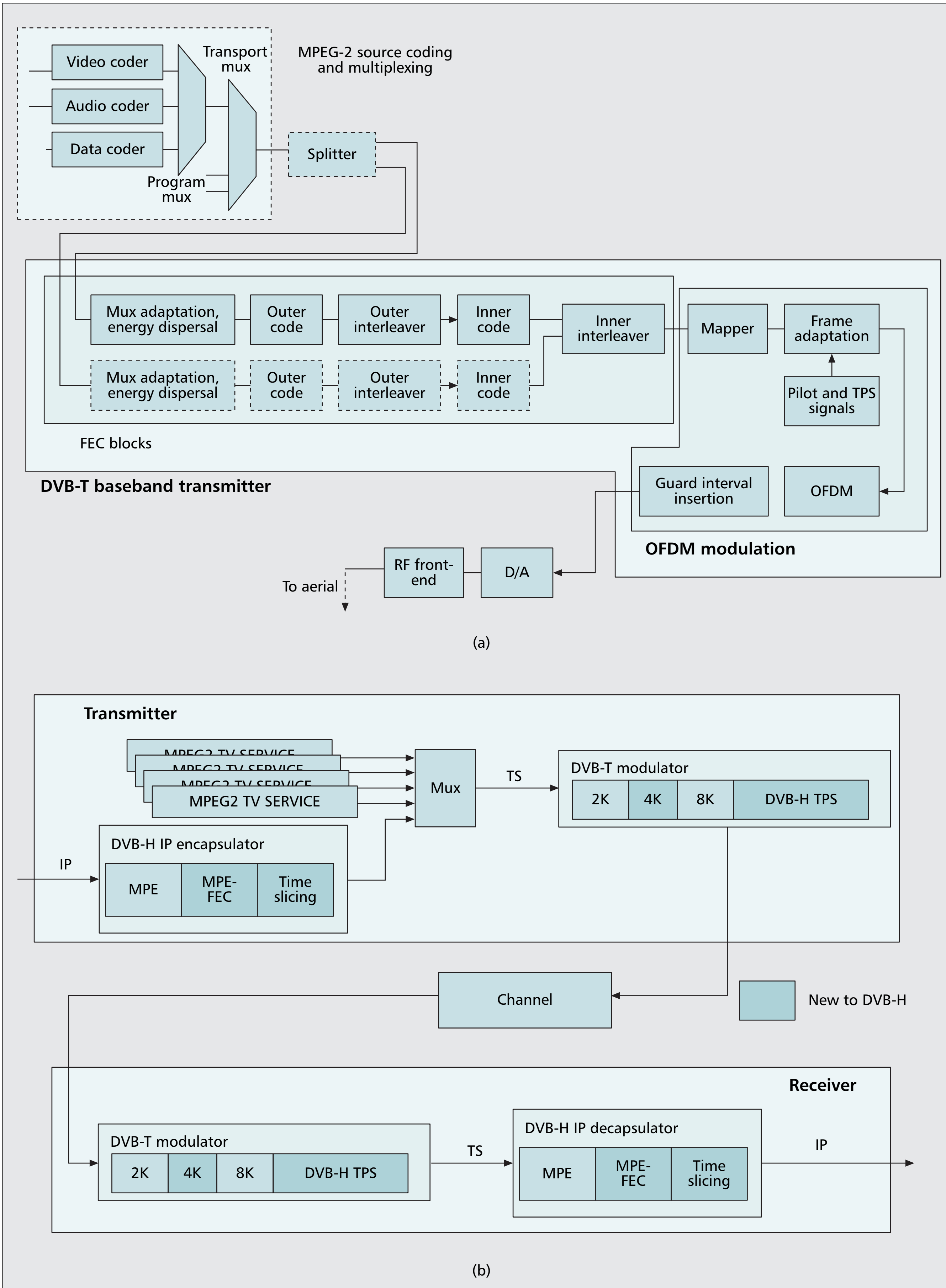


■ **Figure 1.** *Block diagram of DVB-T/H system: a) DVB-T baseband transmitter; b) DVB-H system.*

Basically, cell-based CMOS IC design flow is adopted in the second phase. In the hardware description language (HDL) coding step, if the synthesized HDL codes cannot meet power, speed, and area requirements, we go back to the first phase to refine the system algorithms and architectures.

shift keying (QPSK), 16 quadrature amplitude modulation (QAM), and 64 QAM to transform bit information into complex data. Before the follow-up OFDM modulation, the transmission parameter signal (TPS) is inserted into the DVB frequency-domain frame structure. Meanwhile, both scattered and continual pilots are included for synchronization and channel estimation on the receiver side. The OFDM module conducts an inverse fast fourier transform (IFFT) operation to convert 8K or 2K mode symbols into time-domain symbols. In the last step, cyclic prefix of the time-domain symbols are inserted to prevent multipath interference before passing to the radio frequency (RF) front-end module. All basic modules of DVB-T baseband receiver are inverse operations of transmitter blocks.

Figure 1b shows an overview of a DVB-H baseband processing system [2] derived from the existing DVB-T standard. The payload of DVB-H includes IP datagrams or other network layer datagrams encapsulated into multiprotocol encapsulation (MPE) sections [6] and then passed to an MPEG-2 multiplexer that is shared by other MPEG-2 TV services.

The major differences between DVB-T and DVB-H baseband processing are the following: 4K OFDM mode, in-depth interleaver, updated TPS code, and additional 5-MHz channel bandwidth. In the data link layer, an additional multiprotocol encapsulation-forward error correction (MPE-FEC) [6] frame structure is used. In addition, the suspend mode of baseband processing must be developed for the time-slicing operation. These new features are added to improve system performance and to reduce the average power consumption in DVB-H mode. Note that the new 4K mode OFDM is adopted for trading off mobility and single-frequency network (SFN) cell size, enabling single-antenna reception at high speeds. The time-slicing operation is a method to transport lower bandwidth requirement data in usable higher-provided bandwidth, and it could suspend the RF and baseband modules to reduce power consumption. The in-depth interleaver uses an existing 8K mode interleaving method to perform the interleaving operation in 4K/2K OFDM symbols to reduce probability of burst errors [7, 8]. A more in-depth discussion on system behavior and performance analysis of the DVB-H system can be found in [9]. Note that performance improvement of the MPE-FEC and power saving via the time-slicing operation mode are the main research topics of interest for the DVB-H system.

DVB-T/H Baseband Receiver Design

Our receiver design schedule includes two phases: algorithm development and integrated circuit (IC) implementation. For the former, we use the MATLAB simulation-based platform to develop various algorithms to meet system specifications. The main task in this domain is focusing on algorithm development and fixed-point word-length analysis. When several algorithms are developed to meet system specifications, all functional modules must transfer to fixed-point simulation to evaluate required word-length of each internal signal with minimum performance loss. After signal word-lengths are confirmed, these fixed-point simulation results are reserved and prepared for test bench coding in the follow-up IC implementation phase.

Basically, cell-based CMOS IC design flow is adopted in the second phase. In the hardware description language (HDL) coding step, if the synthesized HDL codes cannot meet power, speed, and area requirements, we go back to the first phase to refine the system algorithms and architectures. Meanwhile, the refined algorithms must meet the performance requirement for system specifications.

All modules in IC implementation are checked by specified testbenches from the algorithm development phase. This procedure can guarantee that the behavior of all modules in IC implementation corresponds to the functional blocks defined in the algorithm development phase.

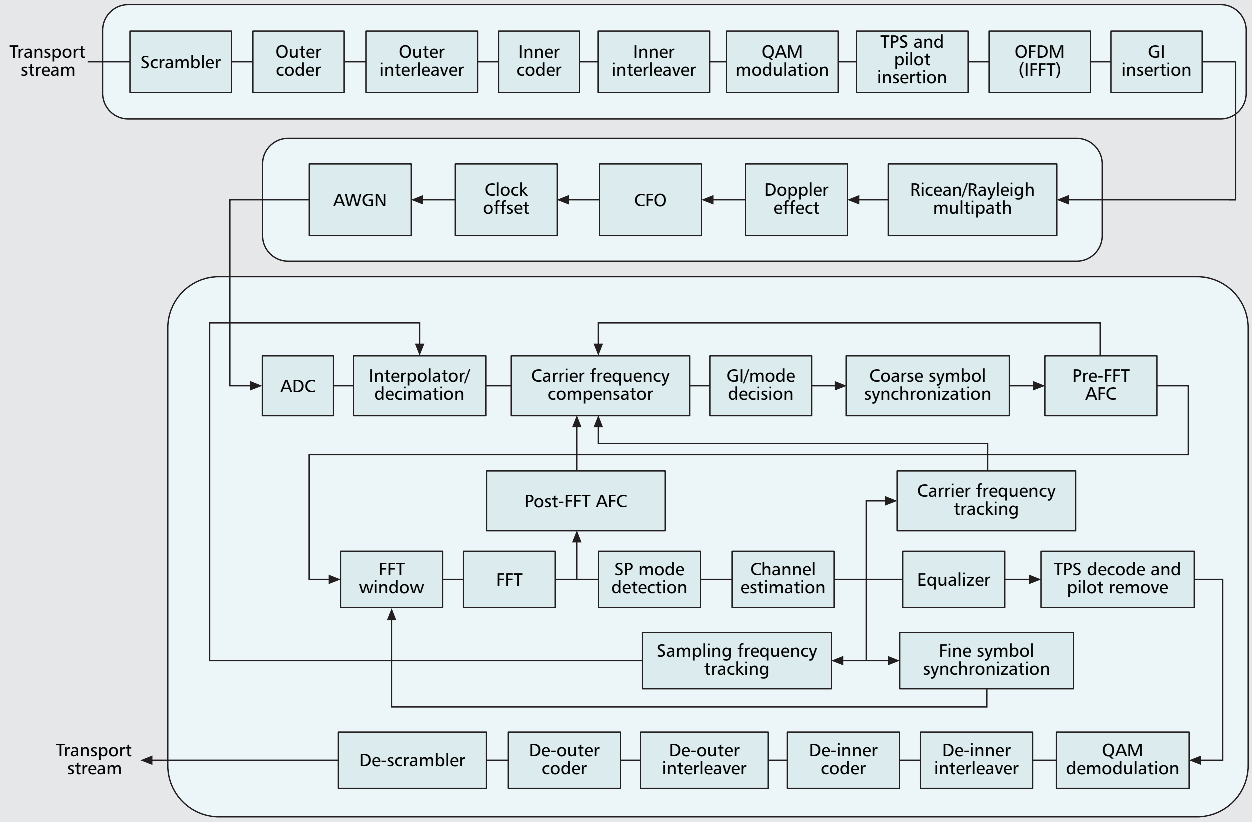
For algorithm design, we build a simulation platform to observe overall system behavior and evaluate performance results of our proposed schemes under different channel conditions. For the architecture design, we double check the I/O behavior of each module and analyze data flow among different modules so that redundant operations can be removed without degrading the overall system performance. In addition, specific memory organization and data reuse schemes are developed to reduce memory accesses. Finally, we propose power-saving schemes in computation-intensive modules to reduce power consumption, such as in a fast fourier transform (FFT) processor, Viterbi decoder, and outer interleaver.

Simulation Platform Design

Our proposed simulation platform includes a transmitter, channel models, and a receiver as shown in Fig. 2a. The transmitter includes channel coding and OFDM modulation as defined in the standard. The channel coding includes the scrambler, RS encoder (outer coder), outer interleaver, punctured convolutional encoder (inner coder), and inner interleaver. A QAM modulator supporting QPSK, 16 QAM, and 64 QAM is applied to the OFDM modulation. Both TPS coding and pilot insertion are performed before the IFFT operation. The IFFT operation must support three modes of IFFT: 8K and 2K mode operations for the DVB-T system and a 4K mode operation for the DVB-H system.

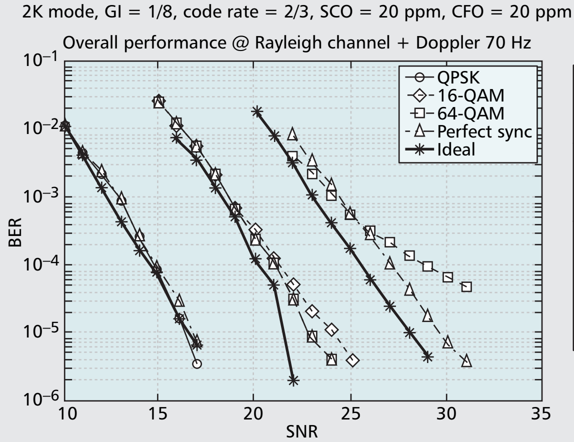
For channel models, the multipath profiles are developed based on [4]. In addition, the following effects are taken into account: Doppler effect, carrier frequency offset (CFO) effect, sampling clock offset (SCO), and additional white gaussian noise (AWGN).

The receiver covers both inner and outer modules, where the former targets synchronization and OFDM demodulation, and the latter performs channel decoding operations. The inner receiver includes timing synchronization, frequency synchronization, the FFT operation, channel equalization, and TPS decoding. The inter-symbol interference (ISI) effect will destroy the orthogonality of OFDM symbols and hence



(a)

2K mode, GI = 1/8, code rate = 2/3, SCO = 20 ppm, CFO = 20 ppm



Performance comparison about Doppler effect

	Proposed design	DiBCom DIB7700-P[14]	DiBCom DIB7000-H[14]
Doppler tolerance	70 Hz @ 2K mode *1 20 Hz @ 8K mode *1	10 Hz @ 2K mode *2	130 Hz @ 8K mode *3
System condition	*1: 64QAM, GI = 1/8, code rate = 2/3, Rayleigh channel with Doppler effect *2: 64QAM, GI = 1/32, code rate = 2/3, TU6 mode *3: 16QAM, GI = 1/4, code rate = 1/2, TU6 mode		

(b)

Figure 2. *The proposed DVB-T/H baseband simulation platform: a) system data flow; b) performance results (left) and comparison (right).*

must be minimized. Here, we propose a three-stage timing synchronization scheme to identify symbol location to avoid ISI and reduce the timing offset of received signals as well. In the first stage, the timing synchronizer uses the normalized maximum correlation method to detect the operation mode (2K, 4K, or 8K) and guard interval ratio (1/32, 1/16, 1/8, or 1/4) of the received signal. Meanwhile, the synchronizer locates the coarse symbol boundary. The second stage (fine symbol synchronization) and the third stage (timing tracking) are operated separately in the frequency domain. The fine symbol synchronization exploits the linear phase rotation of scattered pilots in each OFDM symbol to estimate symbol timing offset. Then the symbol boundary is updated. In the third stage, we calculate the phase drift of continual pilots in the same subcarrier location between continuous OFDM symbols, because this phase drift is caused by sampling clock offset. To reduce sampling clock offset, the phase drift information is passed to the interpolator at the input of baseband receiver to resample receiving signal.

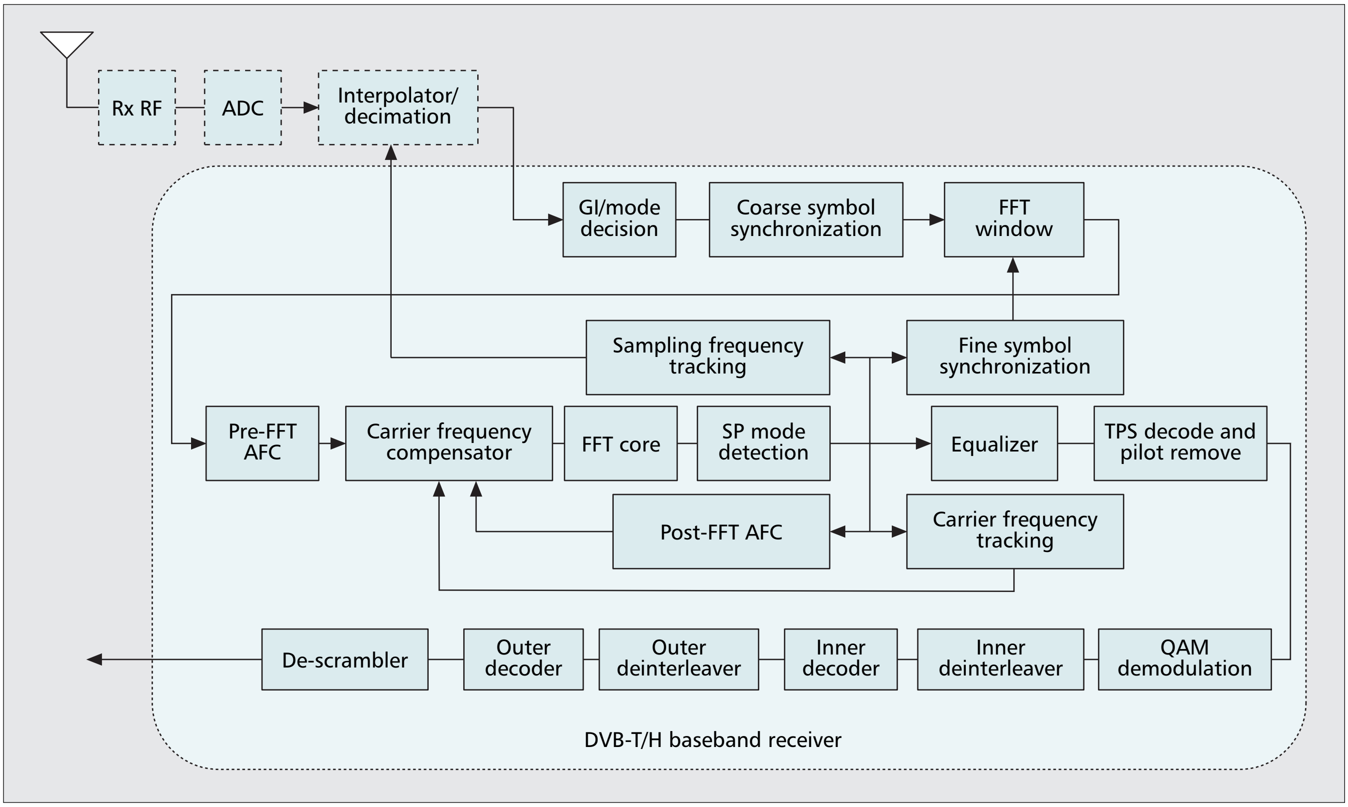


Figure 3. *The proposed DVB-T/H baseband receiver.*

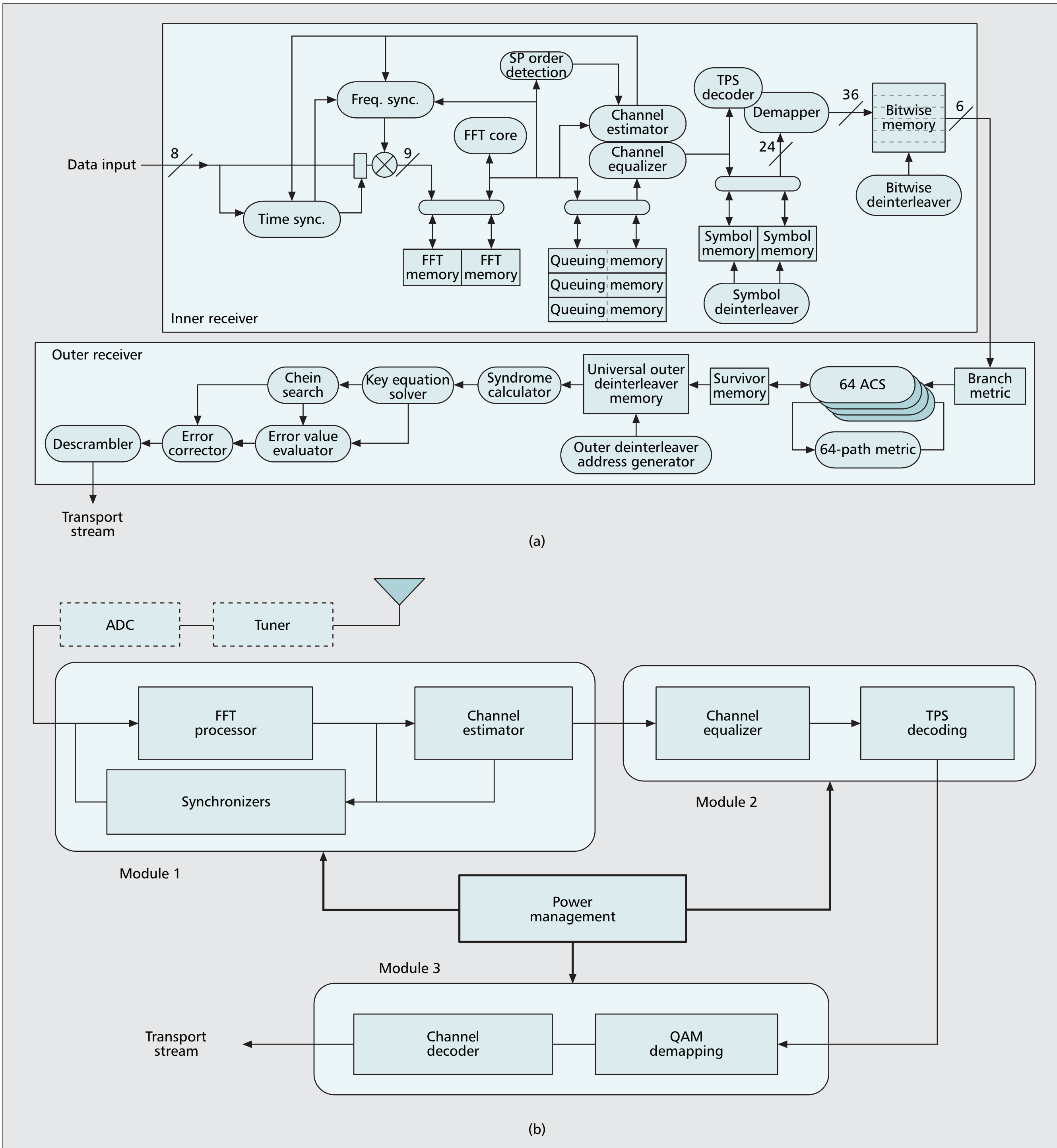
In OFDM systems, the carrier frequency offset (CFO) effect will contaminate the signal in each sub-carrier and cause inter-carrier interference (ICI). To reduce ICI and overcome the Doppler frequency drift, a three-stage frequency synchronization scheme is developed to estimate the fractional part of the CFO in time-domain and the integer part of the CFO in the frequency-domain. Then, a CFO tracking scheme is used to reduce the residual CFO. The first stage is to estimate the phase rotation between the guard interval and the copied data in the OFDM symbol for the fractional part of the CFO. The integer part of CFO is estimated in the frequency-domain by a guard band detection method in the second stage. In the third stage, we apply a joint SCO/CFO tracking scheme to estimate the residual CFO and Doppler frequency drift. Outputs from these three-stage estimation/tracking schemes are then exploited to compensate the CFO effects.

To support variant-length FFT operation, a radix-8 hierarchical memory-based FFT processor [10] is exploited to realize 2K/4K/8K FFT operations. In the channel equalizer design, we apply two 1D linear interpolators for channel estimation and zero-forcing method for channel equalization. Note the TPS code contains the information required for demodulation and channel decoding, such as guard interval ratio, transmission mode, QAM method, hierarchical information, and the code rate of the punctured convolutional code. This TPS decoder uses a voting scheme to decide the final answer from a TPS information set in TPS carriers. A 64-level soft-decision QAM demodulation is used to improve the system performance gain.

A path-merging and path-prediction Viterbi decoder [11] is adopted in the outer receiver. It can adjust the traceback length and memory accessing times based on the results from the inner receiver. For the outer de-interleaver, we design a 2D address generator unit that can perform the de-interleaving operation in a single one-port memory. The RS decoder applies the decomposed key equation solver to achieve better area efficiency [12].

To overcome the Doppler effect in a mobile environment, a robust channel equalizer with CFO tracking is required. From mathematical analysis, the Doppler effect can be modeled as a dynamic CFO drift in each sub-carrier of the OFDM symbol. The Doppler tolerant range of the proposed design is limited by channel equalization and CFO tracking schemes. Here we adopt two 1-D linear interpolators for channel estimation and a joint SCO/CFO tracking scheme for frequency synchronization to overcome this frequency drift issue. Our proposed system can tolerate a Doppler effect of 70 Hz in 2K mode and 20 Hz in 8K mode under the following conditions: Rayleigh multipath with a signal-to-noise ratio (SNR) loss of less than 2 dB.

Figure 2b shows an example of the floating-point performance results under the following conditions: 2K mode, GI=1/8, coding rate=2/3, SCO=20 ppm, CFO=20 ppm, Rayleigh multipath channel with a Doppler effect of 70 Hz. Also, a brief comparison of our proposal with other solutions in terms of the Doppler tolerance range is shown in the left-hand side of Fig.



■ **Figure 4.** *Proposed hardware architecture for the DVB-T/H baseband receiver: a) receiver structure; b) sequential power management.*

2b. Note that different channel conditions and transmission parameters may result in different Doppler performance results.

Architecture Design

A block diagram of the proposed DVB-T/H baseband receiver is shown in Fig. 3. The proposed design is composed of synchronization units, a 8K/4K/2K FFT processor, a 2-D channel equalizer, a TPS decoder, an inner de-interleaver, a Viterbi decoder, an outer interleaver, and an RS (204, 188) decoder.

Inner Receiver Design — The structure of the inner receiver is shown in Fig. 4a. When data arrives, the timing synchronization system detects key parameters for the OFDM frame structure, including operation mode (8K/4K/2K) and guard interval ratio (1/4, 1/8, 1/16, 1/32). After detecting the operation mode and guard interval ratio, the coarse symbol boundary is determined by the normalized maximum correlator. In the meantime, the fractional part of the CFO is estimated based on the phase rotation between guard interval data and partial symbol data. The FFT

> In the initial phase, only two synchronization units and the FFT processor must be activated for timing and CFO estimation. Hence, the PM turns off the clock trees and holds the signal transition from channel equalizer to descrambler.

core performs the FFT operation when one complete OFDM symbol is received. The FFT core is based on a radix-8 butterfly unit with a 64-word pre-fetch buffer and dynamic scaling method to reduce word length [10].

The scatter pilot (SP) order detection and post-FFT CFO estimation is activated right after the FFT symbol is processed. These two functions require three OFDM symbols to detect the SP order and to compute the integral part of the CFO that is used to compensate FFT input data to reduce ICI effect. After detecting SP order, the channel estimator extracts SP information from the OFDM symbol. To obtain correct channel frequency response (CFR), the channel estimator requires four OFDM symbols to obtain 2D CFR information. Using two half-size queuing memory and retiming access schemes, only three symbol-size memory blocks are required for stored data. After the channel estimator collects sufficient CFR information, the channel equalizer equalizes data that will be sent to the symbol de-interleaver memory.

After the channel equalizer starts outputting data, we must decode the TPS containing operation mode, QAM modulation method, guard interval ratio, symbol interleaving order, and coding rate of the inner decoder. Without the decoded TPS information, the inner de-interleaver, QAM receiver, and outer receiver cannot be activated. The complete TPS information is embedded in one OFDM frame (68 OFDM symbols) of the DVB-T/H frame structure, implying at least one OFDM frame is required to collect complete TPS codes.

In the final stage of this inner receiver, two operations must be performed: QAM demodulation and inner de-interleaving. We exchange the symbol de-interleaving operation order before the QAM demodulation to reduce memory overhead when the word-length of the soft-decision QAM demodulation is longer than that of the channel equalization output. Based on this reordering scheme, the required word length of the symbol de-interleaving memory is reduced from 36-bit to 24-bit, saving about 145 K-bit memory space.

For each bit-wise interleaving section, the symbol de-interleaver outputs 126 de-interleaved data to a 64-level soft decision QAM receiver. The QAM receiver outputs the demodulated data that are stored into bit-wise de-interleaving memory. After 126 demodulated data are filled into bit-wise interleaving memory, both the symbol de-interleaver and the QAM receiver will hold until the bit-wise de-interleaver transfers one complete section data.

Outer Receiver Design — The structure of the outer receiver is also shown in Fig. 4a. The Viterbi decoder receives bit-wise de-interleaver data to decode punctured convolutional code. The outer de-interleaver can be realized by the general memory structure with a specific address generator. The required memory space can be reduced depending on the RS (204,188) decoding length. There are five steps in the RS (204,188) decoder: namely, syndrome calculator, key equation solver, chien search, error value evaluator, and error corrector. At the output of the RS decoder, the descrambler decodes the scrambled data stream except for the synchronization words.

System Level Power Management Unit

The tasks allocated in this receiver design can be divided into three working phases: namely, the initialization phase, equalization phase, and channel decoding phase. We develop a multi-stage power management (PM) in the proposed receiver to schedule these tasks working in different phases to reduce power consumption and minimize signal transition activities. Figure 4b shows the sequential power management for this test chip.

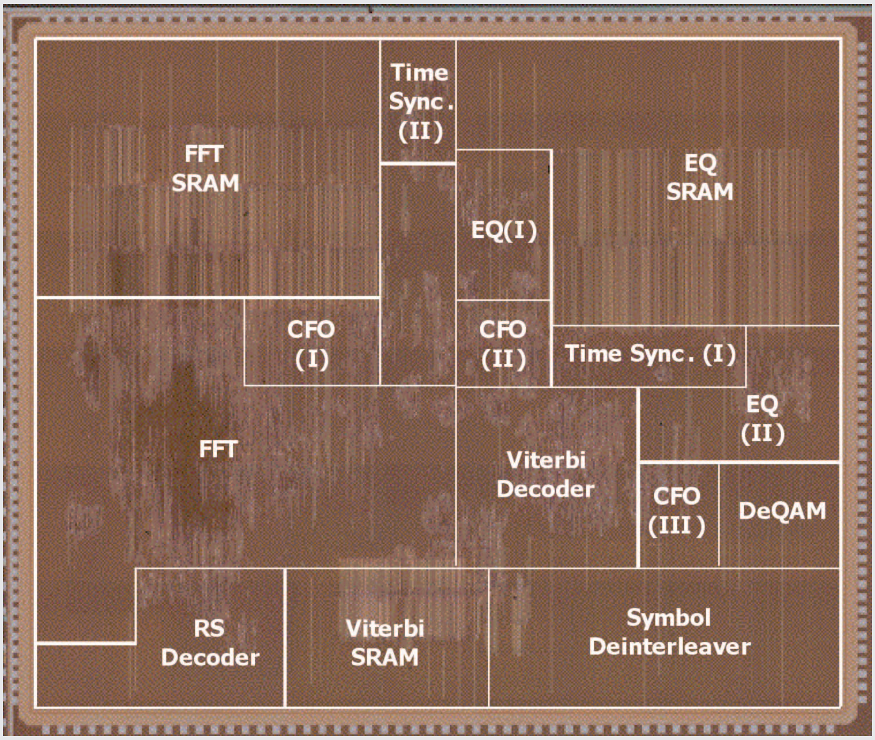
In the initial phase, only two synchronization units and the FFT processor must be activated for timing and CFO estimation. Hence, the PM turns off the clock trees and holds the signal transition from channel equalizer to descrambler. After the acquisition of the timing and CFO estimation, the receiver enters the equalization phase, where the PM turns on both the channel equalizer and the TPS decoder to get the TPS code in one DVB-T/H frame. Once the TPS decoding is correct, the PM starts to turn on the clock tree of the outer receiver and allows only signal transition in data compensation, demodulation, and decoding. Hence, signal switching activities are further reduced to save more power consumption.

Figure 5b shows the summary of power saving schemes we used. These schemes are adopted in algorithm, architecture, and system-level implementation. They can be classified into three types:
- Memory access time reduction
- Word-length reduction
- Redundant power elimination

In the FFT module, the hierarchical memory structure can reduce memory access time, and the dynamic scaling approach can keep the data accuracy without increasing extra word-length. The soft-decision de-QAM reordering can avoid increasing word-length in the symbol de-interleaver. The path-merging and path-prediction schemes can reduce the access time of survival memory of Viterbi decoder. The single memory structure with the specific address generation unit (AGU) in the outer de-interleaver can reduce the number of memory banks. Finally, the PM unit eliminates the redundant power consumption of this receiver processor in both initialization and equalization phases.

Implementation Results

A DVB-T/H COFDM baseband test chip [12] using the aforementioned techniques was designed and fabricated in a 0.18 μm single-poly six-metal CMOS process with an area of 6.9 × 5.8 mm^2. The logic gate count is about 371 K, and the overall embedded memory size is about 158 kilobytes. Figure 5a shows the microphoto of this test chip containing both inner and outer receivers. The largest module and main power consumer of the test chip is the FFT processor, with dual-bank embedded memory, occupies about 40 percent of the total area and consumes



(a)

	Used schemes	Effects
FFT operation	Hierarchical memory structure	Lower memory access power
	Dynamic scaling	Wordlength reduction
Reordering De-QAM	Reordering operations	Storage space reduction
Viterbi decoder	Path merging, path prediction	Less memory access power
Outer de-interleaver	Single memory structure with specified address generator	Less memory access power
Power management	Multiple operation phases	Redundant power elimination

(b)

■ **Figure 5.** *a) Chip microphoto; b) power saving schemes in the test chip.*

In the FFT module, the hierarchical memory structure can reduce memory access time, and the dynamic scaling approach can keep the data accuracy without increasing extra word-length. The soft-decision de-QAM reordering can avoid increasing word-length in the symbol de-interleaver.

44 percent of total power consumption. The overall power consumption is about 250 MW at the highest data rate (31.67 Mb/s) of DVB-T/H system specifications.

Conclusion

In this article, we present a single-chip COFDM-baseband receiver based on DVB-T/H specifications. Several techniques covering algorithm design and architecture exploration to reach a cost-effective solution were reported. Specifically, reducing storage space and minimizing switching activities are explored to reach a better power consumption index. A test chip demonstrates that a low-power and highly-integrated DVB-T/H baseband receiver can be effectively realized in a 0.18 µm CMOS process for portable video applications.

Acknowledgment

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Additional Reading

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