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(54) **METHOD FOR FABRICATING A RESISTOR FOR A RESISTANCE RANDOM ACCESS MEMORY**

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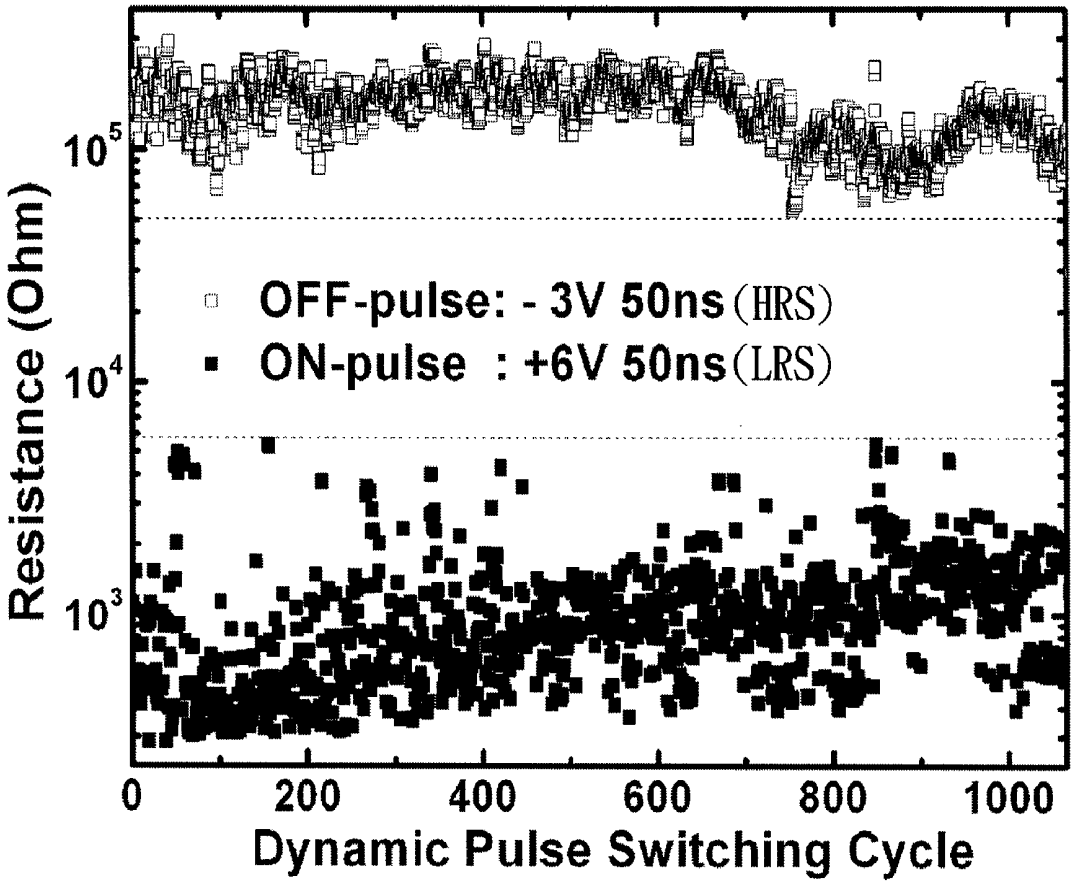
(57) **ABSTRACT**

A method for fabricating a resistor for a resistance random access memory (RRAM) includes: (a) forming a first electrode over a substrate; (b) forming a variable resistance layer of zirconium oxide on the first electrode under a working temperature, which ranges from 175° C. to 225° C.; and (c) forming a second electrode of Ti on the variable resistance layer.



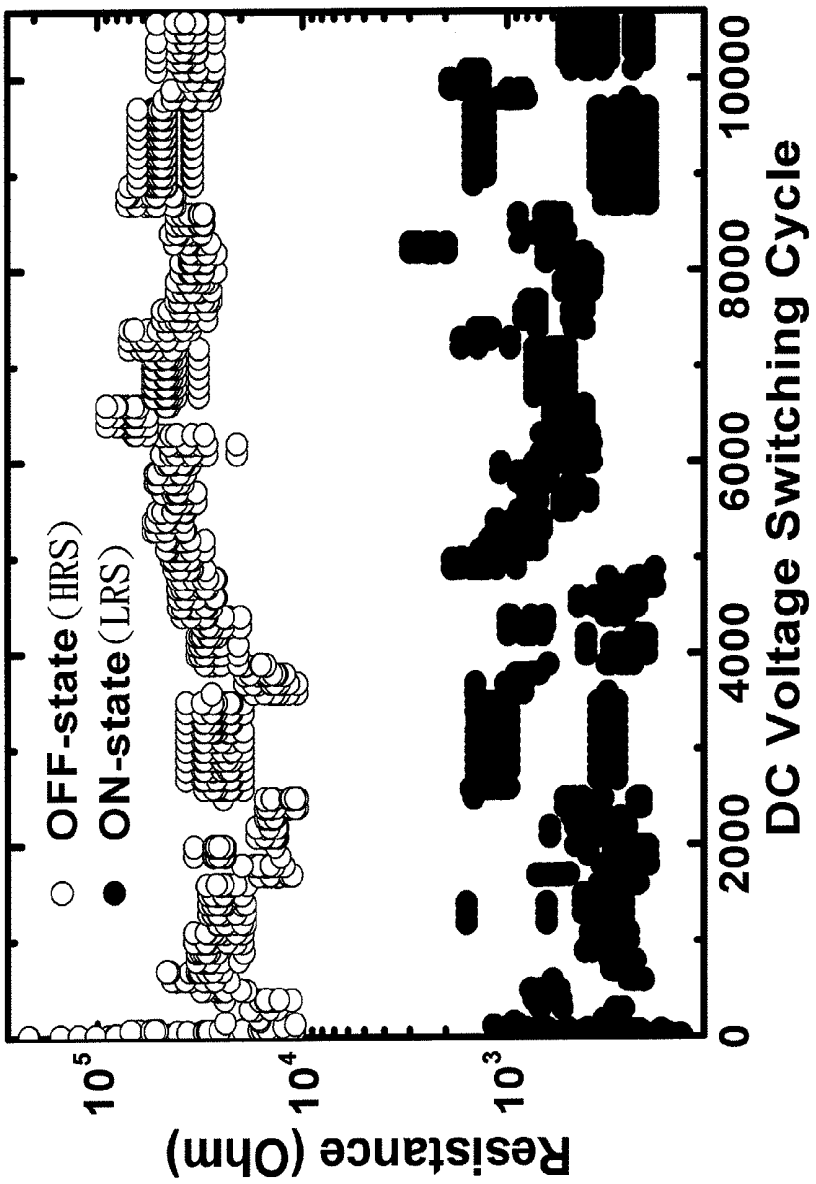

Resistance (Ohm)
10^5
10^4
10^3
0
2000
4000
6000
8000
10000
DC Voltage Switching Cycle
OFF-state (HRS)
ON-state (LRS)

FIG. 1

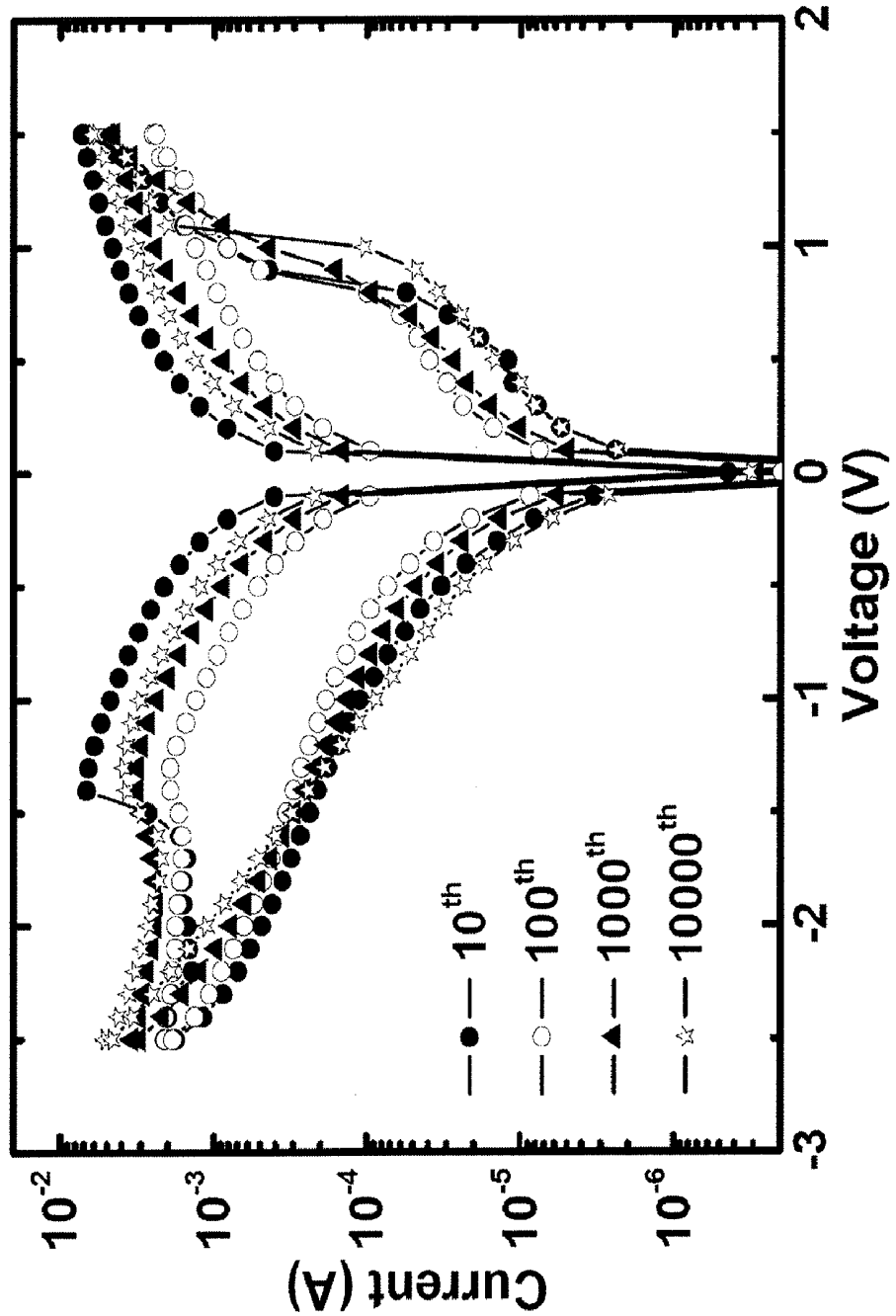

Current (A)
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
Voltage (V)
2
1
0
-1
-2
-3
10^{th}
100^{th}
1000^{th}
10000^{th}

FIG. 2

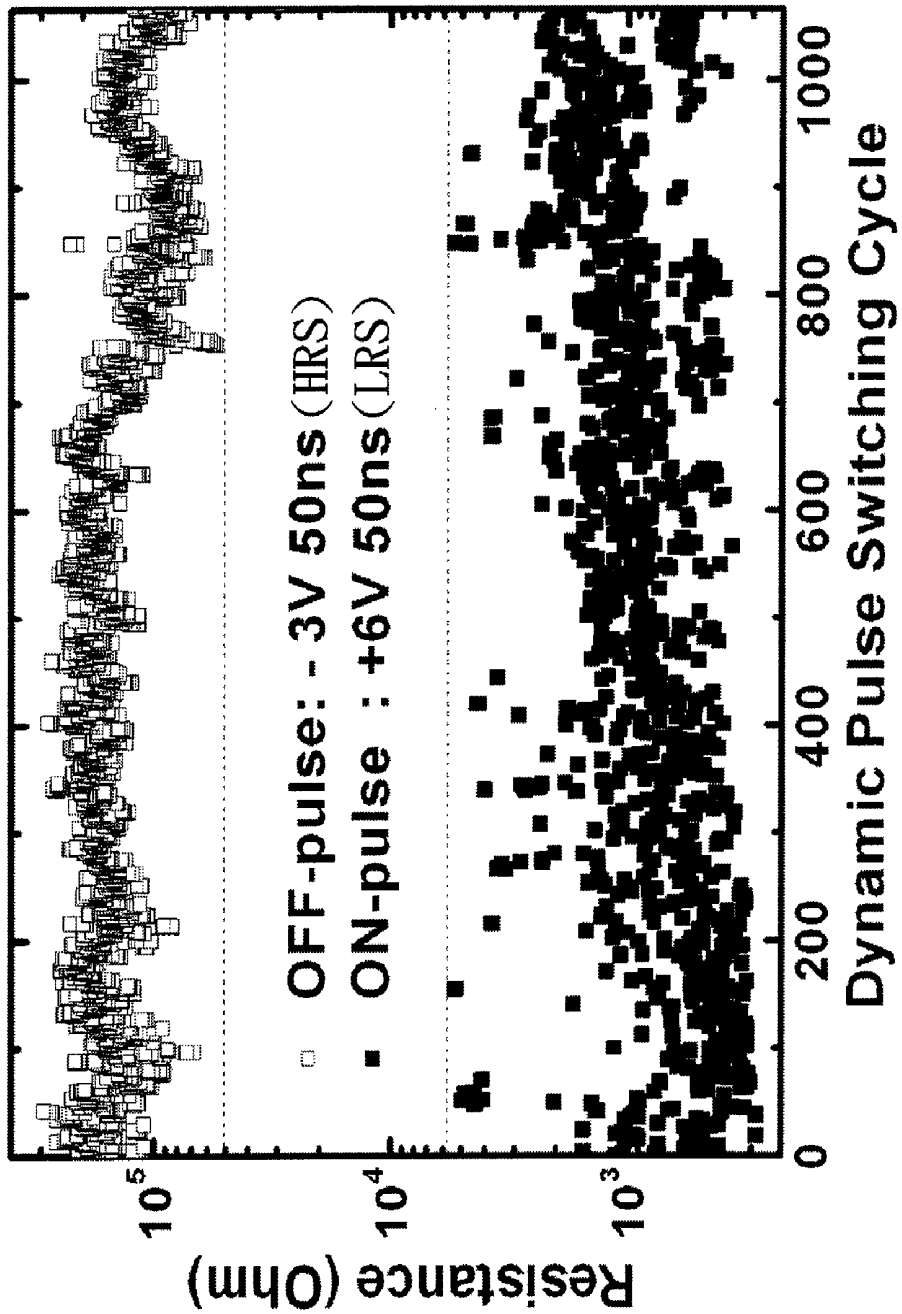

Resistance (Ohm)
10^5
10^4
10^3
0
200
400
600
800
1000
Dynamic Pulse Switching Cycle
OFF-pulse: - 3V 50ns (HRS)
ON-pulse : +6V 50ns (LRS)

FIG. 3

METHOD FOR FABRICATING A RESISTOR FOR A RESISTANCE RANDOM ACCESS MEMORY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority of Taiwanese application no. 099100900, filed on Jan. 14, 2010.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to a method for fabricating a resistor for a resistance random access memory (RRAM), more particularly to a method involving forming a variable resistance layer of zirconium oxide on an electrode under a working temperature ranging from 175° C. to 225° C.

[0004] 2. Description of the Related Art

[0005] Generally, a resistance random access memory (RRAM) circuit is composed of an array of 1T1R cross point memory cells (as described in U.S. Pat. No. 7,208,372), each of which has a transistor and a resistor, or composed of an array of 1D1R cross point memory cells, each of which has a diode and a resistor.

[0006] The resistor has a tri-layer structure including a top electrode, a bottom electrode, and an insulating layer sandwiched between the top and bottom electrodes. Transition metal oxides, such as NiO, CuO, ZrO_2, TiO_2 and HfO_2, with a variable resistance are widely used as the insulating layer. The aforesaid transition metal oxides exhibit a property that the resistance thereof can be switched between a high resistance state (which can be referred as OFF-state) and a low resistance state (which can be referred as ON-state) by applying a set (a write action) or a reset (an erasing action) voltage to the resistor. Several mechanisms of resistive switching between ON-state and OFF-state for the resistors have been proposed over the years (as described in U.S. Patent Application Publication No. 2007/0269683). The high and low resistance states of the insulating layer within the resistor can be used to define as a two-state information (0, 1) stored in the RRAM circuit, and can be read by applying a reading voltage to the resistor.

[0007] A conventional method for fabricating a resistor for a resistance random access memory (RRAM) (see IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 5, PP. 366~368, MAY 2007 by the inventors of the present application) includes the following steps: (A) forming a SiO_2 layer on a Si substrate; (B) forming a bottom electrode of a layer structure of Pt/Ti on the SiO_2 layer; (C) forming a ZrO_2 insulator layer having a layer thickness of 70 nm on the bottom electrode under a working temperature of 250° C. by using a radio-frequency magnetron sputtering system (not shown); and (D) forming a Ti layer, which serves as a top electrode on the ZrO_2 insulator layer, by using the radio-frequency magnetron sputtering system.

[0008] Since the formation of the resistors comes after the formation of the transistors (or the diodes) during a process of fabricating the resistance random access memory (RRAM) circuit, the working temperature (250° C.) when forming the ZrO_2 insulator layer is too high for the fabricated transistors (or the diodes), and would cause defects in the transistors (or the diodes). Furthermore, the life cycle of the resistor is also needed to be enhanced, i.e., more in number of resistive switching times between ON-state and OFF-state that the resistor can endure.

SUMMARY OF THE INVENTION

[0009] Therefore, the object of the present invention is to provide a method for fabricating a resistor for a resistance random access memory (RRAM) that can overcome the aforesaid drawbacks of the previous art.

[0010] According to this invention, it is provided a method for fabricating a resistor for a resistance random access memory (RRAM) that comprises: (a) forming a first electrode over a substrate; (b) forming a variable resistance layer of zirconium oxide on the first electrode under a working temperature, which ranges from 175° C. to 225° C.; and (c) forming a second electrode of Ti on the variable resistance layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Other features and advantages of the present invention will become apparent in the following detailed description of the preferred embodiment of this invention, with reference to the accompanying drawings, in which:

[0012] FIG. **1** is a plot of resistance vs. DC voltage switching cycle to illustrate the endurance test for a resistor of Example 2 (E2);

[0013] FIG. **2** is a plot of current vs. voltage to illustrate the stability of the DC voltage switching cycle for the resistor of Example 2 (E2); and

[0014] FIG. **3** is a plot of resistance vs. dynamic pulse switching cycle to illustrate the write/erase cycling test for the resistor of Example 2 (E2).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0015] The preferred embodiment of a method for fabricating a resistor for a resistance random access memory (RRAM) according to the present invention includes: (a) forming a first electrode over a substrate; (b) forming a variable resistance layer of zirconium oxide on the first electrode under a working temperature, which ranges from 175° C. to 225° C.; and (c) forming a second electrode of Ti on the variable resistance layer.

[0016] Preferably, formation of the variable resistance layer in step (b) is performed by sputtering techniques, and formation of the first and second electrodes in step (a) and (c) is conducted through evaporation techniques.

[0017] Preferably, the first electrode has a Ti adhesion layer deposited on the substrate and a Pt electrode layer deposited on the Ti layer.

[0018] The following examples and comparative examples are provided to illustrate the merits of the preferred embodiment of the invention, and should not be construed as limiting the scope of the invention.

Example 1

E1

[0019] The resistor of Example 1 (E1) was prepared by the following steps.

[0020] A Si substrate was subjected to wet oxidation so as to form a 200-nm-thick SiO_2 layer. Then, the SiO_2 layer formed on the Si substrate was put into an electron beam evaporation system with a working pressure of 2×10^{-6} Torr for depositing a bottom electrode which includes a 20-nm-thick Ti adhesion layer on the SiO_2 layer and an 80-nm-thick Pt electrode layer on the Ti layer. The assembly was subsequently placed into a radio-frequency (r.f.) magnetron sput-

tering system with a working pressure of 10 mTorr for depositing a variable resistance layer of 40-nm-thick ZrO_2 layer at a working temperature of 175° C. by applying an output power of 150 W to a ZrO_2 target in the sputtering system. A mixture of O_2 and Ar in a ratio of 6 to 12 was introduced into the sputtering system during the deposition of the variable resistance layer. Finally, the assembly was placed into the evaporation system for depositing a top electrode of Ti layer with a thickness of 150 nm thereon.

Example 2

E2

[0021] The resistor of Example 2 (E2) was prepared by steps and process conditions similar to those of Example 1 (E1), except that the working temperature was 200° C.

Example 3

E3

[0022] The resistor of Example 3 (E3) was prepared by steps and process conditions similar to those of Example 1 (E1), except that the working temperature was 225° C.

Comparative Example 1

CE1

[0023] The resistor of Comparative Example 1 (CE1) was prepared by steps and process conditions similar to those of Example 1 (E1), except that the working temperature was 150° C.

Comparative Example 2

CE2

[0024] The resistor of Comparative Example 2 (CE2) was prepared by steps and process conditions similar to those of Example 1 (E1), except that the working temperature was 250° C.

<Electrical Analysis>

[0025] An endurance test for Example 2 (E2) was conducted by cyclically applying a DC voltage sweep to the top electrode (Ti electrode) of Example 2 (E2) using a data acquisition instrument (instrument trade name: Agilent 4155C). The sweeping direction is from 0V to +1.5 V, back to 0 V, then to −2.5 V, and back to 0 V with a sweeping voltage step of 0.1 V. During the voltage sweeping cycle, +1.5 V is an applied positive voltage span to permit the variable resistance layer of ZrO_2 to be set to ON-state (LRS), and −2.5 V is an applied negative voltage span to permit the variable resistance layer of ZrO_2 to be set to OFF-state (HRS). As for the endurance test of Example 2 (E2), both the ON-state and OFF-state resistance values of each cycle were measured and recorded by a reading voltage of 0.3 V. Referring to FIG. **1**, the resistor of Example 2 (E2) can be continuously switched between ON-state and OFF-state for over 10^4 times during the DC voltage sweeping spans. In addition, the resistor of Example 1 (E1) and Example 3 (E3) can be continuously switched between ON-state and OFF-state for about 6800 times and 7300 times (see Table 1), respectively, during the same DC voltage sweeping spans. However, the resistor of Comparative Examples (CE1~CE2) only can be continuously switched between ON-state and OFF-state for about 4000 times and 6100 times, respectively, during the same DC voltage sweeping spans.

TABLE 1

Examples	Working temperature (° C.)	Endurance test (times)
CE1	150	4000
E1	175	6800
E2	200	10599
E3	225	7300
CE2	250	6100

[0026] FIG. **2** shows the measured current-voltage (I-V) curves of the test sample of Example 2 (E2), which depicts the 10^{th} time 100^{th} time, 1000^{th} time, and 10000^{th} time resistive switching cycles, respectively. The I-V curves shown in FIG. **2** are close to each other, indicating that the resistor of Example 2 (E2) exhibit a stable electrical property.

[0027] FIG. **3** shows the write/erase cycling test for Example 2 (E2). The write/erase cycling test of Example 2 (E2) was measured by alternately applying a switch-on voltage pulse of +6 V with a pulse-width of 50 ns and a switch-off voltage pulse of −3 V with a pulse width of 50 ns using a power supply (instrument trade name: Agilent 81110A). The resistance of the test sample was measured using the data acquisition instrument (Agilent 4155C), which was set to apply a reading voltage of 0.3 V to the test sample. The results shown in FIG. **3** indicate that the resistor of Example 2 (E2) can be rapidly switched in 50 ns from the write action to the erase action or from the erase action to the write action for over 1000 times.

[0028] In conclusion, by fabricating the variable resistance layer of zirconium oxide sandwiched between the bottom electrode of Pt and the top electrode of Ti under a working temperature ranging from 175° C. to 225° C., not only the endurance number of the switching times between ON-state and OFF-state of the resistor for RRAM application is increased, but also the aforesaid drawback of causing defects in the transistors (or the diodes) as encountered in the previous art is eliminated.

[0029] While the present invention has been described in connection with what is considered the most practical and preferred embodiment, it is understood that this invention is not limited to the disclosed embodiment but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation and equivalent arrangements.

What is claimed is:

1. A method for fabricating a resistor for a resistance random access memory (RRAM), comprising:

(a) forming a first electrode over a substrate;

(b) forming a variable resistance layer of zirconium oxide on the first electrode under a working temperature ranging from 175° C. to 225° C.; and

(c) forming a second electrode of Ti on the variable resistance layer.

2. The method of claim **1**, wherein formation of the variable resistance layer in step (b) is performed by sputtering techniques.

3. The method of claim **1**, wherein formation of the first electrode in step (a) and the second electrode in step (c) is conducted through evaporation techniques.

4. The method of claim **1**, wherein the first electrode includes a Ti adhesion layer deposited on the substrate and a Pt electrode layer deposited on the Ti layer.

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