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(54) **DUAL-THRESHOLD-VOLTAGE TWO-PORT SUB-THRESHOLD SRAM CELL APPARATUS**

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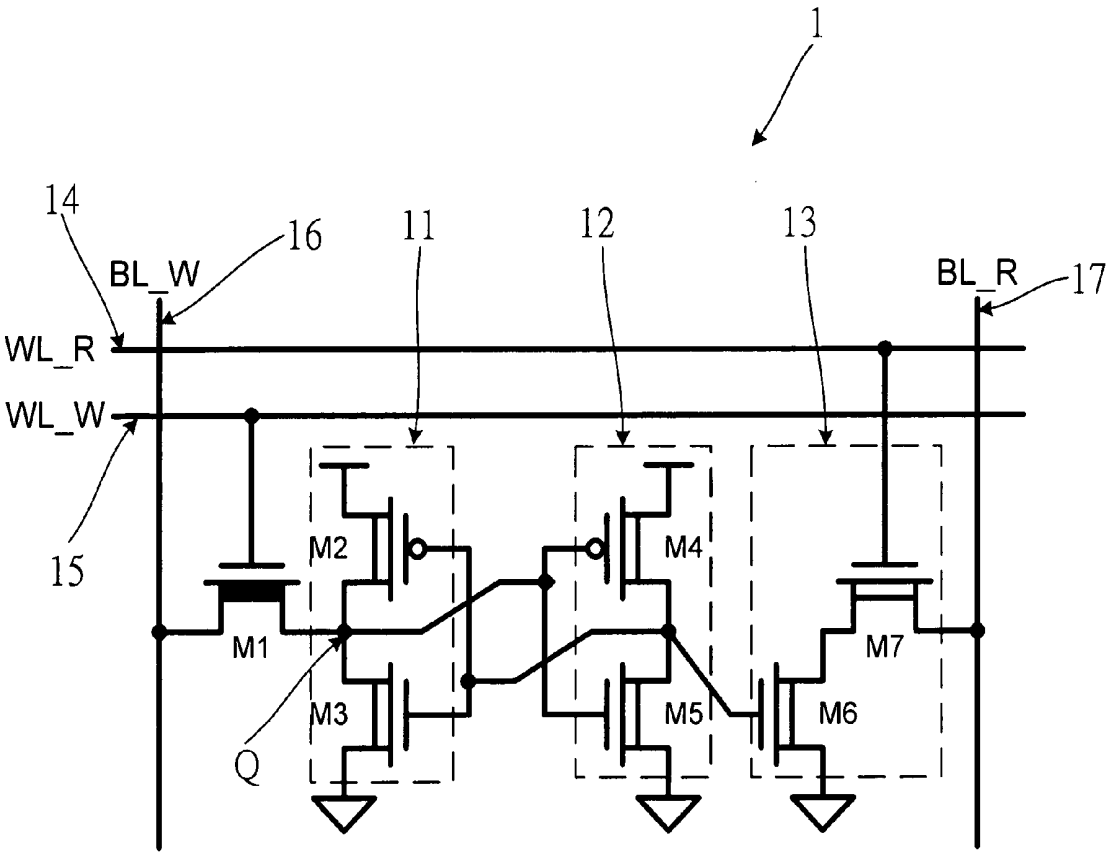
(57) **ABSTRACT**

The invention relates to a dual-threshold-voltage two-port sub-threshold SRAM cell apparatus. The above-mentioned apparatus comprises a first inverter, a second inverter, an access transistor and a read buffer. The first inverter and the second inverter include a plurality of first operating elements and a plurality of second operating elements for storing data. The access transistor is coupled to the first inverter and the second inverter, wherein the first operating elements and the second operating elements are high threshold voltage operating elements and the access transistor is low threshold voltage operating transistor. The read buffer is used for performing a read operation.



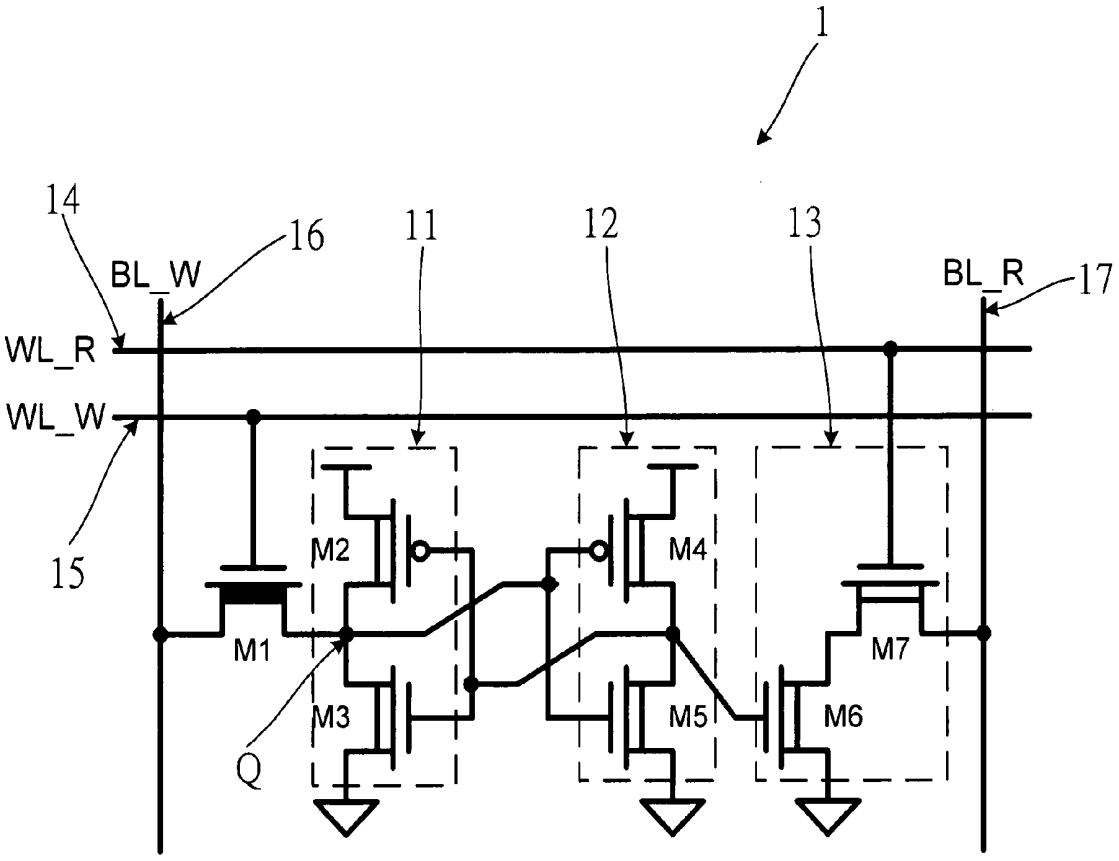


Figure 1

DUAL-THRESHOLD-VOLTAGE TWO-PORT SUB-THRESHOLD SRAM CELL APPARATUS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a SRAM cell apparatus, particularly to a dual-threshold-voltage two-port sub-threshold SRAM cell apparatus.

[0003] 2. Description of the Prior Art

[0004] The Static Random Access Memory (SRAM) is a kind of Random Access Memory (RAM). It means if the electric power is kept in the SRAM, the data will be able to be stored in it constantly. On the contrary, the data stored in the Dynamic Random Access Memory (DRAM) has to be upgraded periodically, and when the power supply is cut off, the stored data will be disappeared, which is completely different from the Read-Only Memory (ROM) or flash memory.

[0005] Thus, in the semiconductor memory devices, compared with the above-mentioned DRAM, the SRAM can provide the advantage of lower power consumption, and faster operation speed. Therefore, the SRAM can be widely used as the flash memory in the computer or in the other portable devices.

[0006] In the prior art, generally the SRAM often contains a wordline driver for receiving a word selection signal from an encoder. The wordline driver usually contains the inverters which are composed of the elements with smaller channel length and wider width. These inverters are used to adjust the voltage level on the wordline upon write program and read data. The inverter usually contains a pair of P-type Metal Oxide Semiconductor (PMOS) transistor and N-type Metal Oxide Semiconductor (NMOS) transistor. These two transistors are connected by a complementary power supply in serial, in order to generate a reverse signal corresponding to an input signal. The above-mentioned SRAM is widely applied in various single chip systems at present.

[0007] Although single chip systems can be used in many specific fields, such as the biomedical and electronic fields etc., but the single chip system stress has to have the characteristics of high reliability, low-voltage operation, low power consumption, and good stability etc. Thus, the design of SRAM is still unable to meet the above-mentioned requirements in the industry at present.

[0008] Therefore, in order to respond the technology demand for the production of SRAM, it is necessary to develop relevant process and technology to reduce the cost of operation manpower and manufacturing time, and reach the goal of energy conservation and carbon reduction effectively.

SUMMARY OF THE INVENTION

[0009] The invention provides a dual-threshold-voltage two-port sub-threshold SRAM cell apparatus to improve the drawback of the existing technology.

[0010] The invention relates to a dual-threshold-voltage two-port sub-threshold SRAM cell apparatus, the dual-threshold-voltage two-port sub-threshold SRAM cell apparatus comprises a first inverter, a second inverter, an access transistor and a read buffer. It can be operated at low voltage near threshold voltage. The first inverter includes a plurality of first operating elements. The second inverter is coupled to the first inverter and includes a plurality of second operating elements. The access transistor is coupled to the first inverter and the second inverter, wherein the first operating elements and the second operating elements have the first threshold voltage, and the access transistor has the second threshold voltage. The first threshold voltage is higher than the second threshold voltage. In addition, the first operating elements and the second operating elements are high threshold voltage operating elements and the access transistor is low threshold voltage operating transistor.

[0011] The dual-threshold-voltage two-port sub-threshold SRAM cell apparatus provided by the invention is suitably to be applied at the sub-threshold voltage. Even the stability of memory cell is decreased at lower voltage, the dual-threshold-voltage and two-port sub-threshold SRAM cell apparatus provided by the invention still can be operated stably at the sub-threshold voltage.

[0012] In addition, the invention utilizes the Dual-Vt scheme to reach the higher stability. The invention adopts the High-Vt device to hold stability and reduce the leakage current for the inverter used to store the data. Meantime, due to the de-couple of the data storage node and the bitline, the read stability will be increased significantly.

[0013] The invention adopts the Low-Vt device at the write-port to increase the write ability. Thus the structure of the invention is single-end read and single-end write, which can reduce the power consumption caused by the excess bitline. As for the design of the write-port, the read buffer is used to isolate the write bitline and the data storage inverter, in order to increase the read stability of the data.

[0014] Therefore, the advantage and spirit of the invention can be understood further by the following detail description of invention and attached Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0016] FIG. **1** is a graph illustrating the circuit of the dual-threshold-voltage two-port sub-threshold SRAM cell apparatus according to an embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] FIG. **1** is a graph for illustrating the circuit of the dual-threshold-voltage two-port sub-threshold SRAM cell apparatus according to an embodiment of the invention. The dual-threshold-voltage two-port sub-threshold SRAM cell apparatus **1** provided by the embodiment includes a first inverter **11**, a second inverter **12**, a read buffer **13**, an access transistor M**1**, a read wordline **14**, a write wordline **15**, a write bitline **16**, and a read bitline **17**.

[0018] The dual-threshold-voltage two-port sub-threshold SRAM cell apparatus **1** provided by the embodiment adopts single-end read and single-end write structure to reduce the number of bitline, so as to reduce the power consumption caused by the excess bitline.

[0019] The above-mentioned first inverter **11** includes a plurality of the first operating elements M**2** and the first operating elements M**3**. The second inverter **12** includes a plurality of second operating elements M**4** and second operating elements M**5**. The read buffer **13** includes the third operating element M**7** and the fourth operating element M**6**.

[0020] In the embodiment, the output end of the first inverter **11** is coupled to the input end of the second inverter **12**, and the output end of the second inverter **12** is coupled to the input end of the first inverter **11**, in order to form a latch for storing data.

[0021] The above-mentioned first operating element M**2** of the first inverter **11** and the second operating element M**4** of the second inverter **12** are the pull-up elements. The first operating element M**3** of the first inverter **11** and the second operating element M**5** of the second inverter **12** are the pull-down elements. In the embodiment, the pull-up elements of the first operating element M**2** and the second operating element M**4** are PMOS transistors. The pull-down elements of the first operating element M**3** and the second operating element M**5** are NMOS transistors. One end of the first operating element M**2** and the second operating element M**4** are coupled to a Vdd power supply, respectively. One end of the first operating element M**3** and the second operating element M**5** are coupled to a Vcc power supply, respectively.

[0022] The above-mentioned access transistor M**1** is coupled to the first inverter **11**, the second inverter **12**, the write wordline **15** and the write bitline **16**. In the embodiment, the operation of access transistor M**1** is controlled by the signal of write wordline **15**. In the embodiment, the access transistor M**1** is an NMOS. It has to mention that the first operating elements M**2**, the first operating elements M**3** and the second operating elements M**4**, the second operating elements M**5** have the first threshold voltage, and the access transistor M**1** has the second threshold voltage. The first threshold voltage is higher than the second threshold voltage. It means the first operating elements M**2**, the first operating elements M**3** and the second operating elements M**4**, the second operating elements M**5** are the high threshold voltage operating elements and the access transistor M**1** is low threshold voltage operating transistor.

[0023] In the embodiment, under the data holding state, the first operating elements M**2**, the first operating elements M**3** and the second operating elements M**4**, the second operating elements M**5** are used for data storage inverter to increase the data hold stability and reduce the leakage current. The stored data will not be changed due to noise, thus the stability of data is increased. In the embodiment, under the write state, the application of

[0024] Low-Vt device on the access transistor M**1** can increase the write ability, namely can mitigate the data write problem caused by the partial voltage effect (partial voltage between the access transistor M**1** and the second operating element M**3**), so as to increase the write ability. Thus the access transistor M**1** has low threshold voltage to help the write state.

[0025] The read buffer **13** is used to execute a read operation. The read buffer **13** is coupled to the first inverter **11**, the second inverter **12**, the read wordline **14** and the read bitline **17**. In addition, the third operating element M**7** is coupled to the fourth operating element M**6**, the read wordline **14** and the read bitline **17**. The fourth operating element M**6** is coupled to the third operating element M**7** and the second inverter **12**. In the embodiment, the operation of read buffer **13** is controlled by the signal of read wordline **14**, thus it can be operated at low voltage near the threshold voltage. The read buffer can isolate the latch and the read bitline, in order to prevent the noise of read bitline entering the latch, so as to increase the stability of the latch upon readind.

[0026] In the embodiment, the third operating element M**7** and the fourth operating element M**6** are the NMOS transistors. The third operating element M**7** and the fourth operating element M**6** have the third threshold voltage, and the third threshold voltage is higher than the second threshold voltage. In the embodiment, it means the third operating element M**7** and the fourth operating element M**6** are high threshold voltage operating elements. Thus M**2** to M**7** have high threshold voltage, which can be used to reduce power consumption and leakage current.

[0027] The dual-threshold-voltage two-port sub-threshold SRAM cell apparatus **1** provided by the embodiment utilizes the Dual-Vt element, de-couple of data storage node Q and bitline to reach the higher stability of the read and the write. Under de-couple of data storage node and bitline, the data storage node Q is not disturbed by the signal of bitline, so as to increase the anti-noise ability upon the read state.

[0028] Summarized from the above description, the dual-threshold-voltage and two-port sub-threshold SRAM cell apparatus provided by the invention is suitably to be applied at the sub-threshold voltage. Even the stability of memory cell is decreased at lower voltage, the dual-threshold-voltage and two-port sub-threshold SRAM cell apparatus provided by the invention still can be operated stably at the sub-threshold voltage. The structure of the invention is single-end read and single-end write can reduce the power consumption caused by long bitline, thus it is very suitable for the design of long term activation FIFO memory.

[0029] It is understood that various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be construed as encompassing all the features of patentable novelty that reside in the present invention, including all features that would be treated as equivalents thereof by those skilled in the art to which this invention pertains

What is claimed is:

1. A dual-threshold-voltage two-port sub-threshold SRAM cell apparatus, comprising:

a first inverter having a plurality of first operating elements;

a second inverter coupled to the first inverter having a plurality of second operating elements;

an access transistor coupled to the first inverter and the second inverter; and

a read buffer coupled to the first inverter and the second inverter, wherein the first operating elements and the second operating elements having the first threshold voltage, and the access transistor having the second threshold voltage, and the first threshold voltage is higher than the second threshold voltage.

2. The apparatus according to claim **1**, further comprises a read wordline, a write wordline, a write bitline and a read bitline, and the access transistor being coupled to the write wordline and the write bitline.

3. The apparatus according to claim **1**, further comprises a read wordline, a write wordline, a write bitline and a read bitline, and read buffer being coupled to the read wordline and the read bitline.

4. The apparatus according to claim **1**, wherein the read buffer comprises a third operating element and a fourth oper-

ating element, wherein the third operating element being coupled to the read wordline and the read bitline, and the fourth operating element being coupled to the second inverter and the third operating element.

5. The apparatus according to claim **4**, wherein the third operating element and the fourth operating element both are the NMOS transistors.

6. The apparatus according to claim **4**, wherein the third operating element and the fourth operating element comprises the third threshold voltage, and the third threshold voltage being higher than the second threshold voltage.

7. The apparatus according to claim **4**, wherein the third operating element and the fourth operating element comprises high threshold voltage operating elements.

8. The apparatus according to claim **1**, wherein the first operating elements and the second operating elements are high threshold voltage operating elements, and the access transistor is low threshold voltage operating transistor.

9. The apparatus according to claim **1**, wherein the read buffer comprises performing a read operation.

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