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(54) **METHOD AND APPARATUS FOR CARRY ESTIMATION OF REDUCED-WIDTH MULTIPLIERS**

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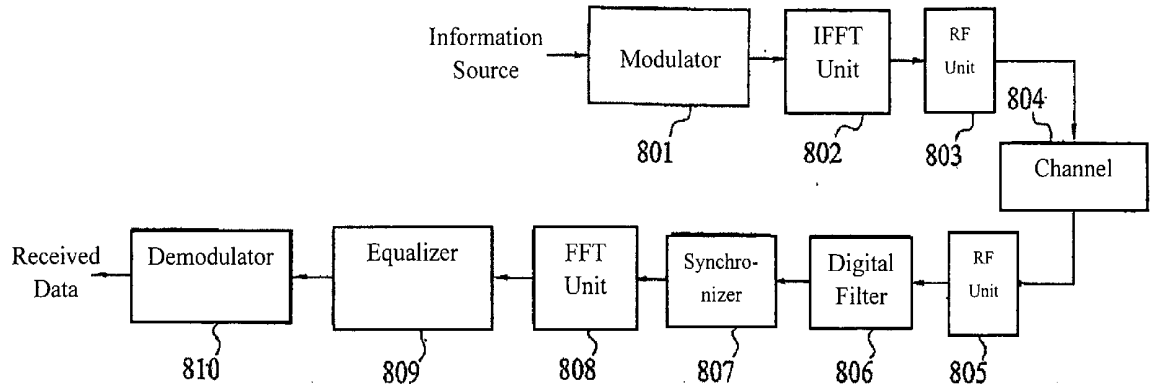
(57) **ABSTRACT**

A low-error reduced-width multiplier is provided by the present invention. The multiplier can dynamically compensate the truncation error. The compensation value is derived by the dependencies among the multiplier partial products, and thus, can be analyzed according to the multiplication type and the multiplier input statistics.



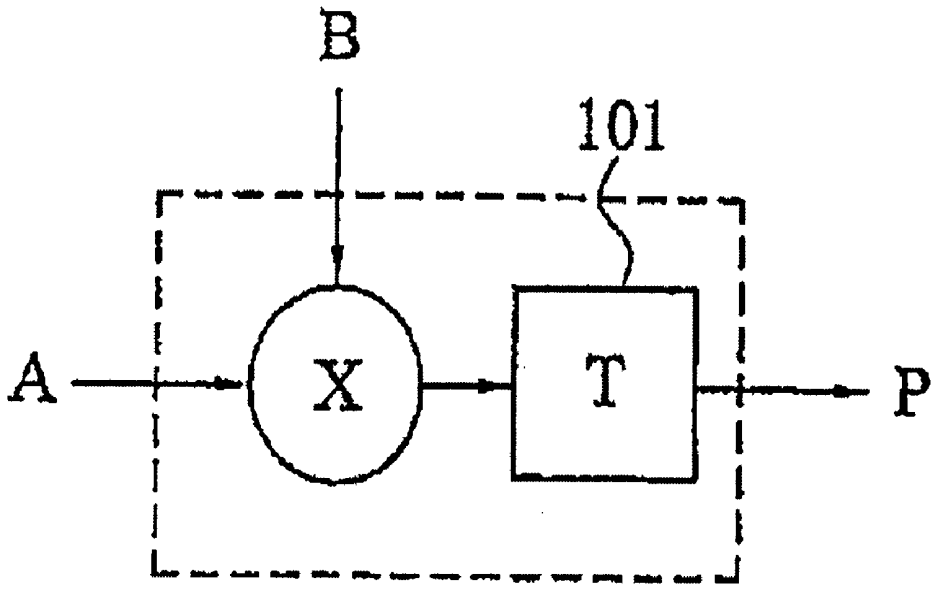


Figure 1.

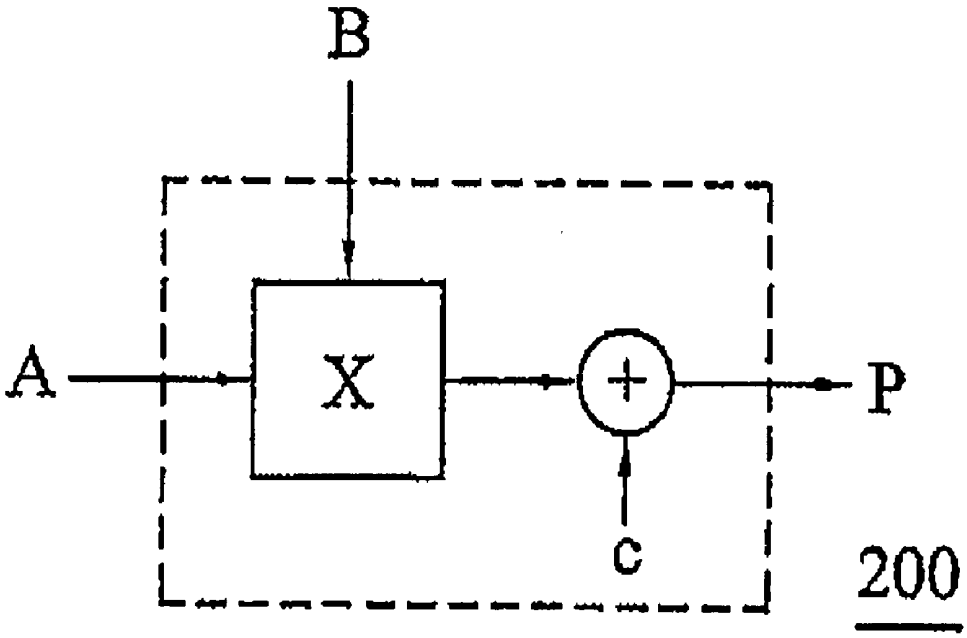


Figure 2.

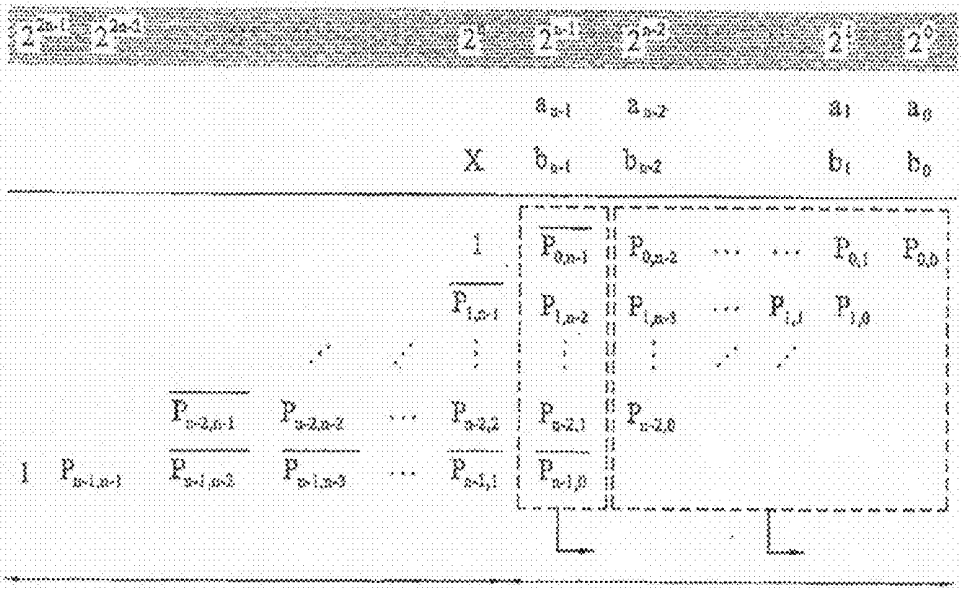


Figure 3.

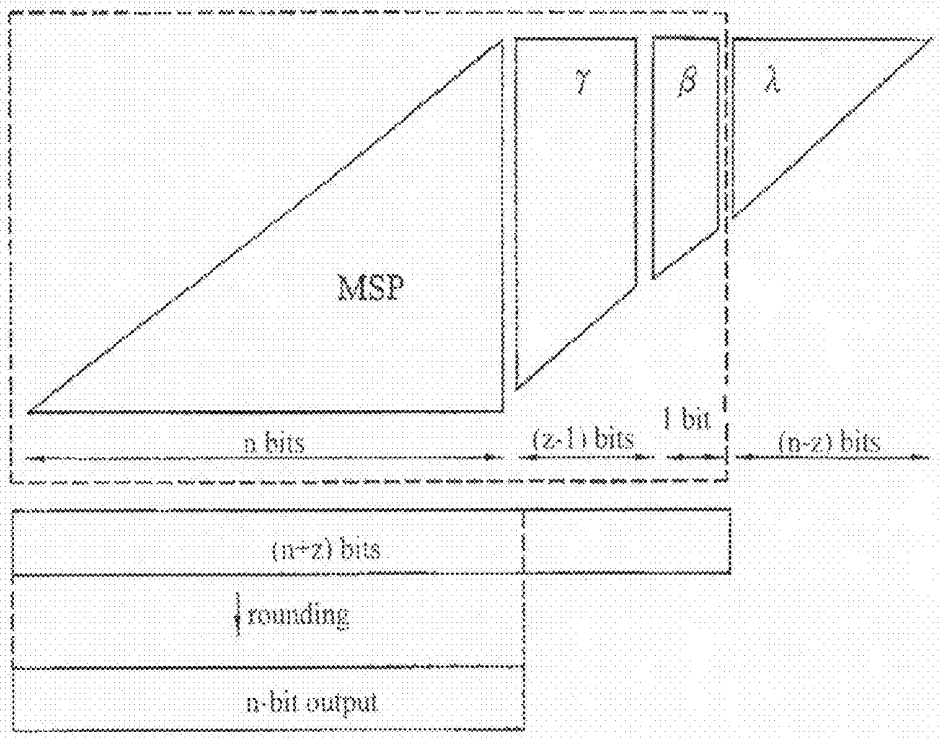


Figure 4

Type	Estimation of λ	Remark
First, a type	$2^{-z}\sum_{j=0}^{n-z-1} a_j$	$A=-a_{n-1}2^{n-1}+\sum_{j=0}^{n-2} a_j 2^j$
First, b type	$2^{-z}\sum_{l=0}^{n-z-1} b_l$	$B=-b_{n-1}2^{n-1}+\sum_{l=0}^{n-2} b_l 2^l$
Second, α type	$2^{-z}\sum_{j=0}^{n-z-1}\left(\frac{\alpha_j}{3}+\frac{1}{6}\right)\left(1-2^{-(n-z-j)}\right)$	$\beta=P_{0,n-z}+P_{n-z,0}+\sum_{l=1}^{n-z-1} P_{l,n-l-1}$
Second, β type	$2^{-z}\sum_{l=0}^{n-z-1}\left(\frac{\beta_l}{3}+\frac{1}{6}\right)\left(1-2^{-(n-z-j)}\right)$	$=P_{0,n-z}+P_{n-z,0}+\sum_{j=0}^{n-z-1} P_{n-j-z,j}$
		$\alpha_j=P_{n-j-z,j},\beta_l=P_{l,n-l-z}$

Figure 5.

Bit Width (n)	Z=1	Z=2	Z=3
8	$\lfloor\frac{1}{2}(\beta-\beta_{n-1}+1)\rfloor$	0, if $\beta-\beta_{n-z}=0$ $\lfloor\frac{1}{2}(\beta-\beta_{n-z}+1)\rfloor$; otherwise	$\lfloor\frac{1}{2}(\beta-\beta_{n-z})\rfloor$
10	0, if $\beta-\beta_{n-1}=0$ $\lfloor\frac{1}{2}(\beta-\beta_{n-1}+2)\rfloor$, otherwise	$\lfloor\frac{1}{2}(\beta-\beta_{n-z})\rfloor$ $+\mathrm{mod}(\beta-\beta_{n-z},2)$	1, if $\beta-\beta_{n-z}=1$ $\lfloor\frac{1}{2}(\beta-\beta_{n-z})\rfloor$, otherwise
12	$\lfloor\frac{1}{2}(\beta-\beta_{n-1}+2)\rfloor$	$\lfloor\frac{1}{2}(\beta-\beta_{n-z}+2)\rfloor$	$\lfloor\frac{1}{2}(\beta-\beta_{n-z})\rfloor$, if $\beta-\beta_{n-z}>3$ $\lfloor\frac{1}{2}(\beta-\beta_{n-z}+1)\rfloor$, otherwise
14	$\lfloor\frac{1}{2}(\beta-\beta_{n-1}+3)\rfloor$	$\lfloor\frac{1}{2}(\beta-\beta_{n-z}+2)\rfloor$, if $0\le\beta-\beta_{n-z}<4$; $\lfloor\frac{1}{2}(\beta-\beta_{n-z}+1)\rfloor$, if $4\le\beta-\beta_{n-z}<9$; $\lfloor\frac{1}{2}(\beta-\beta_{n-z})\rfloor$, otherwise	$\lfloor\frac{1}{2}(\beta-\beta_{n-z}+2)\rfloor$, if $0\le\beta-\beta_{n-z}<2$; $\lfloor\frac{1}{2}(\beta-\beta_{n-z}+1)\rfloor$, if $2\le\beta-\beta_{n-z}<7$; $\lfloor\frac{1}{2}(\beta-\beta_{n-z})\rfloor$, otherwise
16	$\lfloor\frac{1}{2}(\beta-\beta_{n-1}+3)\rfloor$	$\lfloor\frac{1}{2}(\beta-\beta_{n-z}+2)\rfloor$	$\lfloor\frac{1}{2}(\beta-\beta_{n-z}+2)\rfloor$

Figure 6.

Type	Estimation of λ
First Type	$2^{-(z+1)}\sum_{i=0}^{\lfloor n/2 \rfloor+\lfloor z/2 \rfloor} y_{i''}$, $y_{i''}=\begin{cases}1, & \text{if } En(b_{2i-1},b_{2i},b_{2i-1})\neq 0\\ 0, & \text{otherwise}\end{cases}$ In the above equation, En( ) denotes Booth Encoding.
Second Type	$2^{-z}\left(\frac{\beta}{10}+\frac{3}{20}\left\lceil\frac{n}{2}\right\rceil\right)$
Third Type	$2^{-z}\left(\frac{3}{8}\left\lceil\frac{n}{2}\right\rceil\right)$

Figure 7.

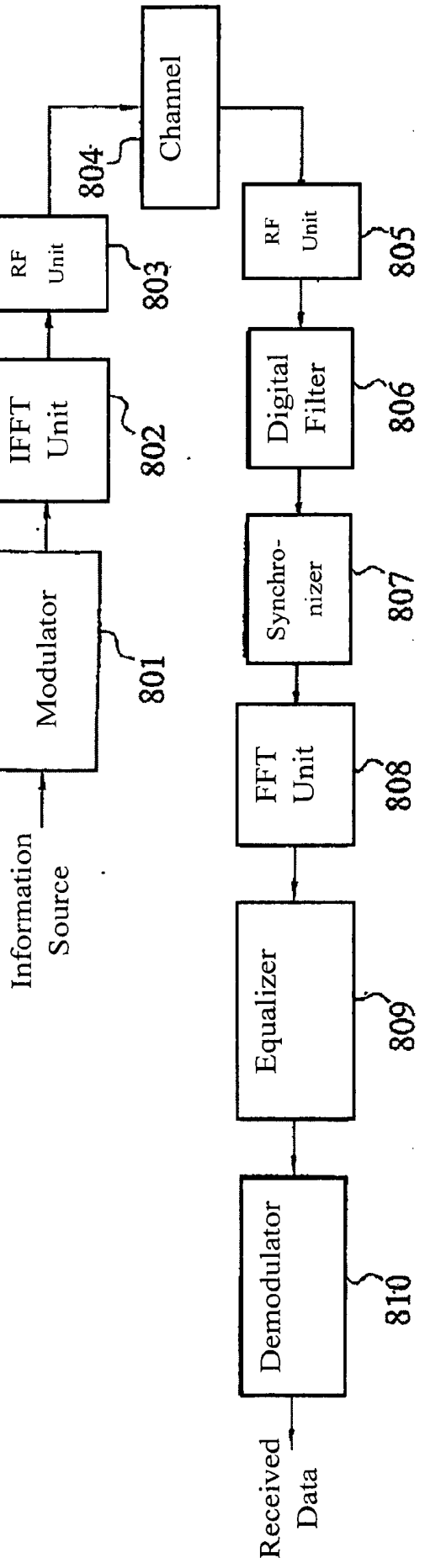

Information Source
Modulator
801
IFFT Unit
802
RF Unit
803
804
Channel
RF Unit
805
Digital Filter
806
Synchro-nizer
807
FFT Unit
808
Equalizer
809
Demodulator
810
Received Data

Figure 8.

METHOD AND APPARATUS FOR CARRY ESTIMATION OF REDUCED-WIDTH MULTIPLIERS

FIELD OF THE INVENTION

[0001] The present invention relates to a multiplier and its method of operation, and in particular relates to a low-error reduced-width multiplier and its method of operation.

BACKGROUND OF THE INVENTION AND PRIOR ART

[0002] Multiplier is one of the most common basic operations for digital signal processing. When performing a digital signal processing, in order to prevent data's bit width from overflow as the operation burden increases, therefore multiplication operation usually incorporates a reduced (or fixed) width characteristic so as to prevent the occurrence of the case of the numerical overflow during the process of the operation. Generally speaking, the reduced-width characteristic is commonly realized by employing a post-truncated multiplier, where the truncation operation is executed at the output of the multiplier in order to maintain the fixed width of bits. In contrast to the post-truncated multiplier, the direct-truncated multiplier only executes a partial product accumulation on the portions that are willing to preserve the output bit of the multiplication so as to reduce the computation complexity; but, however, usually it will result in a relatively large error.

[0003] For the direct-truncated fixed-width multiplier, the bit width of input/output is the same; and for the fixed-width multiplier, the error is compensated by adding a number. However, error compensation methods proposed in prior arts are only applicable for multipliers that utilize a single partial product generating approach, and most of them need to be accompanied with an acquisition of a large amount of simulation auxiliary compensated terms. Because of the lack of effective analysis method, it is difficult to further apply to the system-level analysis. Therefore, a direct-truncated multiplier of the known art only realizes the partial product accumulation corresponding to the remaining parts after truncation.

[0004] Figure depicts a circuit block diagram of a well-known multiplier, in which the bit width of an input data A is n_1, and the bit width of an input data B is n_2. The product of these two inputs has a bid width of (n_1+n_2) bits. This product must be truncated by the truncator (denoted by T) in order to keep the bit width at n (n ? n_1 n_2) bits and therefore to prevent overflow.

[0005] Although there are many kinds of method being proposed in the literature to compensate for this error, however, they all are applicable for those multipliers which utilize a certain partial product generating method. Hereafter a survey of patent literature and non-patent literature relevant to the present invention will be given and analyzed as follows:

[0006] 1. R.O.C. Patent No. 396321, Jul. 1, 2000, "Low-Error Fixed-Width **2**'s Complement Parallel Multiplier." This patent application only provided a compensation for a 2's complement fix-width multiplier, which may dynamically generate a quantity of compensation in accordance with the input value of the multiplier, but, however, due to the lack of theoretic analysis, it is not able to mitigate errors in accordance with the statistical characteristics of the input data, and furthermore it is not applicable for the multipliers that adopt different partial products generating methods.

[0007] 2. R.O.C. Patent No. 484092, Apr. 21, 2002, "A Reducible Bit Length Low-Error Multiplier." This patent application provided a dynamic compensation method for a 2's complement and modified Booth multipliers. The mechanism for generating an amount of compensation is simple, but is not able to efficiently compensate for errors.

[0008] 3. K. K. Parhi, J. G. Chung, K. C. Lee, and K. J. Cho, "Low-Error Fixed-Width Modified Booth Multiplier," Dec. 20, 2005, U.S. Pat. No. 0,069,78426B2. This patent application provided a dynamic compensation method for the modified Booth multiplier, which is able to effectively compensate for errors; but, however, the hardware complexity for generating a quantity of compensation may increase as the width of the input of the multiplier become larger.

[0009] 4. Y. C. Lim, "Single-Precision Multiplier with Reduced Circuit Complexity for Signal Processing Applications," *IEEE Trans. Computers*, Vol. 41, pp. 1333-1336, October 1992. This non-patent literature proposed generating a constant of compensation via a preliminary analysis, and also pointed out the concept of dynamic compensation, but, however, is lack of a detailed and concrete analysis and realization method.

[0010] 5. M. J. Schulte and E. S. Jr., "Truncated Multiplication with Correction Constant," in *Workshop on VLSI Signal Processing*, October 1993, pp. 388-396.

[0011] 6. S. S. Kidambi, F. El-Guibaly, and A. Antoniou, "Area-Efficient Multipliers for Digital Signal Processing Applications," *IEEE Trans. Circuits Syst. II, Vol.* 43, pp. 90-95, February 1996.

[0012] (A) The non-patent literature, item 5 and item 6 mentioned above, both proposed a constant compensation method, which is not able to effectively compensate for errors.

[0013] (B) The non-patent literature, item 4 to item 6 mentioned above, put a special emphasis on the constant compensation method, which, besides being not able to effectively compensate for errors, it is also difficult to change the way of analysis in accordance with different generating method for partial products.

[0014] 7. T. B. Juang and S. F. Hsiao, "Low-Error Carry-Free Fixed-Width Multipliers with Low-Cost Compensation Circuits," *IEEE Trans. Circuits Syst.* II, Vol. 52, No. 6, pp. 299-303, June 2005. This non-patent literature provided a dynamic compensation mechanism only for signed-magnitude modified Booth multiplier, and did not provide any other multiplication compensation method for different partial products generating methods.

[0015] 8. L. D. Van and C. C. Yang, "Generalized Low-Error Area-Efficient Fixed-Width Multipliers," *IEEE Trans. Circuits Syst.* I, Vol. 52, No. 8, pp. 1608-1619, August 2005. This non-patent literature can be treated as a derivative of the above-mentioned patent literature item 1, but these two methods were designed only for 2's complement fixed-width multipliers, and are not appropriate for other multipliers employing different partial products generating method.

SUMMARY OF THE INVENTION

[0016] One of the objectives of the present invention is to provide an operational method of a low-error reduced-width

multiplier for reducing computational complexity and compensating for truncation errors, which is applicable to different types of multipliers.

[0017] Another objective of the present invention is to provide a low-error reduced-width multiplier for reducing computational complexity and compensating for truncation errors.

[0018] To achieve the above-mentioned objectives, in accordance with a first aspect of the present invention, there is provided an operational method of a low-error reduced-width multiplier for reducing computational complexity and compensating for truncation errors, comprising the following steps: dynamically generating a compensation term by using an input value of a multiplier; and an accumulating operation for which the part that is set to be the truncated part in the multiplier is omitted, while the compensation term is used for compensation, in order to reduce the width.

[0019] Furthermore, to achieve the above-mentioned objectives, in accordance with a second aspect of the present invention, there is provided a low-error reduced-width multiplier, in which the multiplier can reduce the width by an accumulating operation for which the part that is set to be the truncated part in the multiplier is omitted, while the compensation term dynamically generated by an input value is used for compensation.

[0020] Therefore, because of the utilization of an accumulating operation that use a dynamically generated compensation term to compensate for the part that is set to be a truncated part, the present invention is able to reduce the computational complexity and compensate for truncation errors, and is also applicable to different types of multipliers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] For the purpose that the said and other objectives, characteristics, and advantages of the present invention can be clearly seen, and be easily and obviously understood, preferred embodiments of the present invention are subsequently described by referring to the enclosing drawings, wherein:

[0022] FIG. **1** depicts a circuit block diagram of a prior art multiplier.

[0023] FIG. **2** depicts a circuit block diagram for an n-bit low-complexity reduced-width multiplier **200** proposed in a preferred embodiment of the present invention.

[0024] FIG. **3** depicts a partial product generating diagram for an n-bit low-complexity reduced-width multiplier **200**.

[0025] FIG. **4** depicts another partial product generating diagram for an n-bit multiplier **200**.

[0026] FIG. **5** and FIG. **6** depict, respectively, three kinds of diagrams of compensation generating formulae for used in different bit-width 2's complement multipliers.

[0027] FIG. **7** depicts three kinds of diagrams of compensation generating formulae for different bit-width modified Booth multipliers.

[0028] FIG. **8** depicts a simplified circuit diagram for an orthogonal frequency division multiplexing (OFDM) system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0029] In the following, preferred embodiments of the present invention are subsequently described by referring to the enclosing drawings.

[0030] The present invention discloses a dynamic generation of compensation and estimation analysis method that is applicable to different bit-width and different parts of products generating procedure of a multiplier. By utilizing this analysis method, it is able to further provide a system level analysis so as to provide a design choice while considering the design cost such as complexity and compensation accuracy. In accordance with the present invention, to achieve low complexity, a direct-truncated multiplier together with a compensating circuit for dynamically generating a quantity of compensation are adopted, where the mechanism for dynamically generating compensation still fulfills the low-error and low-complexity requirements. In connection with those requirements, distribute the correlations among the elements of the products, and observe parts of the partial products to calculate and arrange the state expectation value of the partial products to serve as a quantity of compensation needed in the dynamic compensation. Therefore, the analysis method in accordance with the present invention has a low complexity, and is applicable to the multipliers employing different kinds of partial products generating methods. Hence, under the condition that the statistical characteristics of the input signals to the multiplier are known, it offers much more accurate compensation, and can further provide a system-level truncation error analysis.

[0031] The present invention can be used in LAN\WAN, DVB-T/H, xDSL and high-speed low-power signal processors (such as the kernel processor of fast Fourier transform (FFT) or digital filter, equalizer).

[0032] FIG. **2** depicts a circuit block diagram for an n-bit low-complexity reduced-width multiplier **200** proposed in a preferred embodiment of the present invention. As shown in FIG. **2**, a direct product of an A having n_1 bits and a B having n_2 bits results in a product of n bits; in the mean time, a compensation C is added to the product in order to correct the induced error while decreasing the complexity. The computational complexity and hardware cost of a low-complexity reduced-width multiplier **200** can be reduced by omitting the partial products accumulation corresponding to the last part of the bits. FIG. **3** depicts a partial product generating diagram for an n-bit low-complexity reduced-width multiplier **200**. Taking the product of A×B as an example, if

$$A = -a_{n-1}2^{n-1} + \sum_{j=0}^{n-2} a_j 2^j,$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i,$$

and $P_{ij}=a_jb_i$. Then the result of the multiplication can be represented as the following equation:

$$A \times B = MSP + 2^{n}\left(\left[\frac{\beta}{2} + \lambda\right]_r\right) \approx MSP + 2^{n}\left(\left[\frac{1}{2}(2\beta + 2\lambda - 1)\right]_r\right)$$

where $[\ ]_r$ denotes round-off.

[0033] The multiplier **200** provided by the present invention is able to reduce the complexity by omitting the partial products accumulating operation of λ, while adding an estimation of λ to compensate for the error induced by this simplification. Because any two elements $P_{i\ j}^{\ 1}$, $a_jb_i^{\ 1}$, $P_{ij}=a_jb_i$ that construct the partial product are both related to a_j, and

$P_{ij}^{1}=a_j^{1}b_i^{1}$, $P_{ij}=a_jb_i$ are related to b_i, therefore, by observing the partial product accumulation value of the nth bit

$$\left(B = P_{0,n-1} + P_{n-1,0} + \sum_{i=1}^{n-2} P_{i,n-i-1} = P_{0,n-1} + P_{n-1,0} + \sum_{i=1}^{n-2} P_{n-j-1,j}\right),$$

and by substituting P_{ij}, which constitute λ, with $E[P_{ij}|P_{i,n-i-1}]$, or by substituting P_{ij}, which constitute λ, with $E[P_{ij}|P_{n-j-1,j}]$, it is possible to estimate the value of λ that has been omitted to further compensate for this error. The quantity of compensation provided by the present invention is obtained by observing β, which corresponds to a quantity of compensation that changes dynamically in accordance with the input to an multiplier.

[0034] The multiplier provided by the present invention is capable of changing its omitting ratio of the partial product in accordance with the requested amount of error and complexity requirement of its applications or systems. FIG. **4** depicts another partial product generating diagram for an n-bit multiplier **200**, where the number of percentage occupied by λ can be determined by the parameter z. The compensation estimation method proposed by the present invention can be used with different numbers of the parameter z. The present invention also takes the 2's complement multiplier and the modified Booth multiplier as illustrating examples and provides respectively three types of compensation estimation methods for each of the multipliers. FIG. **5** and FIG. **6** depict, respectively, three kinds of diagrams of compensation generating formulae for used in different bit-width 2's complement multipliers. FIG. **7** depicts three kinds of diagrams of compensation generating formulae for different bit-width modified Booth multipliers. The present invention further provides an analysis method for analyzing the compensation C in accordance with the statistical characteristics of the input signals A, B of the multiplier.

[0035] FIG. **8** depicts a simplified circuit diagram for an orthogonal frequency division multiplexing (OFDM) system, where the information source is inputting to the modulator **801**, passing through an IFFT (Inverse Fast Fourier Transform) unit **802**, transferring from RF (radio frequency) unit **803** through the channel **804** to RF unit **805**, and further inputting to FFT (Fast Fourier Transform) unit **808** through the digital filter **806** and the synchronizer **807**, and then generating received data by adjusting the signal frequency using the equalizer **809** and further processing by the demodulator **810**, in which a great amount of complex multipliers needed in the required correlation calculation of the synchronization of the timing sequence and the calculation and compensation of the frequency offset of the digital filter, equalizer, and synchronizer in the above-mentioned system can all be implemented by the low-complexity, low-error multipliers provided by the present invention.

[0036] To sum up, from the previous description, the low-error reduced-width multiplier and it operation method provided in the present invention, because of the utilization of an accumulating operation that use a dynamically generated compensation term to compensate for the part that is set to be a truncated part, is able to reduce the computational complexity and compensate for truncation errors, and therefore is also applicable to different types of multipliers having different bit widths and using different partial products generating methods.

[0037] Although the present invention is disclosed in a plurality of preferred embodiments described above, the inventive idea should not be limited only to those. It will be understood by those skilled in the art that various other changes in the form and details may be made without departing from the spirit and scope of the present invention. It is to be understood that various changes may be made in adapting to different embodiments without departing from the broader concepts disclosed herein and comprehended by the claims that follow.

1. A method for carry estimation, which is capable of reducing the computational complexity and compensating for truncation error, comprising the following steps:

dynamically generating a compensation term by using an input value of a multiplier; and an accumulating operation for which the part that is set to be the truncated part in the multiplier is omitted in order to reduce the width, while the compensation term is used for compensation.

2. A method for carry estimation in accordance with claim **1**, further comprising the following step:

generating the compensation term by analyzing the statistical characteristics of the input value of the multiplier, in which the statistical characteristics are obtained by the frequency offset and correlation calculation.

3. A method for carry estimation in accordance with claim **1**, further comprising the following step:

generating the compensation term by using the partial product that is obtained by analyzing the input value operation of the multiplier.

4. A method for carry estimation in accordance with claim **1**, wherein the multiplier is a 2's complement multiplier.

5. A method for carry estimation in accordance with claim **1**, wherein the multiplier is a modified Booth multiplier.

6. A method for carry estimation in accordance with claim **1**, wherein the estimation method is applicable for a complex multiplier, where the operation method is that an operation of a real part of the complex multiplier together with an operation of a imaginary part of the complex multiplier are compensated for by using the compensation term.

7. A carry estimation apparatus for complex multiplication, wherein, an estimation method in accordance with claim **1**, the operation of the compensation term can be combined with the real-part or imaginary-part multiplication of the complex multiplication.

8. An apparatus for carry estimation, which is applicable for the method for carry estimation in accordance with claim **1**, wherein the multiplier can reduce the width by an accumulating operation for which the part that is set to be the truncated part in the multiplier is omitted, while the compensation term dynamically generated by an input value is used for compensation.

9. A carry estimation apparatus and error compensation generation method for applying to an application comprising successive multiplications and additions, wherein the estimation method in accordance with claim **1** is used to generate compensation terms corresponding to the need of each of the respective multipliers, and the compensation terms are then combined to apply to a single addition operation.

10. A carry estimation apparatus for complex multiplication, wherein, an estimation method in accordance with claim **2**, the operation of the compensation term can be combined with the real-part or imaginary-part multiplication of the complex multiplication.

11. A carry estimation apparatus for complex multiplication, wherein, an estimation method in accordance with claim **3**, the operation of the compensation term can be combined with the real-part or imaginary-part multiplication of the complex multiplication.

12. A carry estimation apparatus and error compensation generation method for applying to an application comprising successive multiplications and additions, wherein the estimation method in accordance with claim **2** is used to generate compensation terms corresponding to the need of each of the respective multipliers, and the compensation terms are then combined to apply to a single addition operation.

13. A carry estimation apparatus and error compensation generation method for applying to an application comprising successive multiplications and additions, wherein the estimation method in accordance with claim **3** is used to generate compensation terms corresponding to the need of each of the respective multipliers, and the compensation terms are then combined to apply to a single addition operation.

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