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Influences of Ti, TiN, Ta and TaN layers on integration of low-*k* SiOC:H and Cu

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Abstract

The interactions between low-*k* material hydrogenated silicon oxycarbide (SiOC:H) and barrier layers, Ta, TaN, physical-vapor deposition (PVD) and chemical-vapor deposition (CVD) Ti and TiN, have been investigated. The results show these barriers except TaN can react with SiOC:H at evaluated temperature. Furthermore, significant interactions of carbon and oxygen due to the degradation of the SiOC:H films upon annealing exist for all barrier/SiOC:H structures. The CVD-TiN structure can retard the hydrogen out-diffusion, while PVD-TiN structure induces the H out-diffusion from the SiOC:H films. By studying flat band voltage shift in *C–V* tests, it is demonstrated that Cu^+ ions drift into SiOC:H under electric field at elevated temperatures. A thin layer of TaN is proven to be good Cu drift barrier layer with SiOC:H dielectrics.
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Keywords: Hydrogenated silicon oxycarbide; Ti; TiN; Ta; TaN; Cu^+ ions drift

1. Introduction

Copper (Cu) has attracted considerable attention as an interconnect material for deep sub-micron circuits because it has low resistivity and high electromigration and stress migration resistance that is superior to that of Al and its alloy-based interconnecting metal [1,2]. However, Cu diffusion into the dielectrics and subsequently into silicon regions underneath prevents the integration of Cu metallization into integrated circuits (ICs), because it can degrade the device [3,4]. Therefore, a barrier layer is essential to prevent Cu diffusion. A significant amount of research has been performed and various appropriate diffusion barriers have been proposed [5–8].

Meanwhile, SiO_2 must be replaced with materials with low dielectric constants ($k < 3.9$) as the intermetal dielectrics. Hydrogenated silicon oxycarbide (SiOC:H), formed by high density plasma chemical vapor deposition (HPDCVD), has become the leading candidate for replacing SiO_2, because of its low dielectric constant (<3) and excellent interlayer features when used in damascene interconnects. Its properties were studied in detail and are present elsewhere [9,10]. Some of the O atoms are replaced by CH_x groups, yielding the caged SiO_2 structure. The caged structures are interlinked to form a porous network during the inductively coupled plasma (ICP) process, and the dielectric constant of SiOC:H can decrease to approximately 2.9. HDPCVD dielectrics with excellent electric properties outperform those formed by other methods; our recent work described the formation of dielectrics [11,12].

Although several investigations of Ti and Ta barriers on SiO_2 and dielectrics have been published [13–15], interactions with low-*k* SiOC:H have been less well studied. Additionally, adding N elements in Ti and Ta metal can generate the nanocrystalline structures, TiN and TaN. Such a microstructure seems to be required to ensure excellent barrier performance because of the lack of extended defects, and the ability of grain boundaries to serve as short circuit diffusion paths [16]. However, the desorption of C, O, and H atoms in the SiOC:H layers adjacent to the diffusion barriers during annealing may influence the integrity of the films. This study thus aims to examine interactions with the SiOC:H and evaluate the effectiveness of such barriers between the SiOC:H and the diffusion barrier. Furthermore, electrical methods are generally more sensitive than structural methods in detecting failure of the different barrier. The emphasis of this work is on electrical characterization of metal-insulator-semiconductor (MIS) capacitors after bias-temperature stressing (BTS) for different stressing time, using

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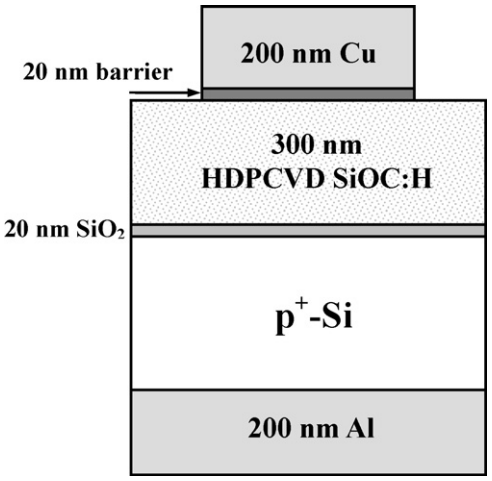

Fig. 1. The structure of the Cu/barrier/SiOC:H MIS capacitor.

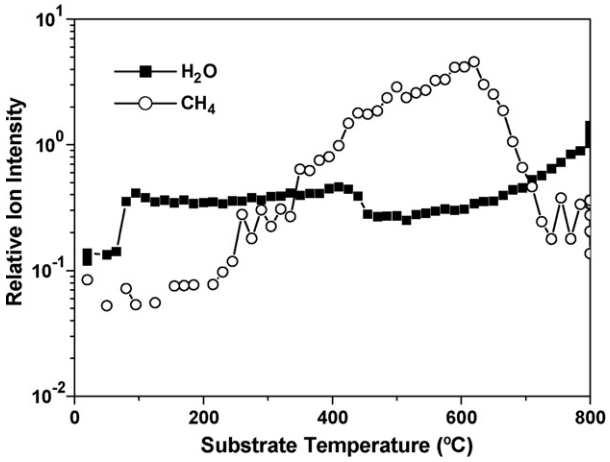

Fig. 2. TDS spectra of H_2O and CH_4 desorption as a function of temperature for the SiOC:H film.

current versus voltage (*I–V*) and capacitance versus voltage (*C–V*) measurements.

2. Experimental

Test capacitors with a MIS structure were fabricated on p^+-Si substrates with a 20 nm thick Ti, TiN, Ta or TaN barrier layer sandwiched between Cu and SiOC:H layers. Fig. 1 shows the schematic cross section of the MIS capacitor. A 20-nm-thick thermal SiO_2 layer was initially grown on Si to produce a high-quality dielectric-semiconductor interface. The SiOC:H film, 300 nm thick, was fabricated using a HDPCVD system, with trimethysilane [$Si(CH_3)_3H$,3MS] and nitrous oxide (N_2O) as precursors at 10 and 90 sccm, respectively. Radio-frequency (rf) power and substrate temperature were 500 W and 300 °C, respectively. The Ta barrier was sputtered from a Ta target in Ar ambient at a pressure of 2 mTorr, while the TaN barrier was reactively sputtered using the same Ta target with Ar/N_2 flow rates of 20/5 sccm at the same pressure of 2 mTorr. The PVD-Ti or TiN barrier layer was deposited on the SiOC:H layer using a sputtering system with a base pressure of 5×10^{-7} Torr and no intentional substrate heating. A CVD-Ti or TiN film was deposited by plasma-enhanced chemical vapor deposition (PECVD) at a temperature of 550 °C, using a mixture of $TiCl_4$, NH_3, H_2 and Ar. The process chamber pressure was at 5 Torr and the rf power was 350 W. The Cu overlay (200 nm) was sputtered onto the barrier layer at room temperature to form a Cu/barrier/SiOC:H/SiO_2/Si MIS structure. The prepared samples were then annealed at 10^{-7} torr for 30 min under various temperatures up to 700 °C, to determine the thermal stability of the samples. A 200-nm-thick Al film was sputtered onto the backside of the wafer to produce an excellent electrical contact.

The sheet resistance (R_s) measurement using the four-point probe method was employed to characterize the obtained barrier films. The surface roughness and morphology of the films were determined using the atomic force microscope (AFM, Digital Instruments Nano-Scope III) with a 0.5 Hz scanning frequency in an air ambient. A thermal desorption spectrometer (TDS, Hitachi Tokyo Electronics) was utilized to monitor the amount of moisture desorbed from the SiOC:H film. The diffusion and reaction that took place at the interfaces or surface of the barrier/SiOC:H caused by annealing were estimated by comparing surface micrographs obtained by a thermal emission scanning electron microscope (TFSEM, JEOL JSM-6500F). Auger electron spectroscopy (AES, VG Microlab 310F) was used to determine the composition of the diffusion barrier films.

For the thermal stability and electric properties study, the dielectric breakdown of the MIS capacitors was measured by applying a voltage ramp stress using a Hewlett-Packard (HP4156B) semiconductor parameter analyzer with the MIS capacitors biased at accumulation polarity. The breakdown electric field (E_{bd}) is defined as the electric field at which the capacitor's leakage current density exceeds 1×10^{-6} A cm^{-2}, and at least 20 capacitors were measured in each category to construct the breakdown statistics. Bias-temperature stressing (BST) experiments were performed with MIS structures at 250 °C and at bias 2 MV cm^{-1}.

3. Results and discussions

Fig. 2 presents the TDS spectra of the SiOC:H/Si sample from 25 to 800 °C. In the TDS spectra, the primary peaks observed are H_2O with a major mass peak at 18 and CH_4 with a major mass peak at 16, physically and chemically absorbed in the SiOC:H film. TFSEM analysis was used to analyze the microstructure

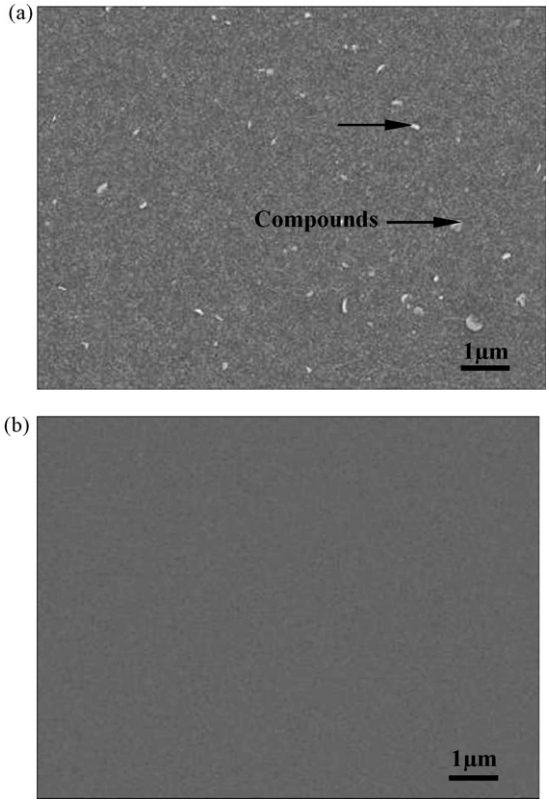

Fig. 3. Top-view SEM micrographs showing the surface morphologies of the: (a) CVD-Ti and (b) PVD-Ti films on SiOC:H films.

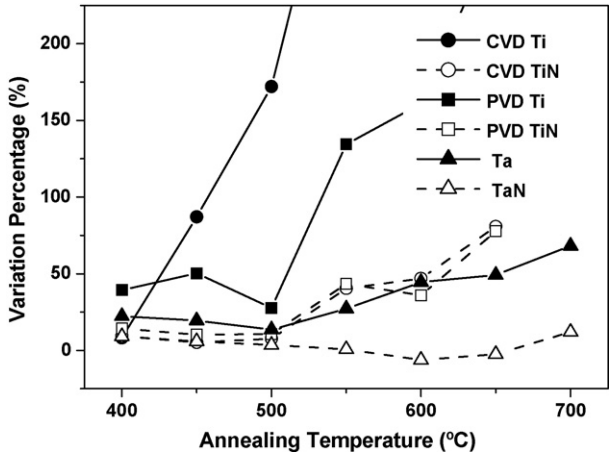

Fig. 4. Variation percentage in sheet resistance of diffusion barrier layers on SiOC:H/Si structures as a function of annealing temperature.

and identify possible surface reactions. Fig. 3 present the top-views of the as-deposited Ti on SiOC:H using CVD and PVD system. Fig. 3(a) indicates that some fine compounds and cracks are present on the surface of the CVD-Ti/SiOC:H sample, but almost no compound is found on the surface of the PVD-Ti/SiOC:H sample, as depicted in Fig. 3(b). The formation of the compounds was caused by the reaction between the inorganic precursor ($TiCl_4$) with SiOC:H in CVD-Ti deposition. A considerable amount of O atoms desorbed from SiOC:H, which is confirmed using TDS analysis, and reacted with Ti atoms to form a Ti(O) compound, raising the resistivity of Ti significantly. Moreover, Ti atoms begin to react and form silicide at ~550 °C [17].

The variation of sheet resistance as a function of the annealing temperature is commonly used to examine the capability of reaction between diffusion barriers and SiOC:H film. The difference of sheet resistance between the annealed and as-deposited samples, divided by the sheet resistance of as-deposited samples, is called the variation percentage of sheet resistance and is defined as follows [18]:

$$\frac{\Delta R_s}{R_s}(\%) = \frac{R_{s,\text{annealed}} - R_{s,\text{as-deposited}}}{R_{s,\text{as-deposited}}} \times 100 \quad (1)$$

Fig. 4 plots the variation percentage in sheet resistance of the barriers/SiOC:H samples following furnace annealing for 30 min at various temperatures. The results indirectly reveal the interactions between the diffusion barriers and SiOC:H. Except for that of CVD-Ti sample, the sheet resistance initially declines gradually as the annealing temperature increases because the number of crystal defects reduce and the grains of the diffusion barrier films grow. However, at certain temperature, the reactions between the diffusion barriers and the SiOC:H result in failure of the diffusion barriers, and the formation of compounds. The increase in sheet resistance of the Ti sample is higher than those in TiN and TaN samples.

Fig. 5(a) and (b) shows the experimental content percentage of C and O resulting from the interactions of the barriers with SiOC:H, based on the AES. The analyses show the as-deposited and annealed CVD and PVD-Ti, TiN, Ta and TaN

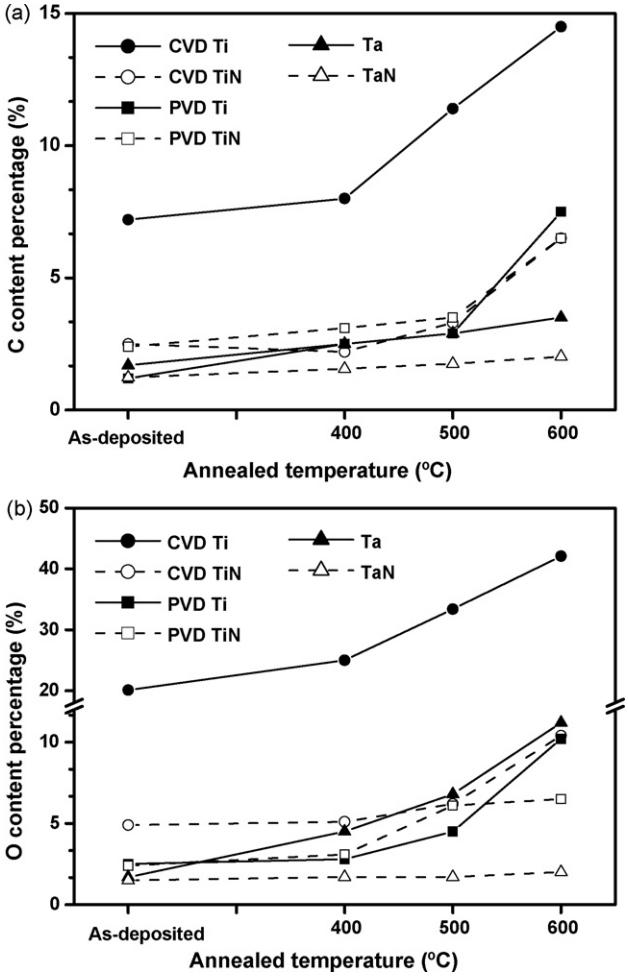

Fig. 5. Experimental content percentage of: (a) C and (b) O resulting from the interactions of the barriers with SiOC:H before and after annealing at 400–600 °C, based on the AES.

films on SiOC:H films upon 600 °C. As shown in Fig. 5, it is obvious that the as-deposited CVD barrier films, especially the CVD-Ti film, have a much higher C and O contents than the PVD barriers. Reaction occurs in CVD-Ti/SiOC:H system due to the decomposition of SiOC:H into Ti during deposition at 550 °C. Upon 400 °C annealing, a significant amount of C and O atoms incorporate into the Ti film. The high content of C and O are due to the formation of the Ti(C) and Ti(O) compounds. For the PVD-Ti film, the AES results are in consistent with sheet resistance analysis, showing the formation of compounds above 500 °C annealing. Moreover, the CVD-TiN film has higher C and O contents than other nitride films. However, there is the evidence of the low reaction between TaN and underlying SiOC:H film.

Fig. 6 displays the AFM images of the PVD-Ti, PVD-TiN and CVD-TiN layers on SiOC:H films. Fig. 6(a) and (b) reveals that the PVD-barriers have a great roughness and a significantly columnar microstructure, which can enhance the rapid out-diffusion (at the grain boundaries) of H atoms [16]. As shown in Fig. 6(c), the CVD-TiN film has a low roughness and fine-grained microstructure so the out-diffusion path of H atoms from the SiOC:H film reduces. Hence, the CVD-TiN barrier is

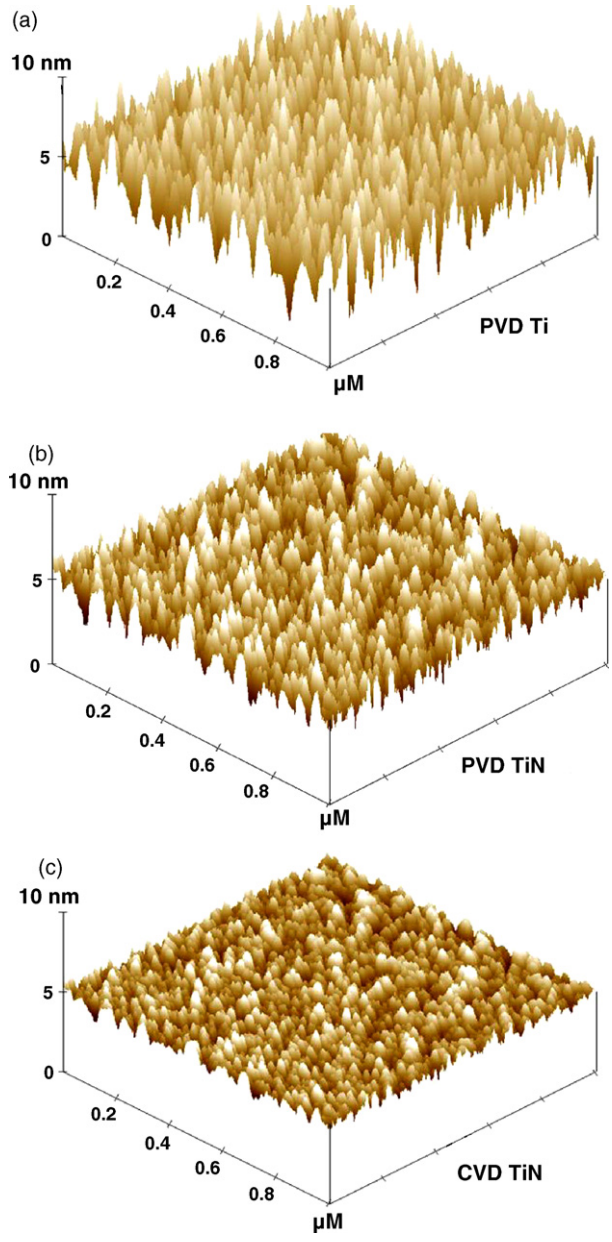

Fig. 6. AFM images of the: (a) PVD-Ti, (b) PVD-TiN and (c) CVD-TiN MIS capacitors.

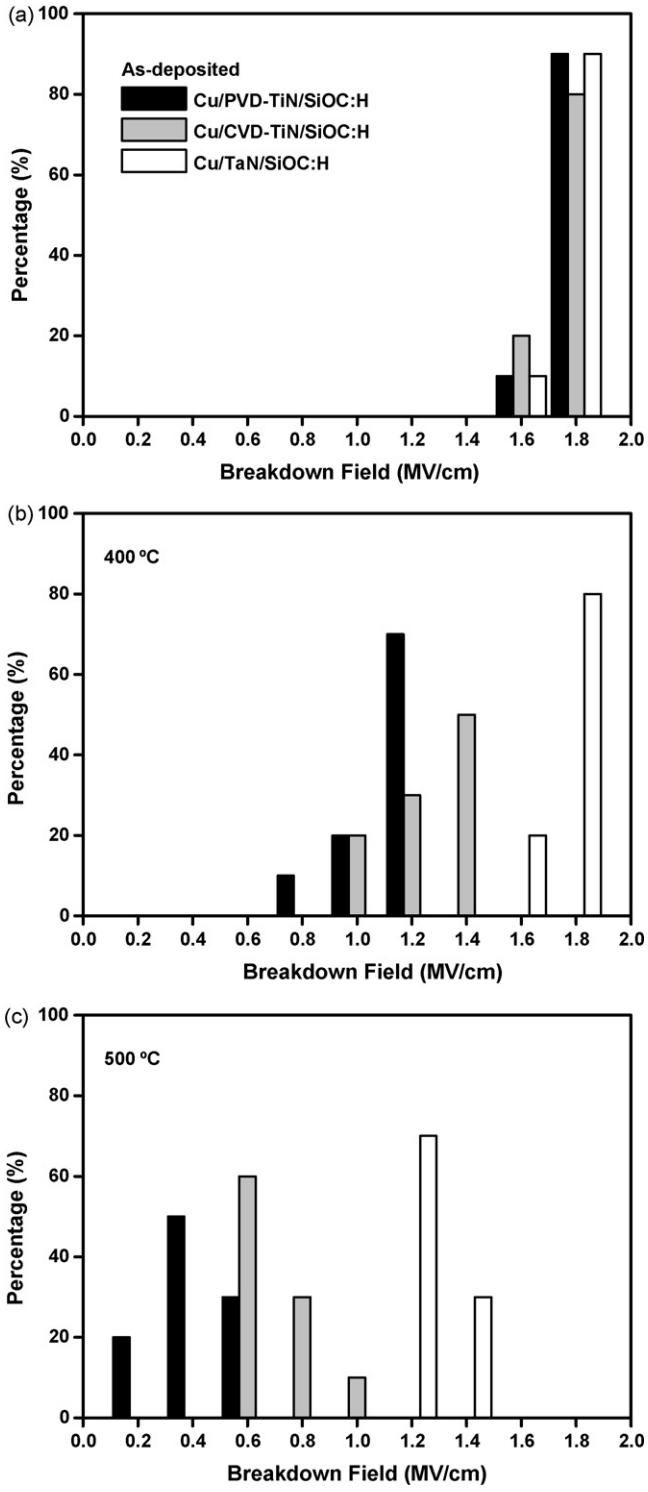

Fig. 7. Breakdown field distributions of (a) as-deposited Cu/barrier/SiOC:H MIS capacitors and after annealing at (b) 400 °C and (c) 500 °C for 30 min.

expected to be more resistant to the out-diffusion of H atoms than PVD-TiN barrier. Accordingly, the C and O impurities are speculated to stuff the grain boundaries of the finely grained CVD-TiN barrier and to block atomic diffusion—at least the initial out-diffusion of H atoms from SiOC:H. Moreover, O impurities can stuff the grain boundaries of TiN, enhancing the property of TiN barrier layers [19]. Atoms normally diffuse much more quickly through grain boundaries than through the crystal lattice. However, the diffusion of H atoms through the lattice is also fast because these atoms are small and have extremely high mobility. The Ti film has a hexagonal close-packed (hcp) structure with two types of interstitial sites—octahedral and tetrahedral [20]. The atomic radius of H ($r_H = 0.2r_{Ti}$) is less than the minimum radius of the interstitial sites, so such interstices can provide the lattice diffusion paths for H atoms. However, the TiN film has a NaCl-type face-centered-cubic (fcc) structure, with Ti atoms' occupying normal fcc lattice sites and N atoms' filling the octahedral interstitial sites [21]. N atoms block the lattice diffusion paths for H atoms, so the lattice diffusion coefficient of H diffusion in the Ti barrier layer exceeds that of the TiN film.

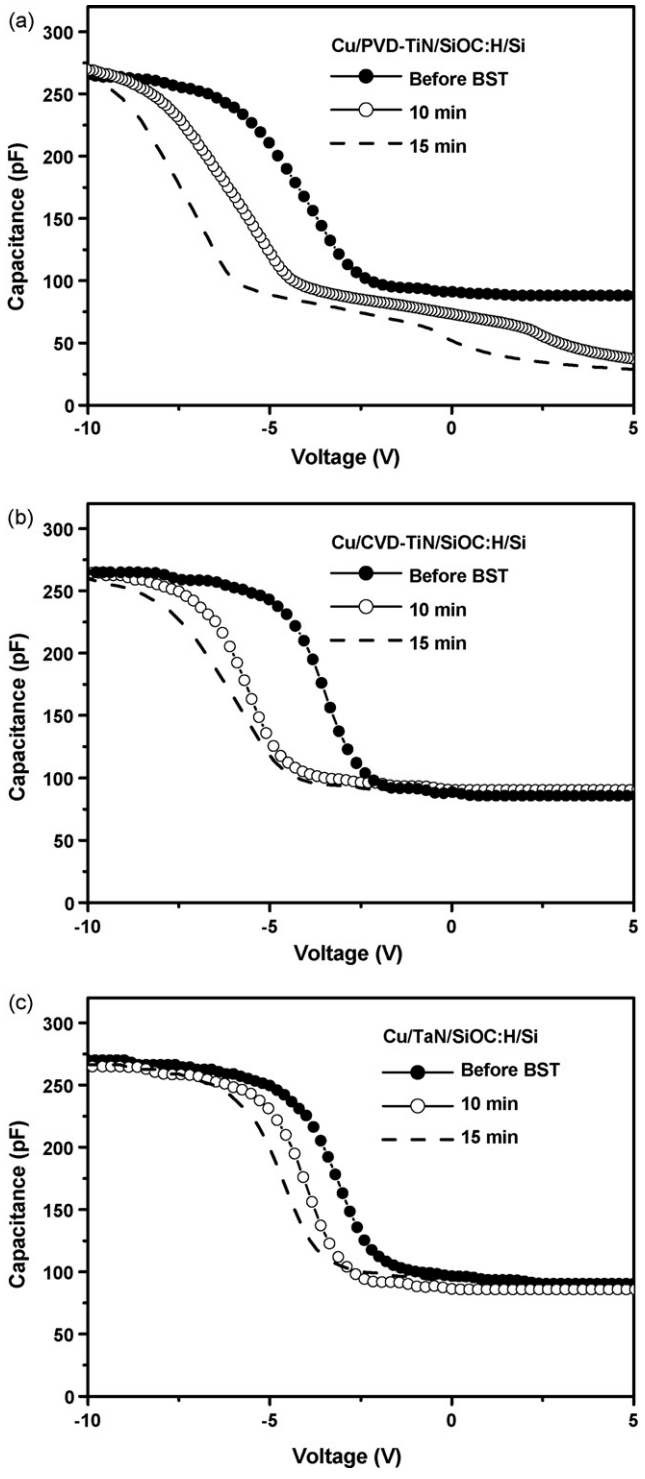

Fig. 8. *C–V* characteristics of Cu/barrier/SiOC:H MIS capacitors after BTS at 2 MV cm^{-1} and 250 °C for the: (a) PVD-TiN, (b) CVD-TiN and (c) TaN layer.

Fig. 7 illustrates the distribution of breakdown field for the as-deposited Cu/barrier/SiOC:H MIS capacitors having a CVD-TiN, PVD-TiN as well as TaN diffusion barrier after annealing at 400 and 500 °C for 30 min. Compared to the samples with CVD and PVD-TiN diffusion barrier, significant improvement in thermal stability was obtained, apparently due to the barrier effectiveness of a TaN layer. In fact, the sheet resistance measurement was reported that the TaN barrier in MIS capacitor can sustain a 30 min thermal annealing up to 600 °C, without causing degradation to the devices' electrical characteristics. Thus, the TaN diffusion barrier layer is believed to be enhanced the thermal stability of the Cu and SiOC:H in back-end process.

Fig. 8 shows the *C–V* results of MIS capacitors subjected to BTS at 250 °C for different stressing time. In BST/*C–V* analysis, capacitors were stressed under 60 V (2 MV cm^{-1}). The Cu^+ ions drift rate will change when stressing time increase. This can happen because Cu^+ ions can pile up at a dielectrics-Si interface creating increasing electric field opposing the external electric field. Continuous flat band voltage shift (ΔV_{FB}) in negative direction under 2 MV cm^{-1} is likely caused by Cu^+ ions drift through SiOC:H and reached SiO_2–Si interface or even gone into Si substrate. For the Cu/PVD-TiN/SiOC:H MIS capacitor, ΔV_{FB} is much larger than that of other capacitors, thus, some of these Cu^+ ions might become neutralized and generate electrically effective trap centers near the Si interface and in bulk Si substrate. These deep-level states generated by Cu near the SiO_2–Si interface reduce the device lifetime. As shown in Fig. 8(c), the constant inversion capacitance of Cu/TaN/SiOC:H MIS capacitor after BTS suggests that low Cu^+ ions drift through SiOC:H and reach SiO_2-Si interface, as expected.

4. Conclusion

The interactions between low-*k* dielectric SiOC:H and diffusion barrier layers varied with the annealing temperature. Deposition of CVD-Ti layer at 550 °C, O and C atoms were dissolved into the Ti film to form Ti(O) and Ti(C) compounds, increasing the sheet resistance. The Ti did not improve the loss of H from SiOC:H caused by the thermal decomposition, however, the TiN block the lattice diffusion path for H atoms. The drift of Cu^+ ions was used to investigate the effectiveness of diffusion barrier layers using BST/*C–V* analysis. Under a 2 MV cm^{-1} electric field, higher Cu^+ ions drift resistance for TaN layer was compared to CVD and PVD-TiN layers.

Acknowledgements

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