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A process for high yield and high performance carbon nanotube field effect transistors

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ABSTRACT

Carbon nanotube field effect transistors (CNTFETs) have been considered as one of the potential candidates for nanoelectronics beyond Si CMOS. However, it is not easy to have high performance CNTFETs with high yield currently. In this work, we proposed a local bottom-gate (LBG) CNTFETs combined with a novel device concept and optimized process technologies. High performance of CNTFET with low subthreshold swing of 139 mV/dec, high transconductance of 1.27 μS, and high I_{on}/I_{off} ratio of 10^6 can be easily obtained with Ti source/drain contact after a post annealing process. Record high yield of 74% has been demonstrated. On the basis of the proposed process, lots of high performance CNTFETs can be obtained easily for advanced study on the electrical characteristics of CNTFETs in the future.

1. Introduction

In recent years, to further scale down the geometry of field effect transistors and improve device performance, carbon nanotube field effect transistors (CNTFETs) have attracted much attention as a candidate for beyond-Si technology [1–3]. The diameter of a single-wall carbon nanotube (SWCNT) ranges from 1 nm to 2 nm. The quasi one-dimensional structure enhances carrier mobility dramatically. According to literatures, the intrinsic mobility of a semiconducting SWCNT can exceed 100,000 $cm^2 V^{-1} s^{-1}$ at room temperature and some high performance CNTFETs have been demonstrated [4–6].

Most of the CNTFETs studied so far have adopted a top-gate structure, as shown in Fig. 1a [5,6]. The top-gate CNTFET is a SWCNT-first and gate-last process. The SWCNT channel can be fabricated by either in situ growth or spin-coating process. For the in situ growth of SWCNT, it is still hard to control the chirality and the number of SWCNT across between source and drain. In addition, the source/drain (S/D) contact metal is usually patterned by lift-off process instead of dry etching process, and the gate dielectric must be deposited by atomic-layer deposition technique to obtain good surface coverage on the SWCNTs. Therefore, the most apparent drawbacks of the conventional top-gate CNTFETs are: (1) high gate leakage current caused by the source/drain lift-off process at the gate to S/D overlap region and (2) low manufacturing yield due to the SWCNTs spin-coating process.

To further reduce the gate leakage current at the gate to S/D overlap region and increase the manufacturing yield of the CNTFETs, we proposed a gate-first local bottom-gate (LBG) process. The gate electrode is patterned by dry etching process instead of the typically used lift-off process. The schematic device structure is shown in Fig. 1b. After process optimization, the LBG-CNTFETs can achieve high yield and high performance goals using a simple SWCNTs spin-coating process.

2. Device fabrication

The starting material was a silicon substrate covered by a 15 nm thick pad oxide (SiO_2) formed by thermally oxidation and a 150 nm thick silicon nitride (Si_3N_4) formed by low-pressure chemical vapor deposition (LPCVD). Two kinds of LBG stacks were prepared, one is n^+ poly-Si(60 nm)/Al_2O_3(10 nm) and the other is TiN(40 nm)/Si_3N_4(30 nm). The 60 nm thick n^+ poly-Si gate was deposited by a in situ phosphorus doped LPCVD process followed by a 900 °C rapid-thermal annealing for 20 s to activate the dopants. The 40 nm thick TiN gate electrode was deposited by a sputtering system. The poly-Si local bottom-gate was patterned by a dry etching process to form individual local bottom-gate electrodes, while the TiN local bottom-gate was patterned by a lift-off process. In order to control the thickness of these two LBG stacks to 70 nm accurately, a 10 nm thick Al_2O_3 gate dielectric was deposited by an atomic-layer deposition (ALD) system, while a 30 nm thick Si_3N_4 was deposited by a plasma-enhanced chemical vapor deposition (PECVD) process.

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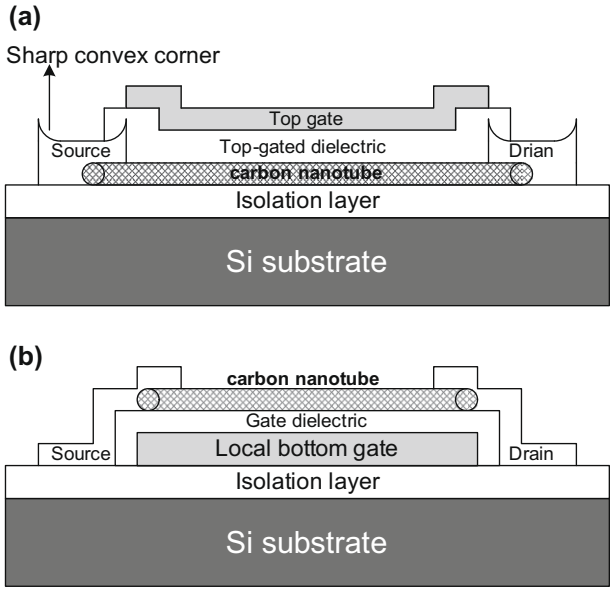

Fig. 1. (a) Schematic structure of the conventional top-gate CNTFETs with sharp convex corner at the source/drain edge due to the lift-off process for source/drain patterning. (b) Schematic structure of the local bottom-gate CNTFETs. As the gate is patterned by dry etching, sharp convex corner as shown in the figure would not exist.

The CNTs were commercially available Carbolex AP-grad SWNTs which were grown by arc-discharge technique. The average diameter of the SWCNTs is 1.4 nm, which is calculated from the radial breathing mode (RBM) of a high-resolution Raman spectroscopy [7]. For the spin-coating process, a 0.25 mg CNT powder was dissolved in 40 ml dimethylformamide (DMF) solution followed by a sonication for 24 h. The solution was then spun onto the substrates by a two-step process. The first step was at 500 rpm for 10 s and the second step was at 2500 rpm for 60 s. The purpose of the first lower rotation speed step is to distribute SWCNTs on the substrate uniformly. The rotation speed of the second step depends on the step height of the LBG stacks and will be explained later. After SWCNTs coating, the substrates were then placed on a hot plate at 150 °C for 10 min to desorb the DMF molecules from substrates. Three kinds of source/drain contact metal, titanium (Ti), nickel (Ni), and chrome (Cr), were deposited by a sputtering system and were patterned by a lift-off process. The gate to S/D overlap length to modulate the schottky barrier at source/drain contact region was designed to 50 nm on each side. Finally, a post-deposition annealing (PDA) process in a high vacuum system at 600 °C for 180 s was performed to form good ohmic contact between source/drain metal and CNTs.

3. Results and discussion

Fig. 2 shows the typical transfer characteristics ($I_d - V_g$) at $V_d = 0.1$ V of the LBG-CNTFETs with a lift-off TiN gate. High gate leakage current of 5×10^{-8} A is observed at $V_g = 4$ V. This high leakage current can be explained by the cross-sectional scanning electron microscopic (SEM) image as the inset in Fig. 2. At the LBG edge, a sharp convex corner exits because of the tapered shape of the photoresist in a lift-off process. The photoresist sidewall will be covered by TiN film and the TiN film will be teared-open as the photoresist was dissolved by acetone. The convex corner can be as high as several hundred nanometers. This sharp convex corner results in a non-conformal gate dielectric deposition, which in turn results in higher gate leakage current due to the gate dielectric

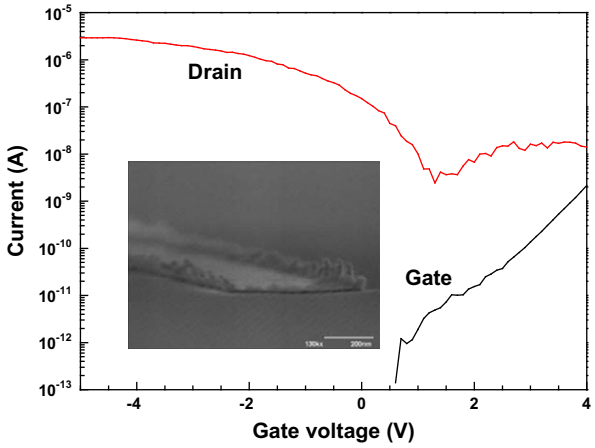

Fig. 2. Transfer characteristics of the LBG-CNTFETs with a lifted-off TiN local bottom-gate. The insert shows the cross-sectional SEM image of the sharp convex corner formed at the lifted-off gate edge.

thinning and local electric field enhancement. Furthermore, the high and sharp convex corner will block CNTs during the spin-coating process. Lots of CNTs will accumulate at gate edge to result in leakage path between source and drain. The high turn-off current shown in Fig. 2 is the result of the leakage path. This problem can be relaxed by utilizing reentrant shape or *T*-shape photoresist. However, the reentrant shape thick photoresist are difficult to form fine pattern. Furthermore, the actual bottom dimension of both shapes of photoresist can not be inspected by in-line SEM. Since the lift-off process have been give-up at 2 μm process technology, this work did not attempt to optimize the lift-off process in this work.

As the gate-first process of the LBG-CNTFETs constructs a 50–70 nm step height, this step height will trap some CNTs at first and then these trapped CNTs will be flung across the local bottom-gate region during the spin-coating process. Thus, the possibility for CNTs to cross gate region between source and drain can be improved dramatically. The results also depend on the spin speed at the second step of the spin-coating process. These SWCNTs could not be trapped easily by the LBG at slower rotation speed (<2000 rpm) or faster rotation speed (>3000 rpm). Fig. 3 shows the SEM image of a CNT connecting source and drain metal. The most suitable step height is around 50–70 nm according to our experience. Smaller step height cannot trap CNTs efficiently and

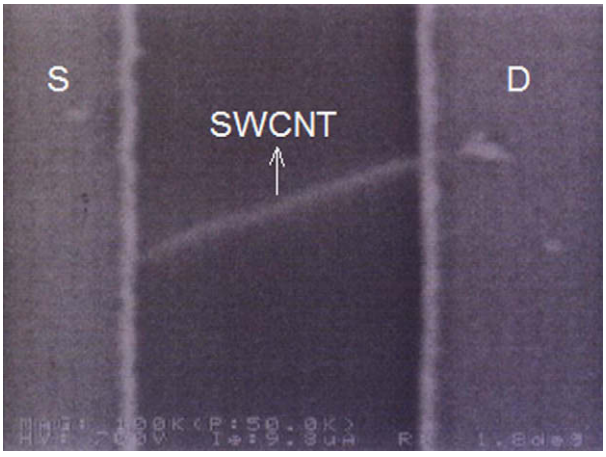

Fig. 3. Top-view SEM image reveals a CNT crosses between source and drain electrode.

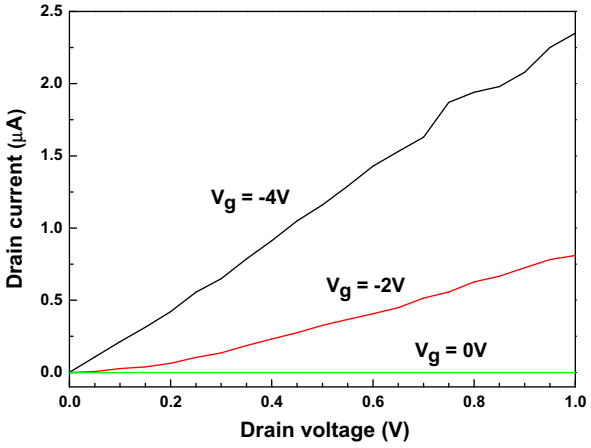

Fig. 4. Output characteristic of the LBG-CNTFET with poly-Si(60 nm)/Al_2O_3(10 nm) gate stack.

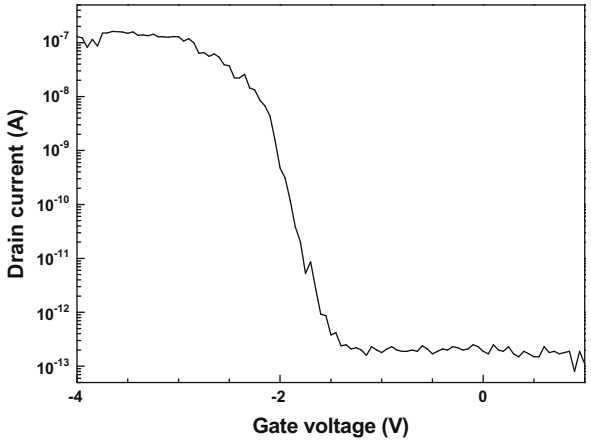

Fig. 5. Transfer characteristics of the LBG-CNTFET with poly-Si(60 nm)/Al_2O_3(10 nm) gate stack.

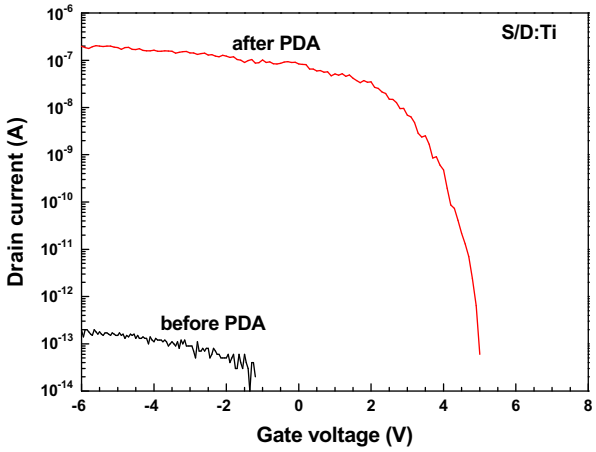

Fig. 6. Transfer characteristics of the LBG-CNTFET before and after 600 °C/180 sec PDA process with poly-Si(60 nm)/Al_2O_3(10 nm) gate stack and Ti S/D contact metal.

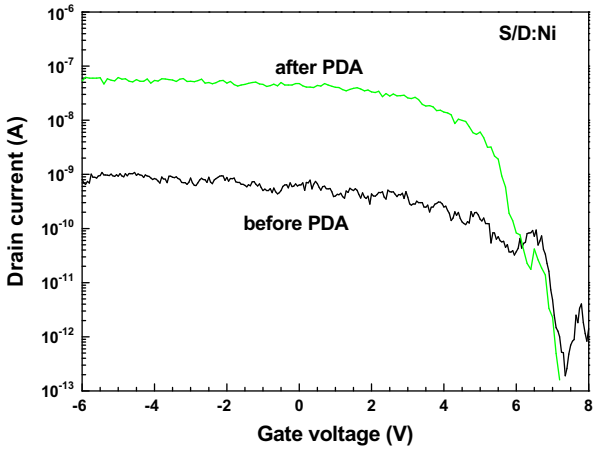

Fig. 7. Transfer characteristics of the LBG-CNTFET before and after 600 °C/180 sec PDA process with poly-Si(60 nm)/Al_2O_3(10 nm) gate stack and Ni S/D contact metal.

higher step height will accumulate too many CNTs. The yield of the LBG-CNTFETs can achieve as high as 74% (119 working devices among 160 measured devices) after process optimization.

Figs. 4 and 5 shows the output ($I_d - V_d$) and transfer characteristics ($I_d - V_g$) of the LBG-CNTFET device with poly-Si/Al_2O_3 gate stack, respectively. The linearity of the output characteristics at linear region agrees that Ti forms ohmic contact with the semiconducting CNT after PDA so that the device performance is mainly controlled by channel potential [8–11]. The drain current exceeds 2.5 μA at V_d = 1 V and V_g = −4 V. According to Fig. 5, the unipolar transport mechanism is due to hole conduction because of hole-injection from source to channel at negative LBG bias and no electron-injection from drain to channel at positive LBG bias. This LBG-CNTFET exhibits superior subthreshold swing of 139 mV/dec with a turn-on/turn-off current ration (I_{on}/I_{off}) ≈ 10^6 at V_d = −0.1 V. The maximum transconductance of the same LBG-CNTFET is 1.27 μS at V_g = −3.8 V. Table 1 lists the device parameters of our LBG-CNTFET and several best samples reported in literatures [12–14]. It is clear that the performance of the proposed LBG-CNTFET with poly-Si/Al_2O_3 gate stack is compatible with the published CNTFETs and the high performance goal has been reached.

It should be noted that the PDA process greatly impacts the yield of the high performance LBG-CNTFETs. In this work, the S/D

Table 1
Device parameters of the proposed LBG-CNTFET and some published best results [12–14].

	Sample A [12]	Sample B [12]	Sample C [13]	Sample D [14]	Our results
CNT diameter	1.7 nm	1.7 nm	1.7 nm	1.7 nm	1.4 nm
S/D metal	Ti	Ti	Ti	Pd	Ti
Gate material	Si	Si	Ti	Al	Si
Gate dielectric	SiO_2 (15 nm)	SiO_2 (90 nm)	SiO_2 (15 nm)	HfO_2 (8 nm)	Al_2O_3 (10 nm)
Gate length	2 μm	2 μm	0.26 μm	0.05 μm	0.8 μm
I_{on}	4.5 μA	0.4 μA	–	–	2.5 μA
G_m	2.6 μS	0.03 μS	3.3 μS	30 μS	1.27 μS
I_{on}/I_{off}	10^5	10^5	10^5	10^3	10^6
SS (mV/dec)	98	165	130	110	139

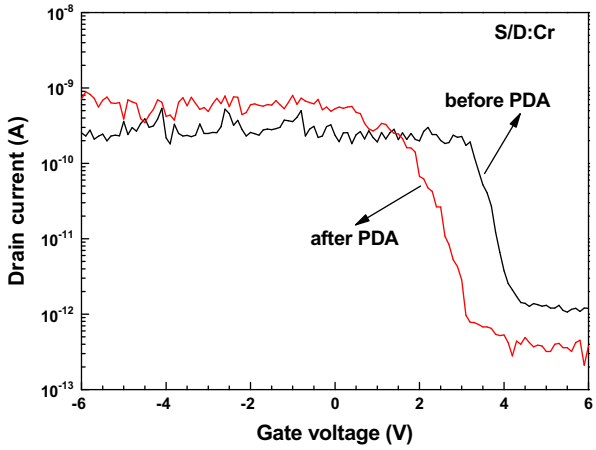

Fig. 8. Transfer characteristics of the LBG-CNTFET before and after 600 °C/180 sec PDA process with poly-Si(60 nm)/Al_2O_3(10 nm) gate stack and Cr S/D contact metal.

metal was deposited by a sputtering technique which is a non-conformal deposition process. Several nano-voids exist between CNTs and source/drain metal due to the high surface curvature of SWCNTs. These nano-voids will reduce the effective contact area. Furthermore, interfacial layer and/or contamination will also increase the contact resistance [15]. Hence, the contact resistance between CNTs and S/D metal would deteriorate the electrical performance of the LBG-CNTFETs seriously. The PDA process can minimize the nano-voids caused by the S/D metal sputtering and form titanium carbide (TiC) phase at the Ti/CNTs contact region to form ohmic contact [16]. Fig. 6 shows that suitable PDA process can increase the I_{on} by six orders of magnitude. Figs. 7 and 8 show the transfer characteristics ($I_d - V_g$) of the LBG-CNTFET with nickel (Ni) and chrome (Cr) as contact metal, respectively. The PDA process can increase the I_{on} by two orders of magnitude with Ni source/drain. No apparent improvement for the Cr contacted device due to the weak sticking and wetting effect between Cr and SWCNTs [17].

4. Conclusions

A novel LBG-CNTFETs with a gate-first process is proposed. High yield and high performance CNTFETs process using a SWCNTs spin-coating process has been demonstrated. The gate-first process constructs a 50–70 nm step height, which enhances the probability for CNTs to cross over the gate region between source and drain, and reduce gate leakage current. The record high yield of the LBG-CNTFETs is 74% after process optimization. High performance LBG-CNTFET with a superior subthreshold swing of 139 mV/dec, high transconductance of 1.27 μS, and high I_{on}/I_{off} ratio of 10^6 has been achieved with Ti source/drain after a 600° PDA process. Following the proposed process, a large amount of high performance CNTFETs can be fabricated easily for advanced study on the electrical characteristics of CNTFETs in the future.

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