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M. C. Wang, T. C. Chang, Po-Tsun Liu, R. W. Xiao, L. F. Lin, Y. Y. Li, F. S. Yeh, and J. R. Chen

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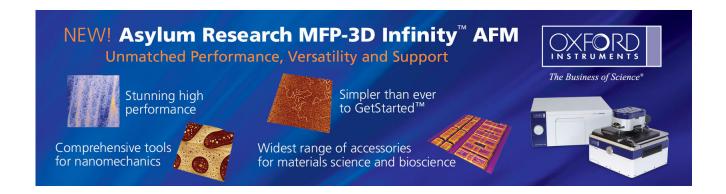
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n^+ -doped-layer-free microcrystalline silicon thin film transistors fabricated with the CuMg as source/drain metal

M. C. Wang

Department of Materials Science and Engineering, National Tsing Hua University, Hsin-Chui, 300 Taiwan, Republic of China

T. C. Changa)

Department of Physics and Institute of Electro-Optical Engineering, Center for Nanoscience and Nanotechnology, National Sun Yat-set University, 70 Lien-hai Road, Kaohsiung, 804 Taiwan, Republic of China

Po-Tsun Liu

Department of Photonics and Display Institute, National Chiao Tung University, Hsin-Chu, 300 Taiwan, Republic of China

R. W. Xiao, L. F. Lin, Y. Y. Li, and F. S. Yeh

Institute of Electronics Engineering, National Tsing Hua University, Hsin-Chui, 300 Taiwan, Republic of China

J. R. Chen

Department of Materials Science and Engineering, National Tsing Hua University, Hsin-Chui, 300 Taiwan, Republic of China

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The feasibility of using CuMg as source/drain metal electrodes for n^+ -doped-layer-free microcrystalline silicon thin film transistors (μ -Si:H TFTs) has been investigated. The Ohmic-contact characteristic has been achieved by using the CuMg alloy as source/drain metal. Furthermore, a wet etching process of Cu alloy source/drain metal has been completed by using the ferric chloride base etchant. The proposed μ -Si:H TFT has shown similar electrical characteristic with the μ -Si:H TFT with n^+ -doped layer. The experimental result also showed that the CuMg alloy was suitable for the replacement of n^+ -doped layer in thin film transistor liquid-crystal displays. © 2007 American Institute of Physics. [DOI: 10.1063/1.2749847]

Hydrogenated amorphous Si thin film transistors (a-Si:H TFTs) have been widely used as switching devices for active matrix liquid crystal displays. The a-Si:H TFT is particularly advantageous to the production of large flat panel displays and facilitates mass production. The main objectives for flat panel display application are to enhance the field effect mobility and to reduce the off-state leakage current under backlight illumination. Crystallized polycrystalline silicon (poly-Si) thin film transistors with high mobility are very attractive for peripheral circuit driver and switching applications in active matrix backplanes for flat panel displays and imagers. This is particularly true with active matrix organic light emitting diode displays. However, poly-Si suffers from high cost, complex processing, and significant nonuniformity over large area.

As a result, hydrogenated microcrystalline silicon has recently received considerable attention as a viable alternative to its amorphous counterpart for large-area applications. In terms of TFT performance, not only a-Si:H TFTs employing $n^+\mu$ -Si:H as Ohmic contact layer show an improved electrical property but also fully μ -Si:H TFTs are expected to yield higher field effect mobility and better electrical stability. More importantly, μ -Si:H films can be prepared using low thermal budget glow discharge gas decomposition method, which is also a standard industrial technique for a-Si:H deposition. However, small grain sizes (a few tens

nanometer size), and poor quality at grain boundaries and at low thicknesses, are obstacles in achieving device grade μ -Si:H films for high performance μ -Si:H TFTs. In addition, most of the μ -Si:H TFTs reported have been fabricated using nonindustrial reactors such as very high frequency plasma enhanced chemical vapor deposition (PECVD), hot wire CVD, and electron cyclotron resonance CVD. It is very desirable to achieve high grade TFTs using intrinsic and doped μ -Si:H films by the standard PECVD compatible to mass production. Therefore, the direct deposition of high quality μ -Si thin films is a promising alternative for high mobility TFTs. 11-13 On the other hand, the Ohmic-contact characteristic of the μ -Si:H was also important for the application of μ -Si:H TFTs. Compared to its amorphous counterpart, highly doped microcrystalline silicon $(n^+-\mu-Si:H)$ is attractive due to its much higher conductivity and doping efficiency. However, the thickness of μ -Si:H was also limited by n^+ -etching process for the production concern. In this letter, the CuMg alloy was used as source/drain metal and provided self-aligned Ohmic-contact characteristic.

A 100-nm-thick MoW gate electrode was deposited and patterned on the glass substrate. It was followed that the back-channel-etched (BCE) μ -Si:H TFT devices were fabricated by depositing a 100-nm-thick silicon oxide (SiO $_x$), and a 100-nm-thick μ -Si:H active layer subsequently on the MoW gate using PECVD method. However, the n^+ -doped-layer was not deposited in the proposed structure compared with the conventional process. After the μ -Si:H

a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw

BCE Structure Process Flow

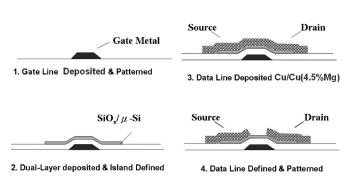


FIG. 1. Detail process flow of the proposed μ-Si:H TFT with the CuMg source/drain and back-channel-etched (BCE) inverted-staggered TFT structure.

active islands were patterned, a thin CuMg alloy layer (300 nm) was deposited by dc magnetron sputtering a 99.99% purity level of CuMg alloy target (4.5 at. % Mg) at room temperature. The sputtering condition of CuMg alloy was as follows: the base pressure of the deposition chamber was 7.0×10^{-7} torr, the Ar pressure was 6 mtorr, the sputtering power was 1500 W, and the substrate temperature was at room temperature. The CuMg metal films were patterned by wet etching process to form source/drain electrodes. The wet etching process of the CuMg alloy structure was also completed by introducing the ferric chloride base etchant, typically used in printed circuit boards. The etch rate of CuMg film was about 1.9 nm/s and the critical dimension loss was less than 1.4 μ m. The detail process flow was illustrated in Fig. 1. For comparison, the BCE μ -Si:H TFT devices with n⁺-a-Si:H layer were also fabricated by depositing a 100-nm-thick SiO_x, a 100-nm-thick μ -Si:H active layer, and a 50-nm-thick n^+ -a-Si:H layer subsequently on the MoW gate using PECVD method. After the μ -Si:H active islands were patterned, a 300-nm-thick sputter-deposited Al layer was patterned by wet etching process to form source/drain electrodes. Finally, the n^+ -a-Si:H layer on the TFT channel region was etched via the source/drain pattern electrodes as the etching mask. The channel length and width were 12 and 36 μ m, respectively. The μ -Si:H film was confirmed by Raman analysis and the scanning electron microscopy (SEM). The annealing stability of CuMg alloy as source/drain metal was also tested at 300 °C for 30 min in a vacuum chamber. The electrical measurement was carried out at an HP 4156C precision semiconductor parameter analyzer.

Figure 2 showed the Raman analysis of μ -Si:H. We deposited μ -Si:H films at 400 °C using a standard large-area single-chamber 13.56 MHz PECVD system by high H₂

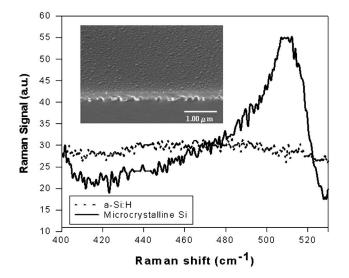


FIG. 2. Raman analysis of μ -Si:H and a-Si:H film. The inset shows the SEM surface profile of μ -Si:H.

dilution of SiH₄ process gas (H₂/SiH₄=80). The Raman peaks of the film were very sharp at 510 cm⁻¹. The full width half maximum (FWHM) was measured about 11 cm⁻¹. The Raman peak was deconvoluted using a Lorenztian multipeak function. The crystal fraction was calculated using the formula $(I_c+I_\mu)/(I_c+I_\mu+I_a)$ where I_c is the area of crystalline peak (520 cm⁻¹), I_{μ} is the area of the microcrystalline peak (510 cm⁻¹), and I_a is the area of the amorphous peak $(480 \text{ cm}^{-1})^{14}$ The resulting μ -Si:H film shows a Raman crystallinity (X_C) about 70% (Fig. 2). The films were analyzed for their surface morphology using SEM. As shown in the inset of Fig. 2, presence of small grains can be observed in the SEM image. The size of the grains and the grain size distribution across the film surface vary depending on specific deposition conditions of μ -Si:H and pretreatments on the silicon oxide surface. The performance of a bottom gate TFT with back-channel etch is very sensitive to the grain size distribution uniformity. It was, therefore, important to develop the thin film with uniform grain structure. The grain size of the μ -Si:H using SEM images was about 80 nm. Figure 3(a) shows the transfer characteristics of the n^+ -doped layer-free μ -Si:H TFT with the CuMg source/drain metal after annealing at high temperature process. 15,16 The proposed n^+ -doped layer-free μ -Si:H TFT with the CuMg alloy source/drain metal demonstrated the field-effect mobility of 0.1 cm²/V s, the subthreshold slope of 1.26 V/decode, and the threshold voltage of 5.02 V. The mobility was extracted from the linear I_D - V_G plot, where the drain voltage (V_D) is 0.1 V, and the threshold voltage was extracted from the lin-

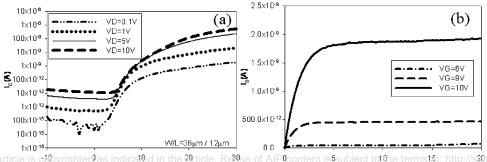


FIG. 3. (a) Transfer characteristics $(I_D\text{-}V_G\text{ curve})$ of $n^+\text{-}\text{doped-layer}$ free $\mu\text{-}\text{Si:H}$ TFT with the CuMg source/ drain metal after the 300 °C 30 min annealing process in the vacuum chamber. The channel length and width are 12 and 36 μm , respectively. (b) Output characteristics $(I_D\text{-}V_D\text{ curve})$ of $n^+\text{-}\text{doped-layer-free}$ $\mu\text{-}\text{Si:H}$ TFT with the CuMg source/drain metal after the 300 °C, 30 min anneal-

ear I_D - V_G plot, where the V_D =0.1 V. The a-Si:H-like characteristic was due to 20-nm-thick a-Si:H incubation layer in bottom-gate structure. The electrical characteristic of μ -Si:H TFT with the n^+ -doped layer also showed the same a-Si:H-like characteristic. Therefore, the a-Si:H-like characteristic was not due to the CuMg alloy as source/drain metal. Furthermore, the output characteristics of μ -Si:H TFT are also shown in Fig. 3(b), measured at the gate voltages sweeping from 6 to 10 V by a voltage step of 2 V. It is shown no current crowding effect appears in the CuMg alloy source/drain metal μ -Si:H TFT device. This indicates also the voltage applied on the TFT was not limited by the source/ drain contact resistance. According to pervious report, the Ohmic behavior is observed for metals having work function (Φ_m) lower than the electronic affinity (χ_s) of the Si film $(\chi_s \sim 4.0 \pm 0.1 \text{ eV})$. Because the Φ_m of Mg was 3.46 eV, the Mg was easily to form the Ohmic contact with μ -Si:H.¹⁷ The μ -Si:H layer also reduced the contact resistance. According to previous report, 18 the carrier transfer mechanism across the barrier is a thermally activated process, the contact resistance will be proportional to the Si film resistivity. As s result, the lower Si film bulk resistivity is resulted in lower contact resistance. The similar electrical characteristic of μ -Si:H TFT with n^+ -a-Si doped layer also indicated the good Ohmic-contact characteristic of CuMg alloy structure.

The μ -Si:H TFT device without n^+ -a-Si doped layer has been developed in this work. The CuMg alloy film acting as the source/drain electrode could replace the n^+ -a-Si doped layer due to the lower work function (Φ_m) of Mg than the electronic affinity (χ_s) of Si film and the use of μ -Si layer to reduce the contact resistance. Compared to the μ -Si:H TFT with n^+ -doped layer, the μ -Si:H TFT with CuMg alloy source/drain metal exhibited the similar electrical performance. For the production concern, the CuMg source/drain metal could be applied for the TFT with the n^+ -doped layer-free process and provided self-aligned Ohmic-contact characteristic.

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