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(54) MINIATURE INDUCTOR SUITABLE FOR INTEGRATED CIRCUITS

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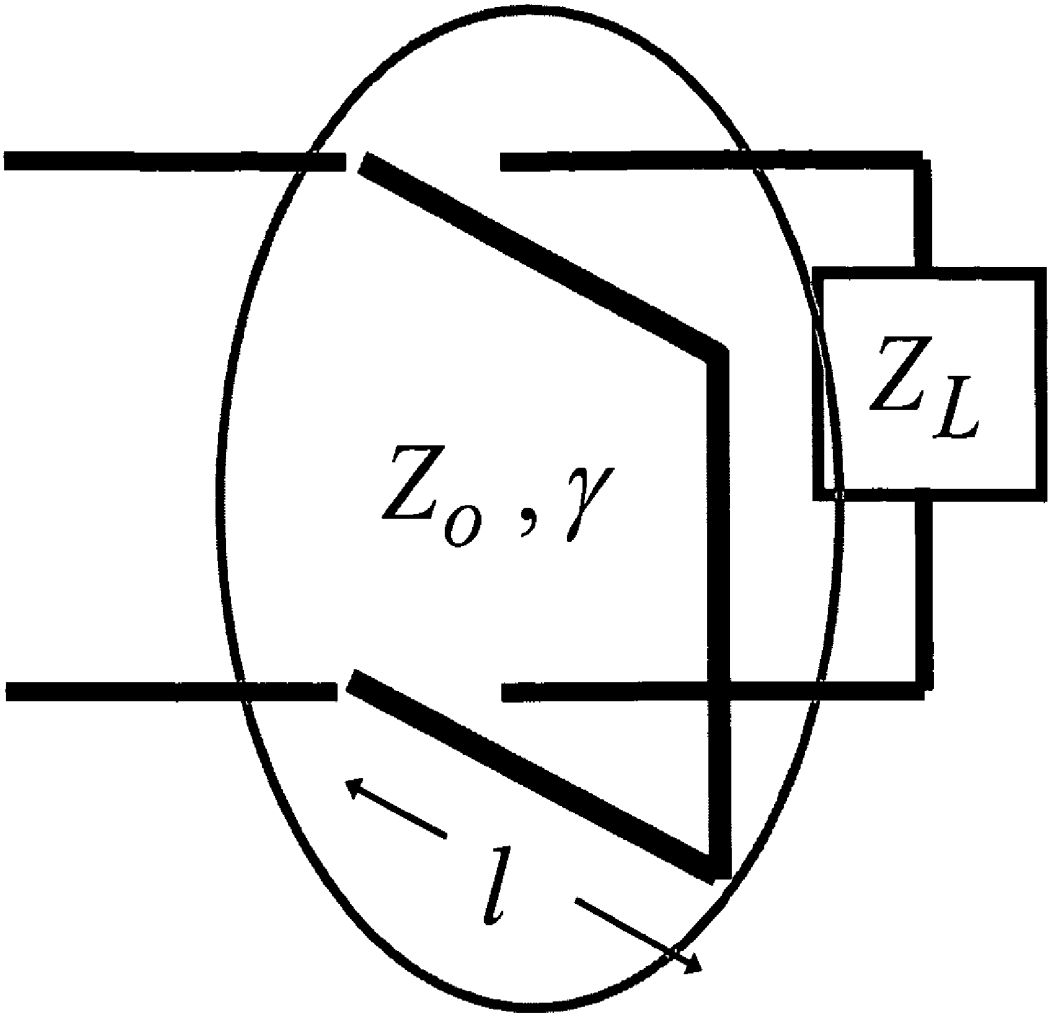
(57) **ABSTRACT**

A miniature inductor suitable for integrated circuits comprises a semiconductor substrate having a coplanar strip line and a plurality of metal-insulator-metal (MIM) capacitors, wherein the plurality of MIM capacitors are connected between the transmission lines of the coplanar strip line in parallel, and the coplanar strip line connected with the MIM capacitors further comprises a crossed planar strip line structure or a shifted planar strip line structure. The present invention reduces the occupied area for an inductor by adding the MIM capacitors and folding the transmission lines, and alleviates the quality factor degradation of the inductor caused by substrate loss.



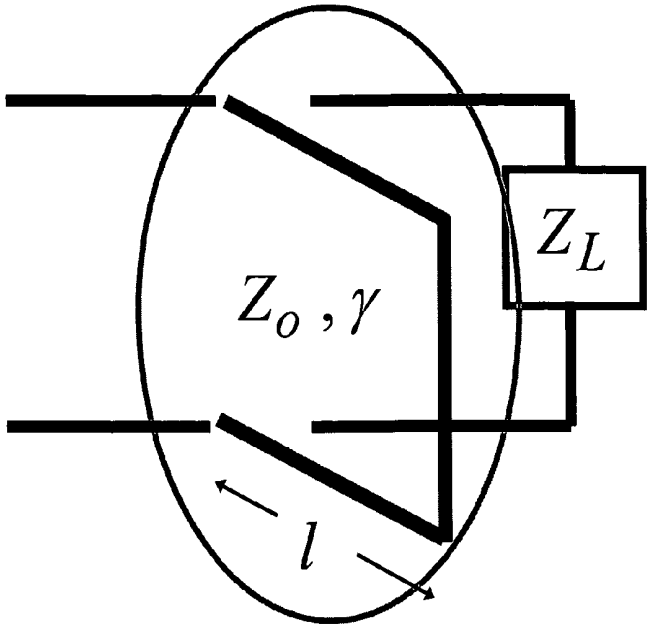


FIG. 1

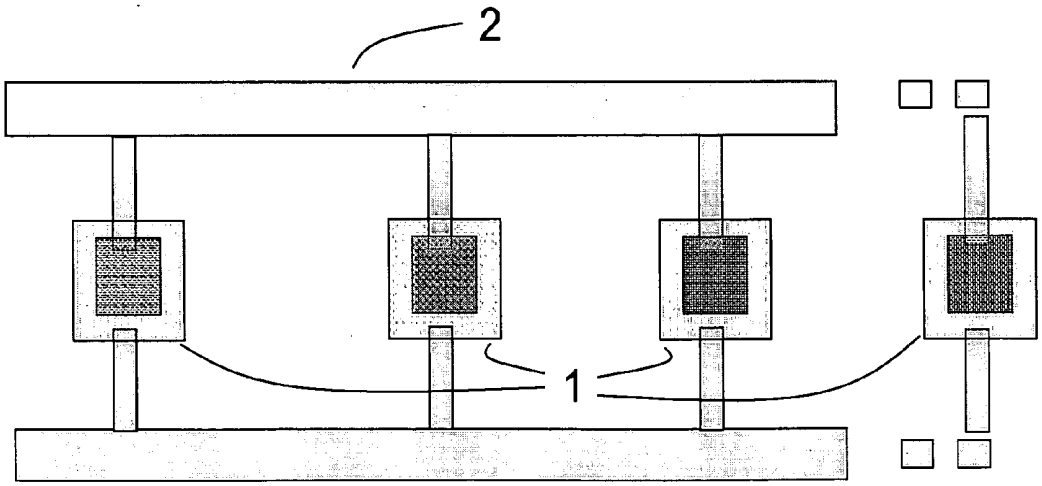


FIG. 2

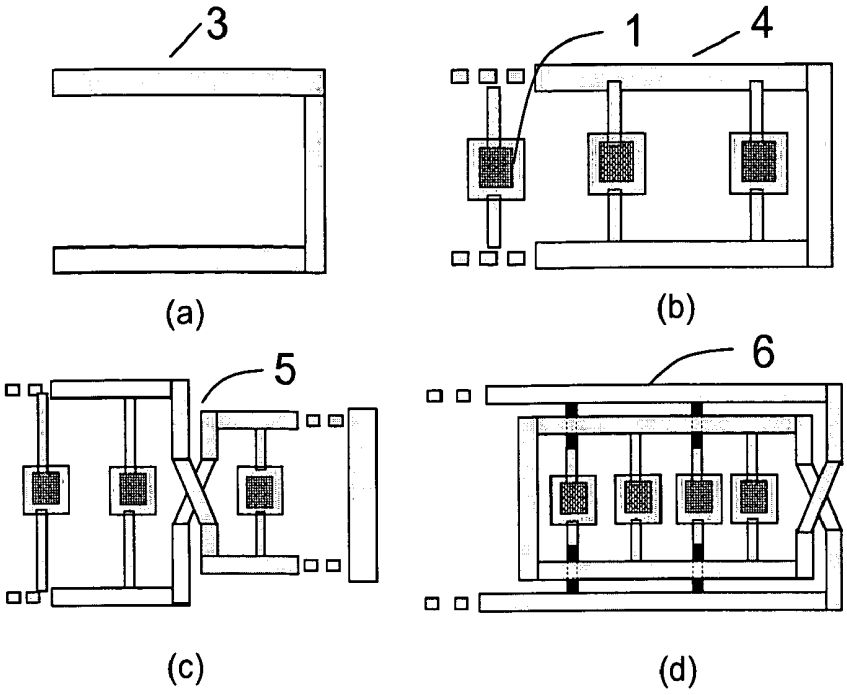


FIG. 3

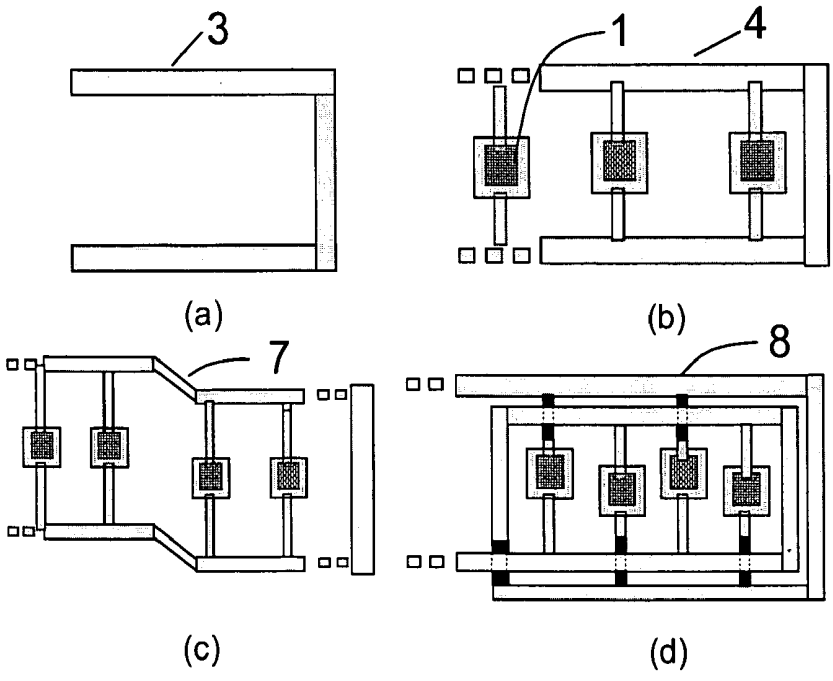
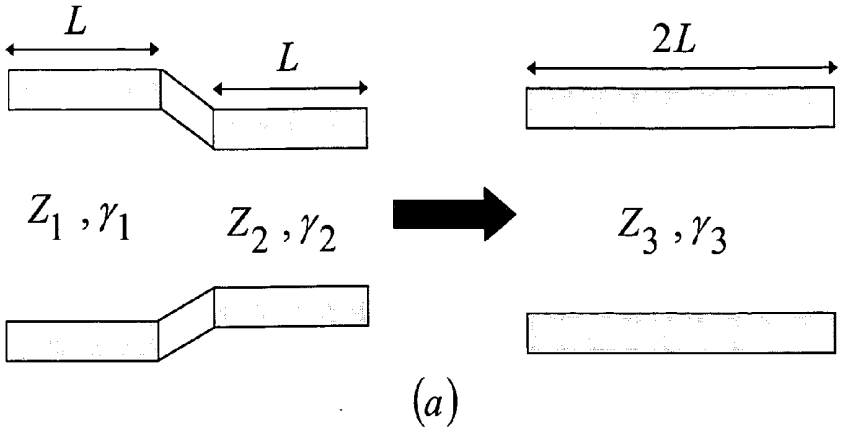
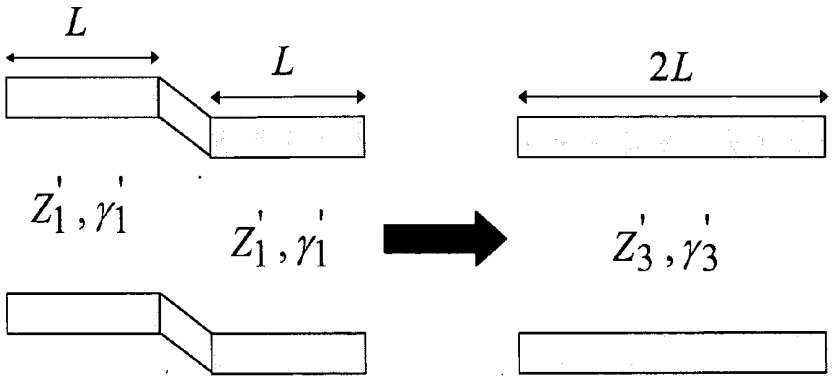


FIG. 4

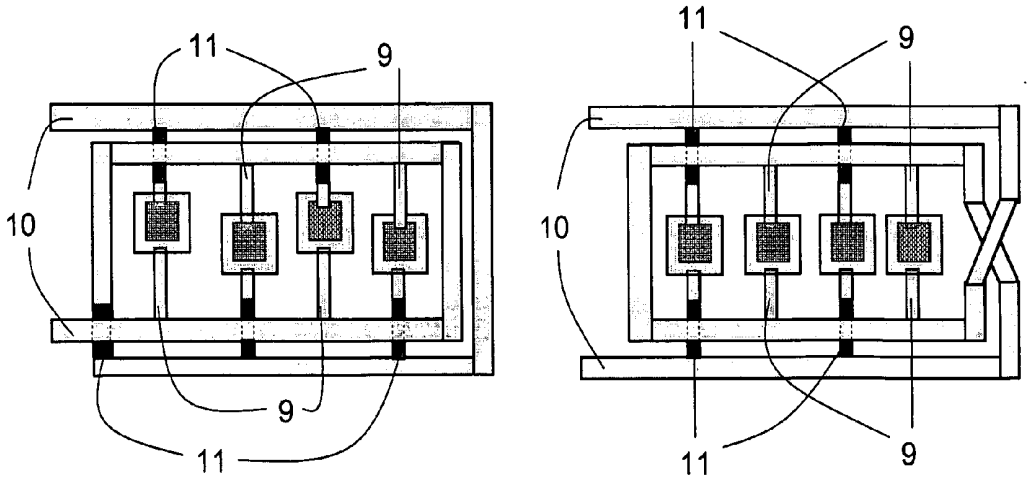


(a)



(b)

FIG. 5



(a) (b)

FIG. 6

MINIATURE INDUCTOR SUITABLE FOR INTEGRATED CIRCUITS

BACKGROUND OF THE INVENITON

[0001] 1. Field of the Invention

[0002] The present invention relates to a miniature inductor suitable for integrated circuits, and in particular to a miniature inductor having a folded coplanar strip line.

[0003] 2. Description of the Related Art

[0004] In the prior art, a miniature inductor for integrated circuits occupies a quite large area, and is easily affected by material loss, and has low quality factor and low self-resonant frequency.

[0005] Currently, there are various ways to manufacture an inductor in general integrated circuit manufacturing process technology. For example, U.S. Pat. No. 6,714,113, entitled "Inductor for Integrated Circuits", filed in April 2004 by W. Abadeer et al., and Paper "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," IEEEMTT, January 1996, submitted by J. N. Burghartz et al. all use a microstrip line structure, which is planar. Although it adopts a spiral line shape or a folded line shape, the disadvantage is that it takes up a larger area. Moreover, in integrated circuit silicon manufacturing process, an inductor is easily affected by substrate loss, and it is difficult to enhance quality factor.

[0006] Furthermore, in accordance with paper "Miniature 3D Inductors in Standard CMOS Process" submitted in April, 2002 by C.-C. Tang et al., an inductor is designed into a 3D type by using a multilevel metal interconnection structure, such that its occupied area can be reduced. The disadvantage is that the multilevel structure causes a larger parasitic capacitance, resulting in lower frequency bandwidth (it is difficult to be increased to more than 10 GHz). Moreover, in paper "Differentially Driven Symmetric Microstrip Inductors" submitted in January, 2002 by Danesh et al., it is discussed that if a microstrip line is used differentially, quality factor can be greatly increased. However, the disadvantage is that it cannot reduce the occupied area.

SUMMARY OF THE INVENTION

[0007] In the views of the above, an object of the present invention is to provide a miniature inductor suitable for integrated circuits. The miniature inductor can reduce the area occupied by the inductor and efficiently decreases costs for high-frequency integrated circuits. Meanwhile, it can alleviate the quality factor degradation caused by the inductor on substrate loss.

[0008] In order to achieve this object, the present invention provides a miniature inductor suitable for integrated circuits fabrication. The miniature inductor comprises: a semiconductor substrate having a coplanar strip line, a plurality of metal lines, a plurality of metal-insulator-metal (MIM) capacitors **1**, wherein the plurality of metal lines are formed on a surface of the semiconductor substrate, and the plurality of MIM capacitors are connected between the transmission lines of the coplanar strip line in parallel.

[0009] According to a preferred embodiment of the present invention, the miniature inductor has two kinds of folded structures: one is a crossed planar strip line structure **6**; and the other is a shifted planar strip line structure **8**. The crossed planar strip line structure **6** has a shape in which the coplanar strip line is crossed and inverted at its central portion. The shifted planar strip line structure **8** has a shape in which a portion of the coplanar strip line is shifted and inverted.

[0010] The present invention further provides a method for manufacturing a miniature inductor suitable for integrated circuits. The method comprises the following steps: providing a semiconductor substrate; forming a coplanar strip line on the semiconductor substrate; connecting a plurality of MIM capacitors **1** between the transmission lines of the coplanar strip line; crossing the coplanar strip line at its central portion; and inverting the crossed coplanar strip line.

[0011] The present invention additionally provides a method for manufacturing a miniature inductor suitable for integrated circuits. The method comprises the following steps: providing a semiconductor substrate; forming a coplanar strip line on the semiconductor substrate; connecting a plurality of MIM capacitors **1** between the transmission lines of the coplanar strip line; shifting a portion of the coplanar strip line; and inverting the shifted coplanar strip line.

[0012] In summary, the present invention applies transmission line theory to add MIM capacitors **1** into a terminal short-circuited coplanar strip line **3** so as to increase slow-wave factor. With the addition of crossing or shifting plus inverting methods, the area occupied by the manufactured miniature inductor can be reduced. Since the design architecture of the present invention employs a planar architecture, it has a smaller parasitic capacitance and is suitable for high-frequency bandwidth.

[0013] The above and other objectives, features and advantages of the present invention will become more clearly understood from the detailed descriptions given hereinafter and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] **FIG. 1** is a drawing showing a single-stub impedance matching method;

[0015] **FIG. 2** is a drawing showing a coplanar strip line (CPS) added with MIM capacitors according to a preferred embodiment;

[0016] **FIGS. 3***a*~**3***d* are drawings showing a tape-out inductor structure according to a preferred embodiment of the present invention;

[0017] **FIGS. 4***a*~**4***d* are drawings showing a tape-out inductor structure according to a preferred embodiment of the present invention;

[0018] **FIG. 5***a* is a drawing showing an equivalent model of a crossed and inverted CPS according to a preferred embodiment of the present invention;

[0019] **FIG. 5***b* is a drawing showing an equivalent model of a shifted and inverted CPS according to a preferred embodiment of the present invention.

[0020] **FIGS. 6***a* and **6***b* are drawings showing two kinds of folding structures according to a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] **FIG. 1** is a drawing showing a single-stub impedance matching method. As shown **FIG. 1**, when the terminal of a transmission line is short-circuited, it can be used as an inductive component. Its input impedance can be expressed as Equation (1). After expanding and arranging Equation (1), the real and imaginary parts of the input impedance can be obtained, and Equation (2) can be further derived.

$$Z_{in} = Z_o \cdot \tanh(\gamma l) = (R + jX) \cdot \tanh((\alpha + \beta j)l) \quad \text{Equation (1)}$$

$$Q = \frac{\frac{\sin 2\beta l}{\sinh 2\alpha l} + \frac{X}{R}}{1 - \frac{X}{R}\frac{\sin 2\beta l}{\sinh 2\alpha l}} \quad \text{Equation (2)}$$

[0022] As shown on the following Equation (3), under a specific characteristic impedance R, if it is intended to reduce the length of the transmission line, a larger β value must be used. Furthermore, we lean from Equation (4) that our goal can be achieved by increasing inductance or capacitance value per unit length

$$L_{eff} = R \tan(\beta l)/\omega \quad \text{Equation (3)}$$

$$\beta = \omega\sqrt{LC} \quad \text{Equation (4)}$$

[0023] **FIG. 2** is a drawing showing a coplanar strip line (CPS) added with MIM capacitors **1** according to a preferred embodiment. Please referring to **FIG. 2**, the used length can be efficiently reduced by increasing the β value according to the concept of high slow-wave factor CPS (HS-CPS) **2**. That is, the area becomes smaller. However, since the characteristic impedance is also reduced, the effect of reduced length depends on the rising rate of the tangent function. When a larger β value is used, since the rising rate of the function is faster, a shorter length can be adopted. As to the Q value of the inductor, we can see from Equation (2) that the smaller the α value of the inductor is, the Q value will become much better. Energy loss is mainly caused by substrate loss and conductor loss. Besides the self differential excitation characteristic of the CPS makes the substrate loss reduced, the MIM capacitors **1** located between the transmission lines of the CPS can further concentrate electric field, and thus reduce the coupling in the silicon substrate, which will lower the loss to the lowest level. For the problem of metal loss, it can be resolved by connecting two layers of metal lines in parallel in manufacturing process.

[0024] Since the length of the designed CPS can reach up to several hundreds μm, the present invention makes the CPS folded. According to the present invention, there are two kinds of folded structures. The first kind is a crossed planar strip line structure **6**, as shown in the drawing of **FIGS. 3***a*~**3***d* illustrating a tape-out inductor structure according to a preferred embodiment of the present invention. First, **FIG. 3***a* depicts a structural view of a terminal short-circuited coplanar strip line **3**. Next, a plurality of MIM capacitors **1** are connected between the transmission lines of the coplanar strip line in parallel to form a terminal short-circuited high slow-wave factor CPS **4**, shown in **FIG. 3***b*. Then, the coplanar strip line connected with the plurality of MIM capacitors **1** is crossed at its central portion. That is a crossed high slow-wave factor CPS **5**, shown in **FIG. 3***c*. Finally, as illustrated in **FIG. 3***d*, crossed high slow-wave factor CPS **5** is inverted.

[0025] In another preferred embodiment of the present invention, the other kind of folded structure is adopted, that is, a shifted planar strip line structure **8**. As shown in **FIGS. 4***a*~**4***d*, the difference to the above-stated embodiment is that a portion of coplanar strip lines connected with the plurality of MIM capacitors **1** are shifted. That is a shifted high slow-wave factor CPS **7**, shown in **FIG. 4***c*. Subsequently, as depicted in **FIG. 4***d*, the shifted high slow-wave factor CPS **7** are inverted.

[0026] The above-stated two kinds of folding methods not only reduce half occupied area due to folding, but also increase inductance value per unit length due to the mutual inductance between the two transmission lines. As a result, the β value and characteristic impedance are increased as well. This will facilitate the reduction of the total length of the CPS.

[0027] In a preferred embodiment of the present invention, it is to enable a 1 nH inductor operating at about 10 GHz, and the total length of the inductor is less than 200 μm. Herein, taking a 1 nH inductor as an example, first, in step a, when let β**1**=40°, l=400 μm, the required P and characteristic impedance R are 1.8 (rad/mm) and 75 ohm, respectively. Next, in step b, it can be derived by electromagnetic simulation software and hand calculation analysis that: when the MIM capacitors each having 16 fF per unit are spaced 64 μm apart, the required β can be substantially obtained. Finally, in step c, the pitch and width of the metal lines are adjusted to make the characteristic impedance meet with the design requirement and have a 1 nH inductance at 10 GHz.

[0028] **FIG. 5***a* is a drawing showing an equivalent model of a crossed and inverted CPS according to a preferred embodiment of the present invention. Please referring to **FIG. 5***a*, it is noted that there are two transmission lines per unit length to pass due to folded CPS. When taking the first folding method (that is, the crossed planar strip line structure **6**) into consideration, we see that two transmission lines having different characteristic impedance Z_1 and Z_2 and the same lengths L are connected to each other. Finally, the two transmission lines are equivalent to one transmission line having a characteristic impedance Z_3 and a length 2 L. The equivalent Z**3** and γ**3** can be obtained by using electromagnetic simulation software in order to design the inductor with the above-stated equations.

[0029] **FIG. 5***b* is a drawing showing an equivalent model of a shifted and inverted CPS according to a preferred embodiment of the present invention. Referring to **FIG. 5***b*, when taking the second folding method (that is, the shifted planar strip line structure **8**) into consideration, since two transmission lines have the same characteristic impedance Z_1', they can be equivalent to a transmission line having a characteristic impedance Z_3' and a length 2 L.

[0030] Two kinds of structures according to a preferred embodiment of the present invention are shown in **FIGS. 6***a* and **6***b*. MIM capacitors **1** are connected to two peripheral metal lines via sixth metal line **9**. If MIM capacitors **1** need to be connected to the outmost metal lines, it is necessary to use fourth metal line **11** in order to cross the parallel-connected sixth and fifth metal lines **10**.

[0031] In a preferred embodiment of the present invention, an efficiency comparison between the two kinds of structures is made. The same specifications are set as 8 μm in metal line width, 2 μm in metal line pitch and simulation starting in a case that M6 and M5 are connected in parallel.

[0032] First kind of structure Symmetric (differential excitation): no capacitors are added, that is, the regular symmetric inductor; and second kind of structure MiM_S64 μm: MIM capacitors **1** are added inside an inductor and spaced 64 μm apart.

[0033] The result shows that under the same inductance value, as compared to the first structural inductor having no MIM capacitors added, the second structural inductor can reduce about more 15% in area. Furthermore, Qmax occurring at around 10 GHz means that Qmax can also be adjusted by using this structure so as to make the inductor more efficient.

[0034] Although the invention has been disclosed in terms of preferred embodiments, the disclosure is not intended to limit the invention. Those skilled in the art can make changes and modifications still within the scope and spirit of the invention which will be defined by the claims below.

LIST OF MAJOR ELEMENTS AND THEIR CORRESPONDING REFERENCE NUMERALS

[0035] **1** metal-insulator-metal (MIM) capacitors

[0036] **2** high slow-wave factor CPS

[0037] **3** terminal short-circuited coplanar strip line

[0038] **4** terminal short-circuited high slow-wave factor CPS

[0039] **5** crossed high slow-wave factor CPS

[0040] **6** crossed planar strip line structure

[0041] **7** shifted high slow-wave factor CPS

[0042] **8** shifted planar strip line structure

[0043] **9** sixth metal line

[0044] **10** sixth and fifth metal lines

[0045] **11** fourth metal line

[0046] L Length

[0047] 2 L Length

[0048] Z_1 characteristic impedance

[0049] Z_1' characteristic impedance

[0050] Z_2 characteristic impedance

[0051] Z_3 characteristic impedance

[0052] Z_3' characteristic impedance

1. A miniature inductor suitable for integrated circuits, comprising:

a semiconductor substrate having a coplanar strip line; and

a plurality of metal-insulator-metal (MIM) capacitors being connected between the transmission lines of the coplanar strip line in parallel;

wherein the coplanar strip line connected with the MIM capacitors further comprises a crossed planar strip line structure or a shifted planar strip line structure.

2. The miniature inductor as claimed in claim 1, wherein the crossed planar strip line structure has a shape in which the coplanar strip line is crossed and inverted at its central portion.

3. The miniature inductor as claimed in claim 1, wherein the shifted planar strip line structure has a shape in which a portion of the coplanar strip line is shifted and inverted.

4. The miniature inductor as claimed in claim 1, wherein the terminals of the coplanar strip line are short-circuited.

5. The miniature inductor as claimed in claim 1, wherein the area of metal loss is the connection portion of the coplanar metal strip lines in parallel.

6. The miniature inductor as claimed in claim 5, wherein the miniature inductor is manufactured by an integrated circuit silicon process.

7. A method for manufacturing a miniature inductor suitable for integrated circuits, which comprise the steps of:

providing a semiconductor substrate;

forming a coplanar strip line on the semiconductor substrate;

connecting a plurality of MIM capacitors between the transmission lines of the coplanar strip line; and

forming a shape in which the coplanar strip line is crossed and inverted at its central portion.

8. The method as claimed in claim 7, wherein the terminals of the coplanar strip line are short-circuited.

9. The method as claimed in claim 7, wherein the area of metal loss is the connection portion of the coplanar metal strip lines in parallel.

10. The method as claimed in claim 7, wherein the miniature inductor is manufactured by an integrated circuit silicon process.

11. A method for manufacturing a miniature inductor suitable for integrated circuits, which comprises the following steps:

providing a semiconductor substrate;

forming a coplanar strip line on the semiconductor substrate;

connecting a plurality of MIM capacitors between the transmission lines of the coplanar strip line;

forming a shape in which a portion of the coplanar strip line is shifted and inverted.

12. The method as claimed in claim 11, wherein the terminals of the coplanar strip line are short-circuited.

13. The method as claimed in claim 11, wherein the area of metal loss is the connection portion of the coplanar strips line in parallel.

14. The method as claimed in claim 11, wherein the miniature inductor is manufactured by an integrated circuit silicon process.

* * * * *