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(54) **SILICON CONTROLLED RECTIFIER FOR THE ELECTROSTATIC DISCHARGE PROTECTION**

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(52) **U.S. Cl.** **361/56**

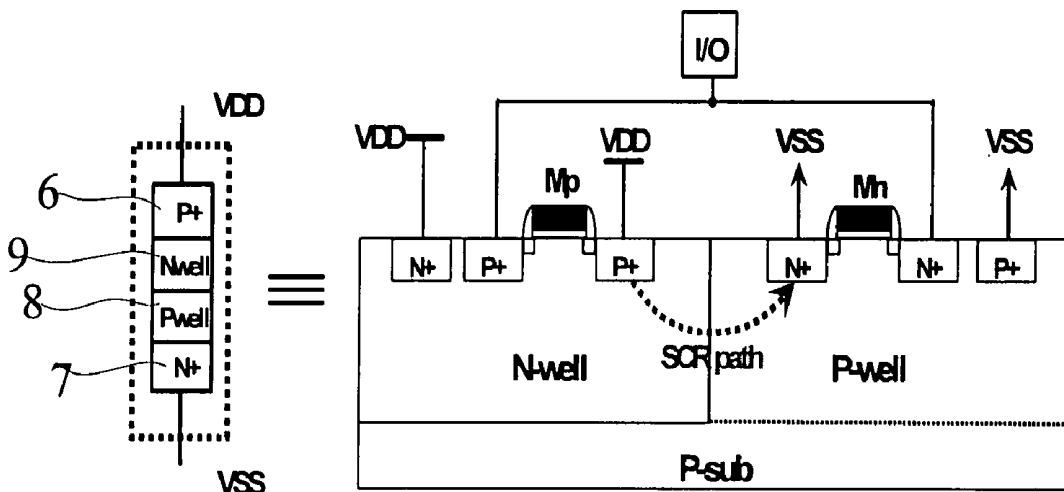
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(57) **ABSTRACT**

The present invention relates to an SCR (Silicon Controlled Rectifier) for the ESD (electrostatic discharge) protection comprising two terminal electrodes of a first electrode and a second electrode, a PMOS, an NMOS and an SCR structure. By utilizing an embedded SCR, a whole-chip ESD protection circuit design can be obtained. The present invention is suitable for IC products, and for applications by IC design industries and IC foundry industries.

(73) Assignee: **National Chiao Tung University**

(21) Appl. No.: **10/857,836**



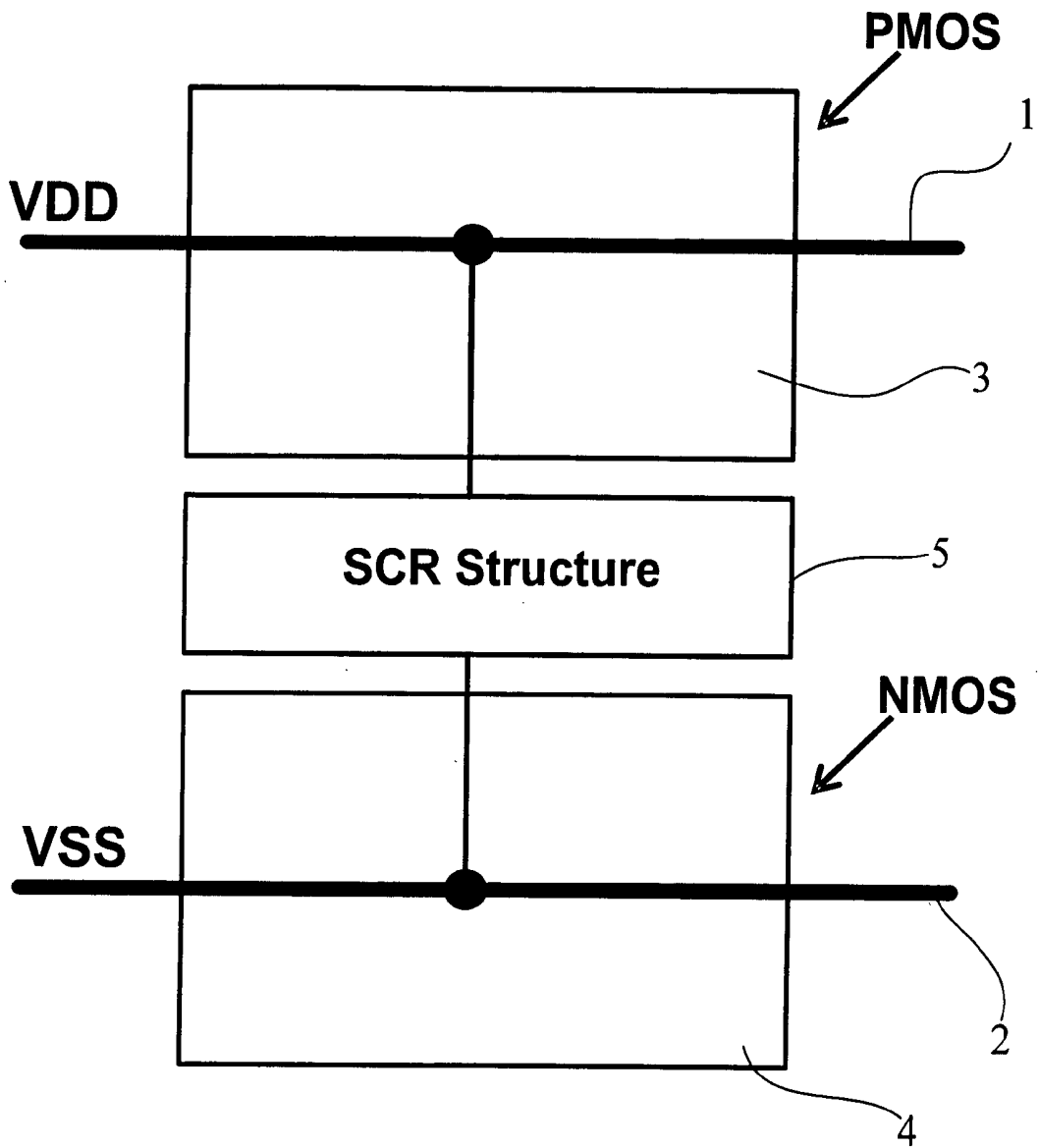


FIG.1

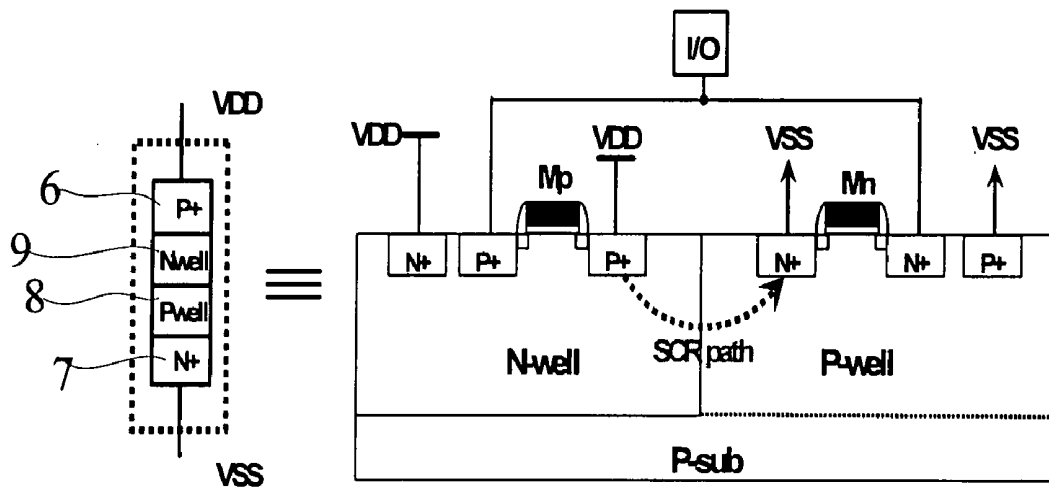


FIG.2

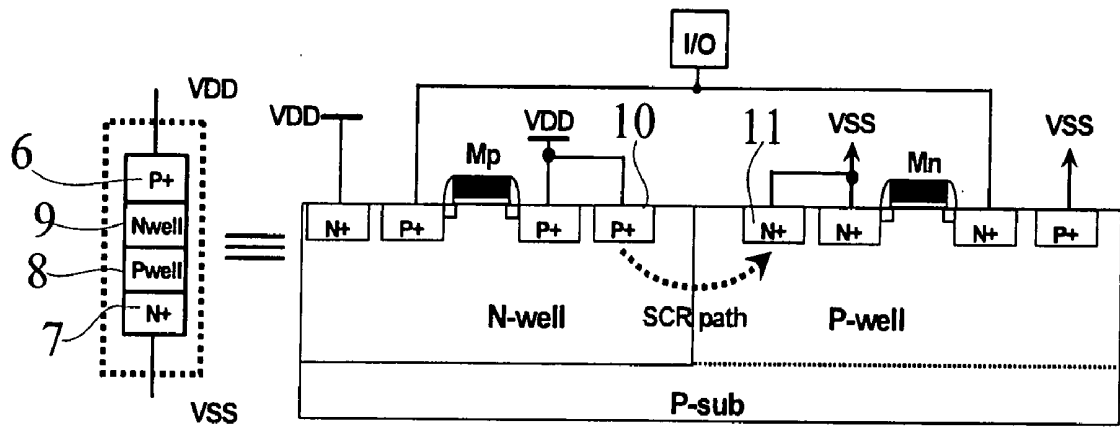


FIG.3

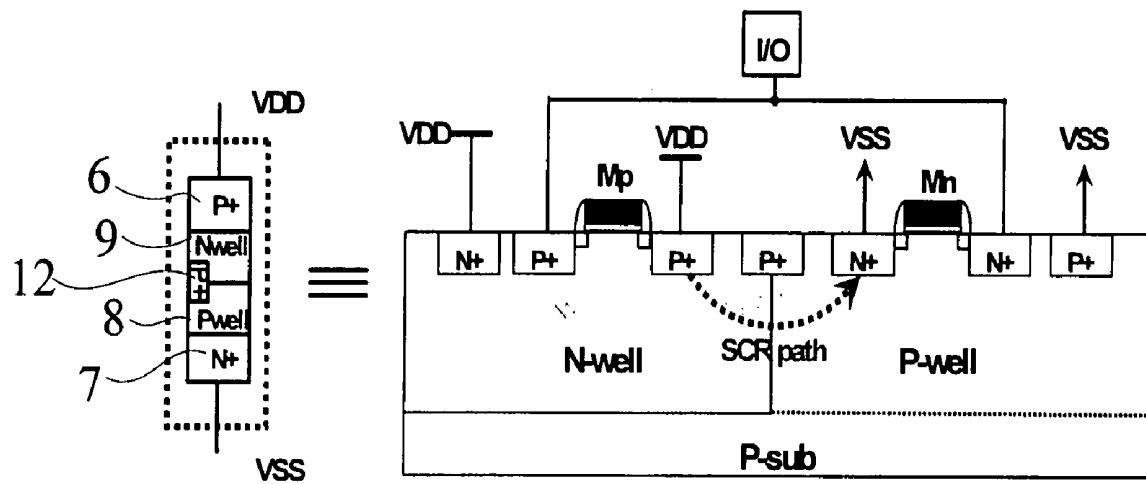


FIG.4

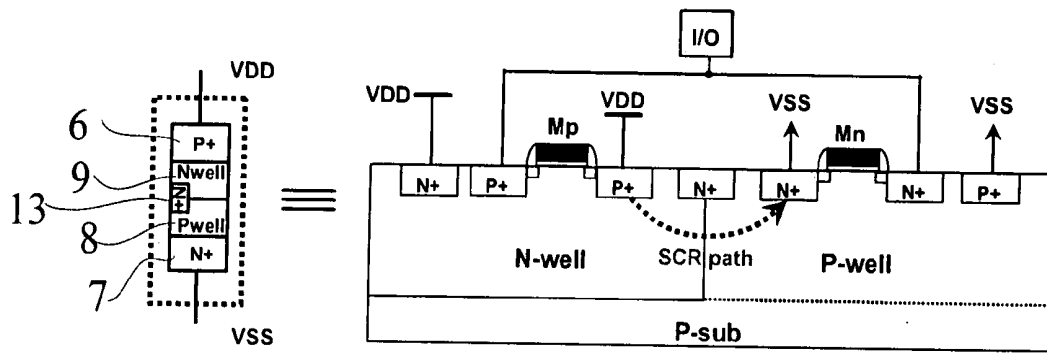


FIG.5

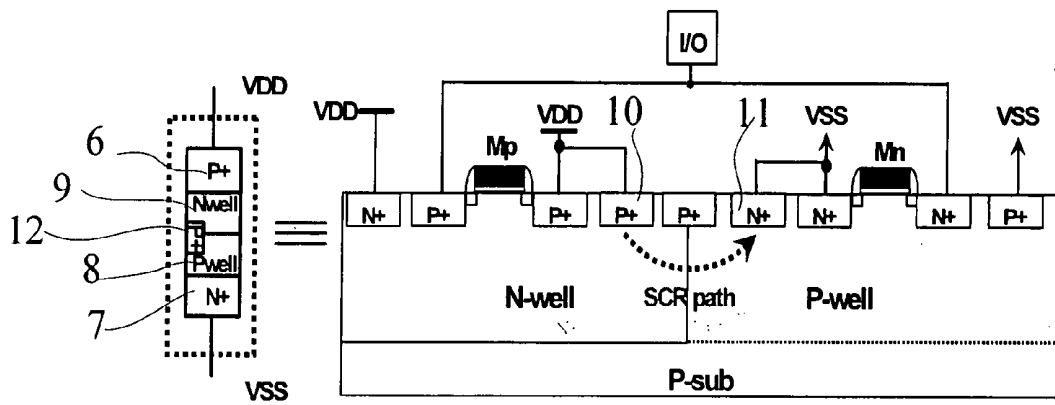


FIG.6

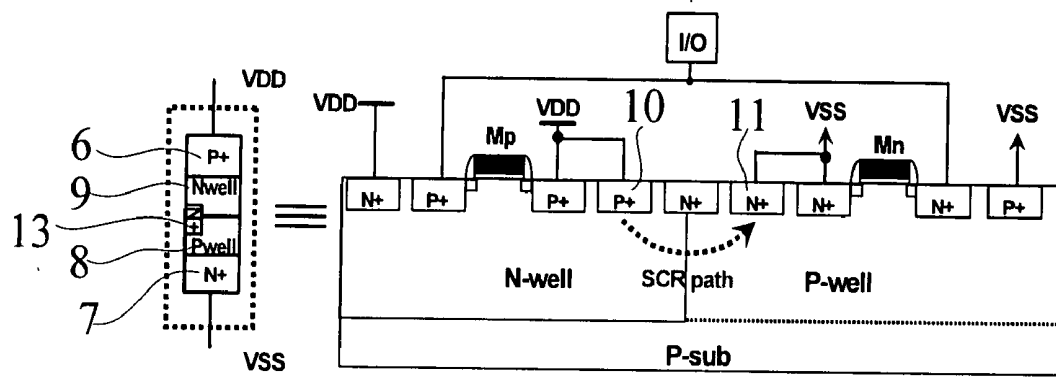


FIG. 7

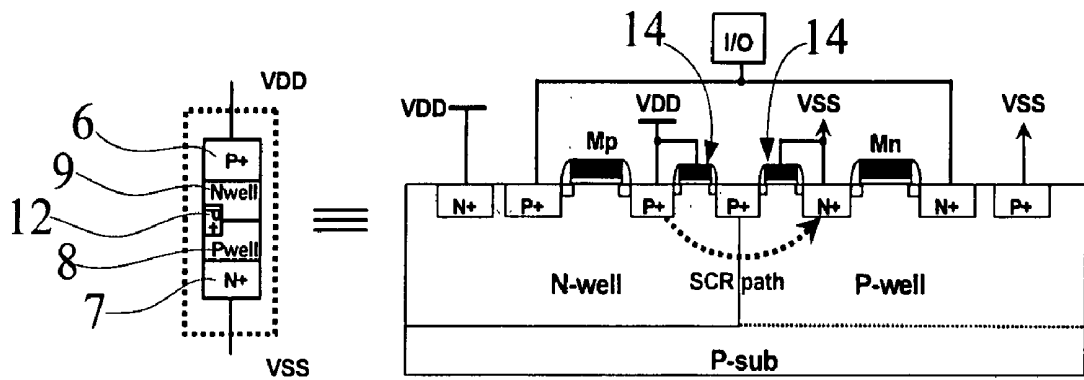


FIG.8

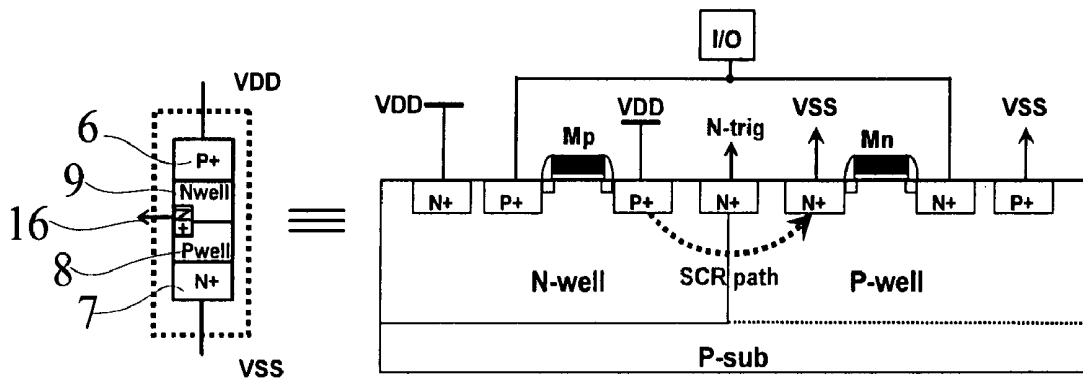


FIG.11

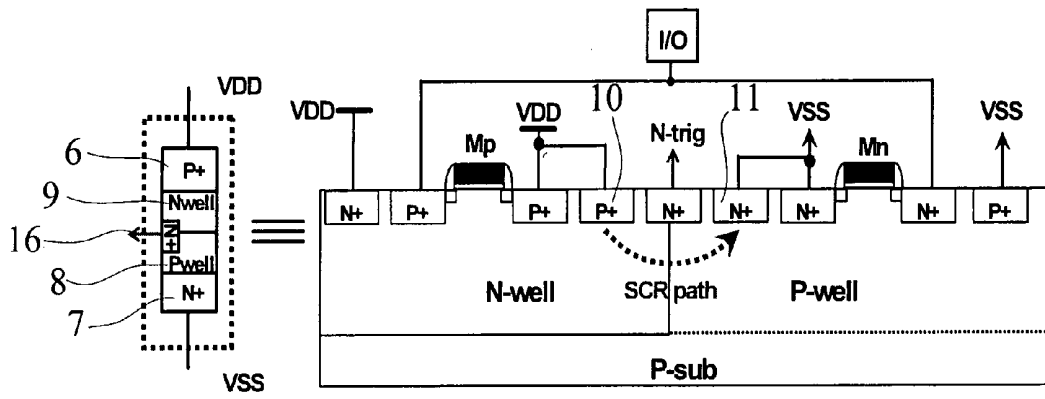


FIG.13

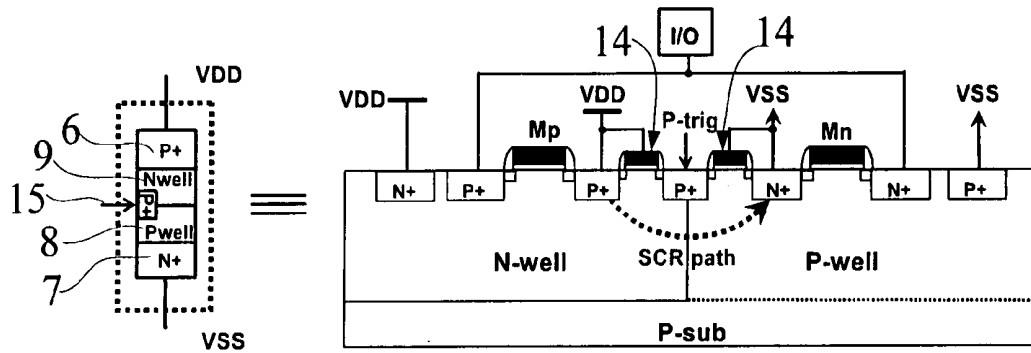


FIG.14

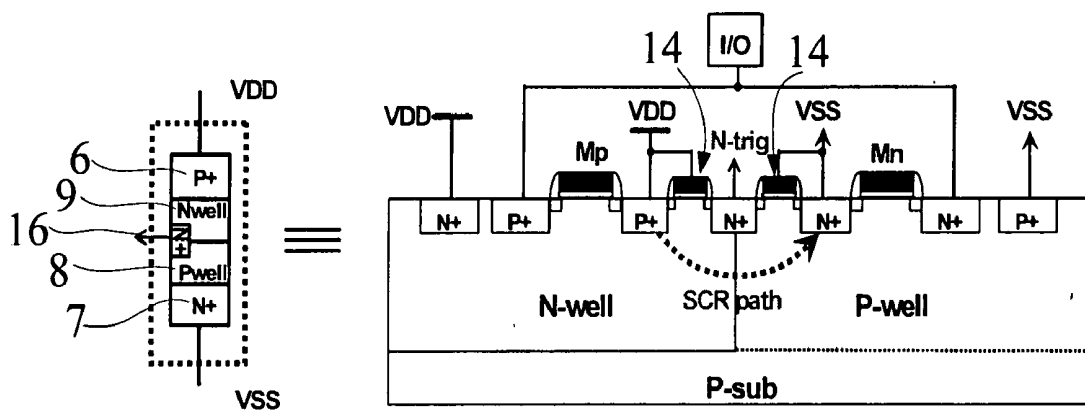


FIG. 15

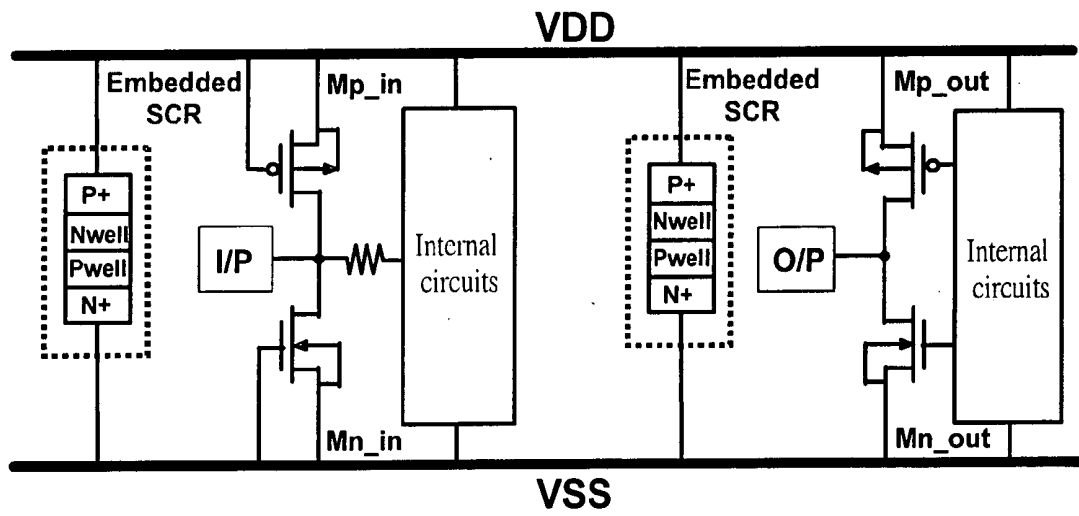


FIG.16

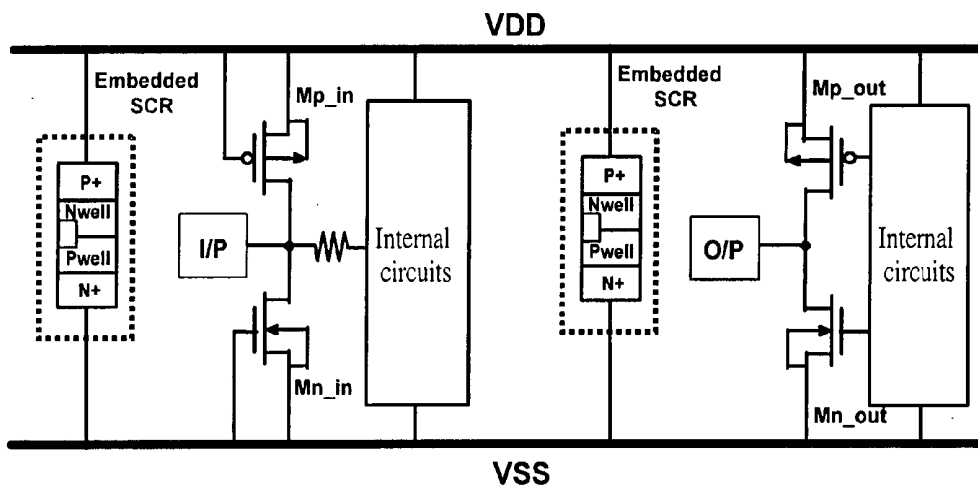


FIG.17

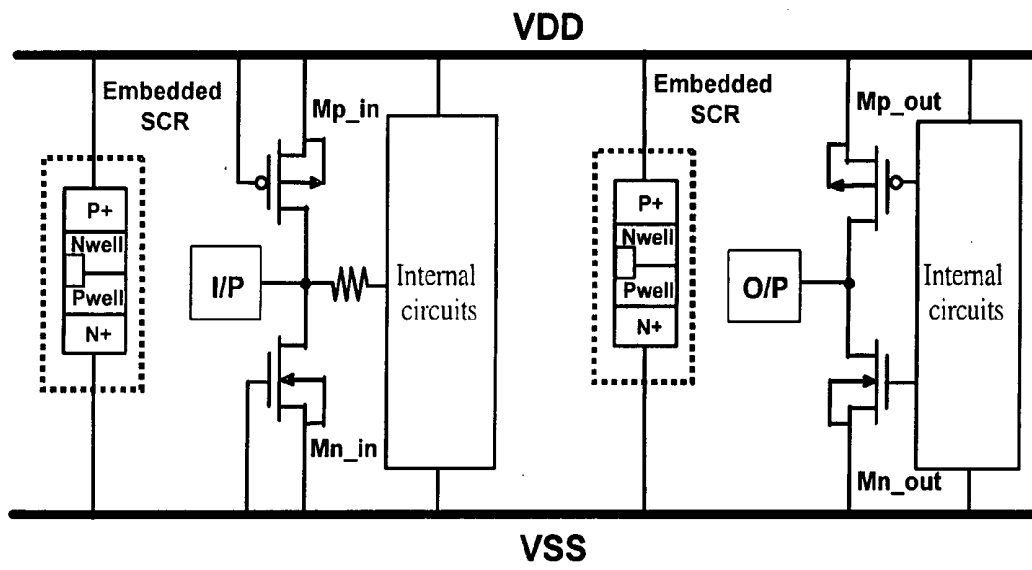


FIG.18

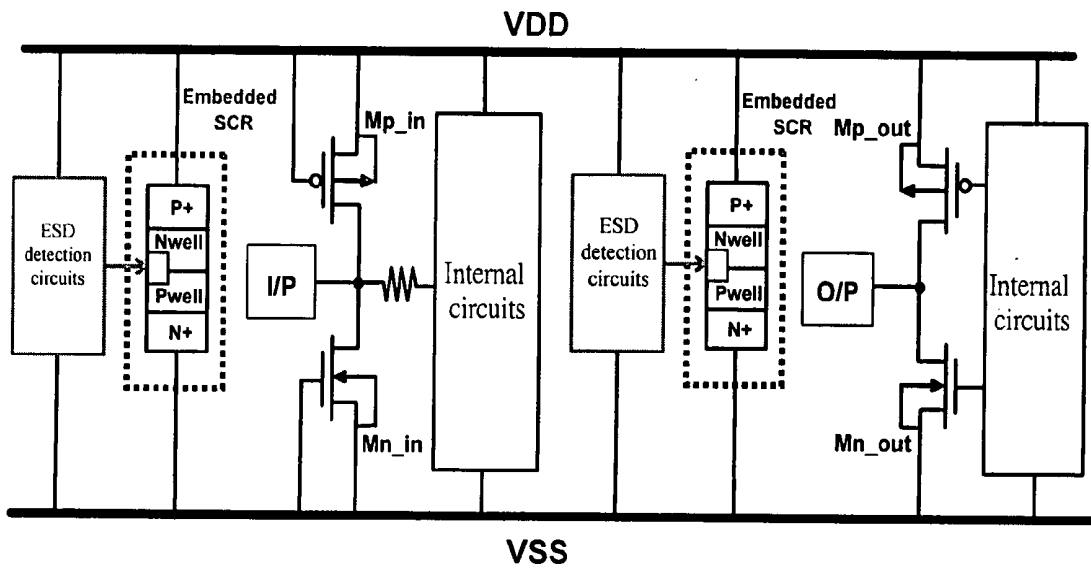


FIG.19

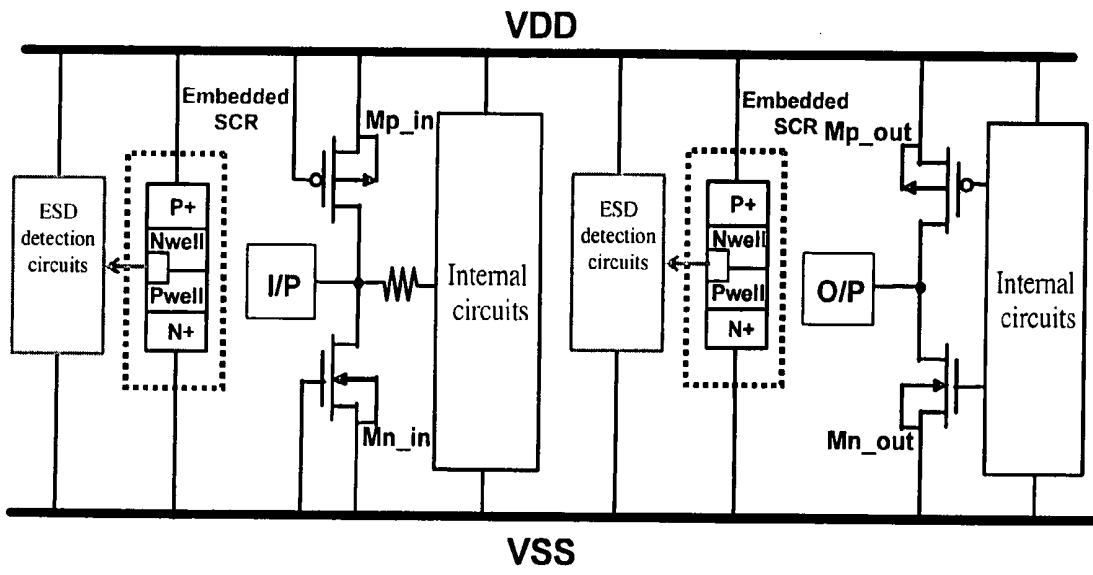


FIG.20

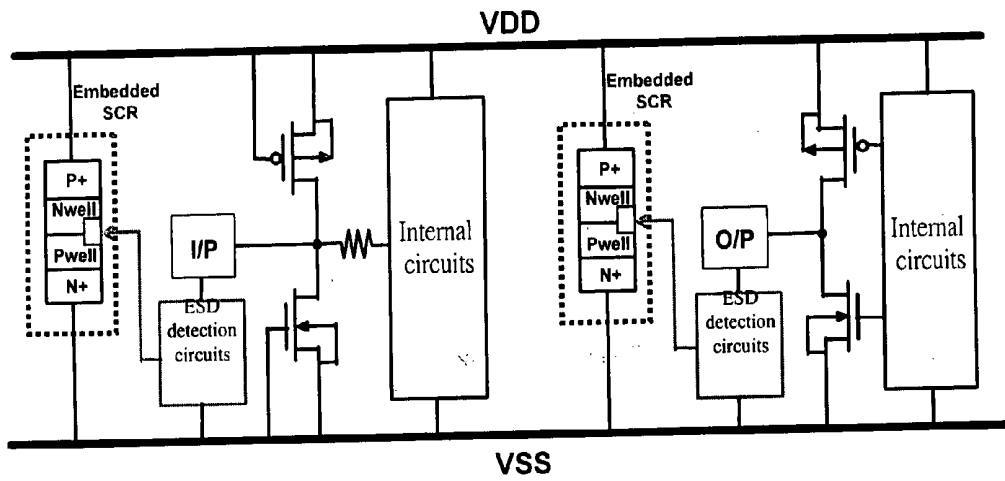


FIG.21

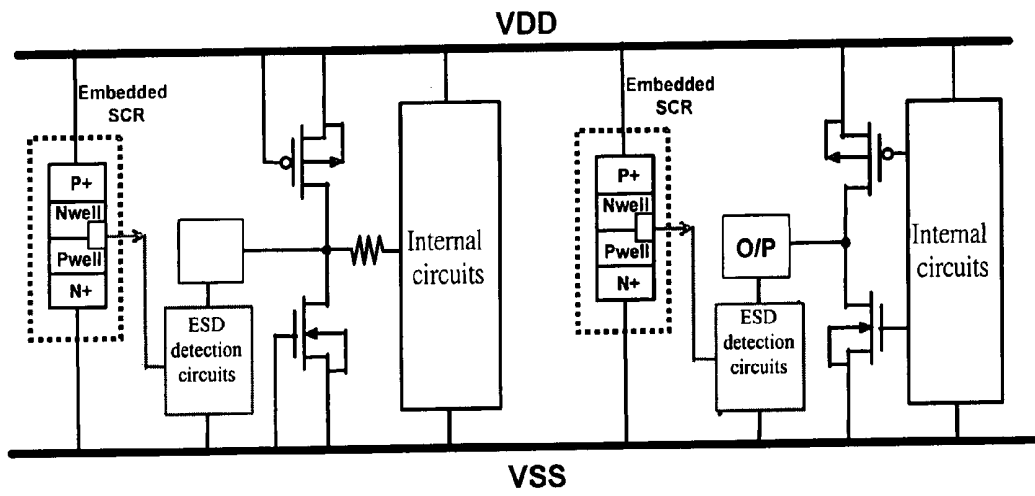


FIG.22

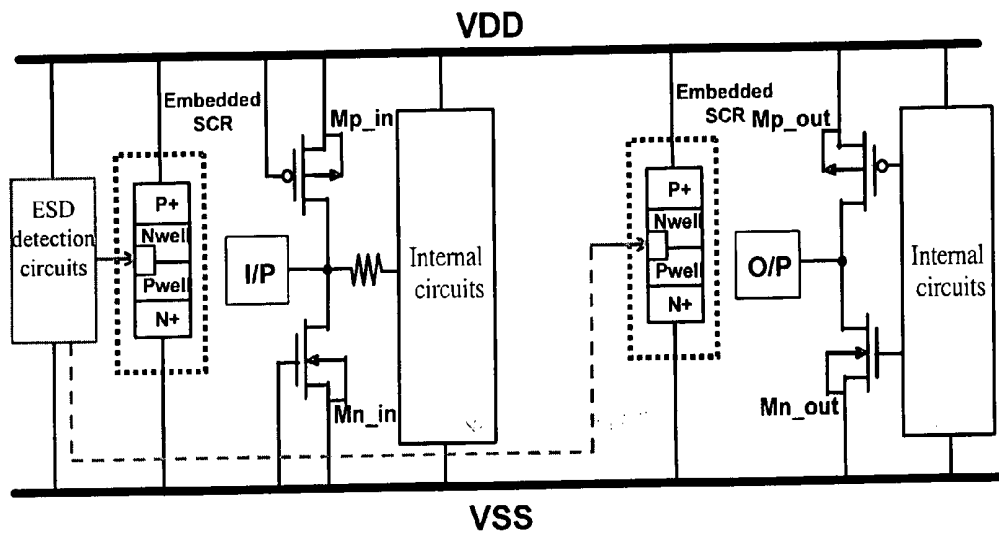


FIG.23

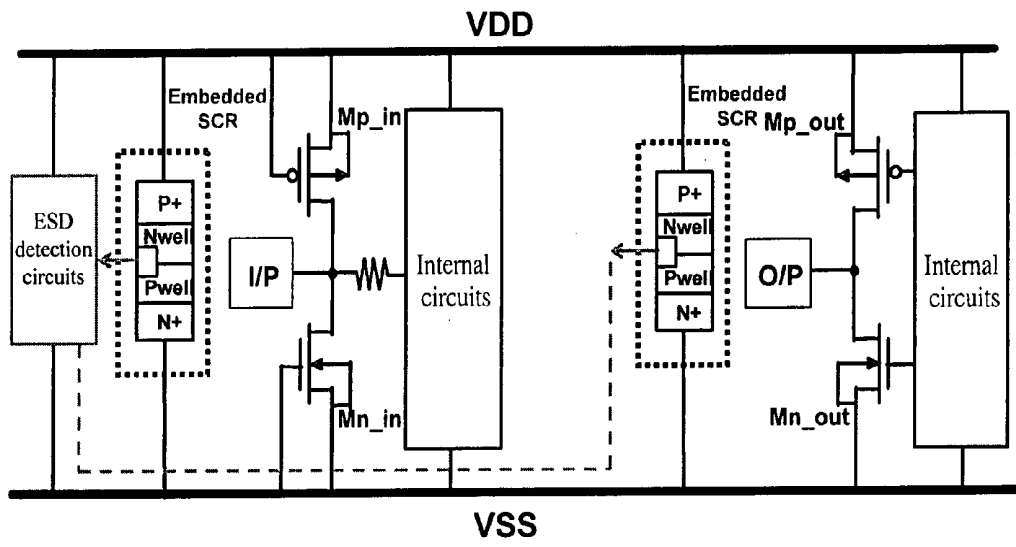


FIG.24

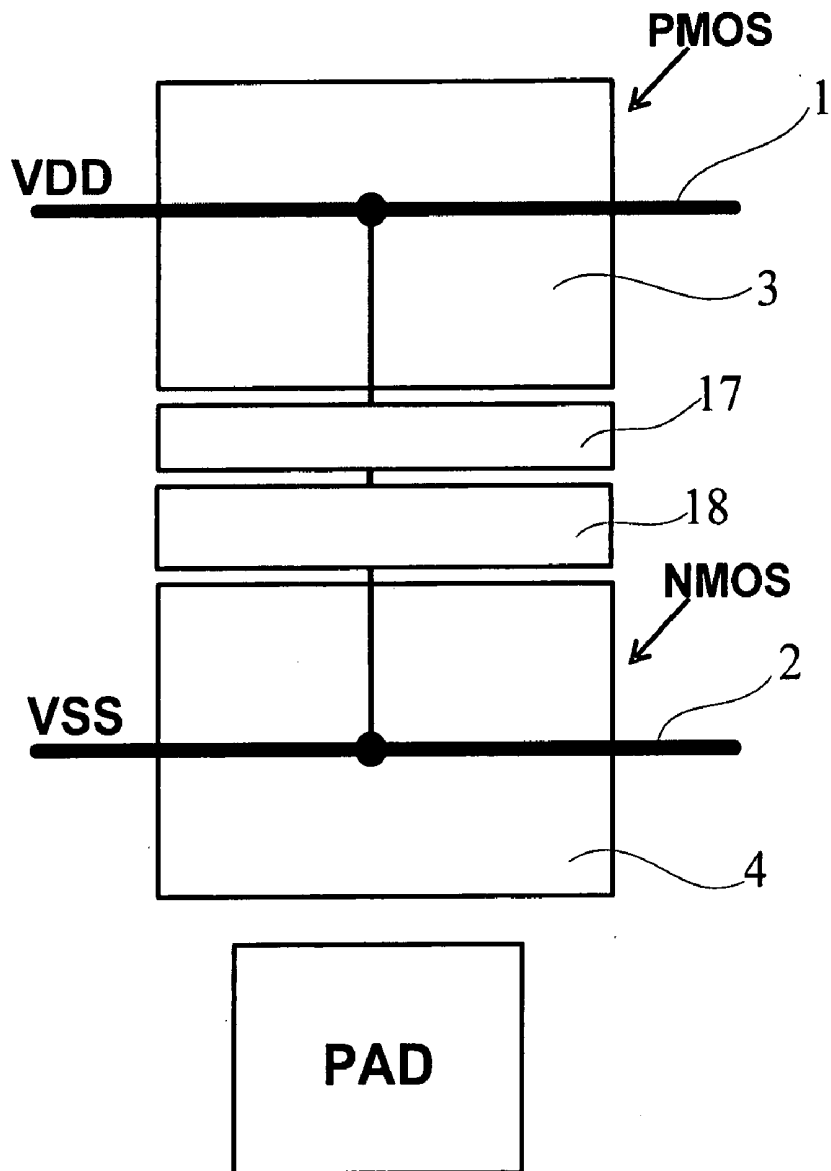


FIG.25

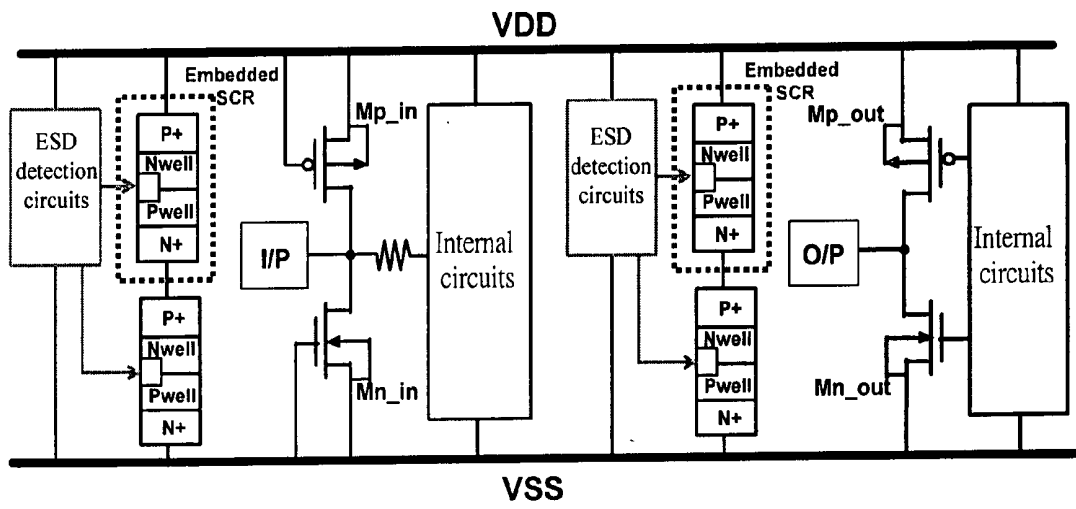


FIG.26

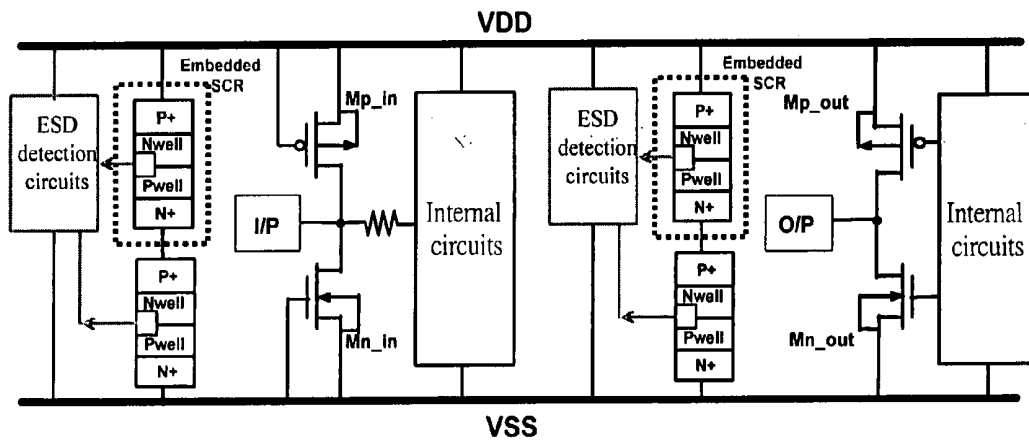


FIG.27

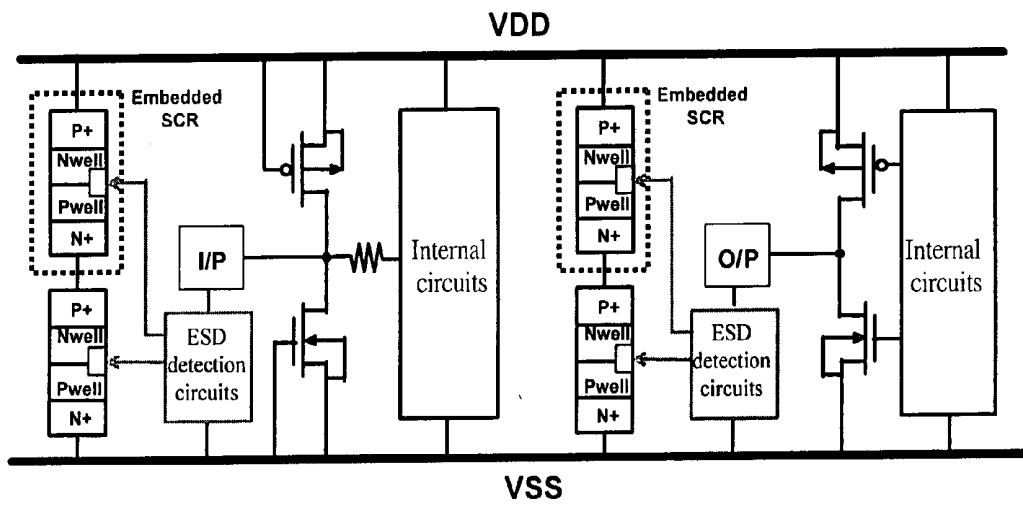


FIG.28

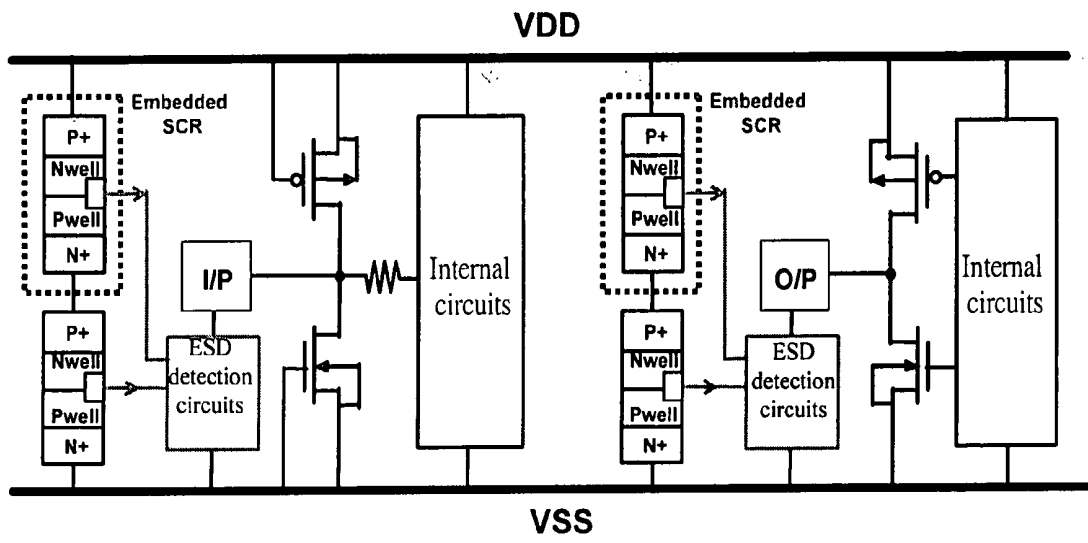


FIG.29

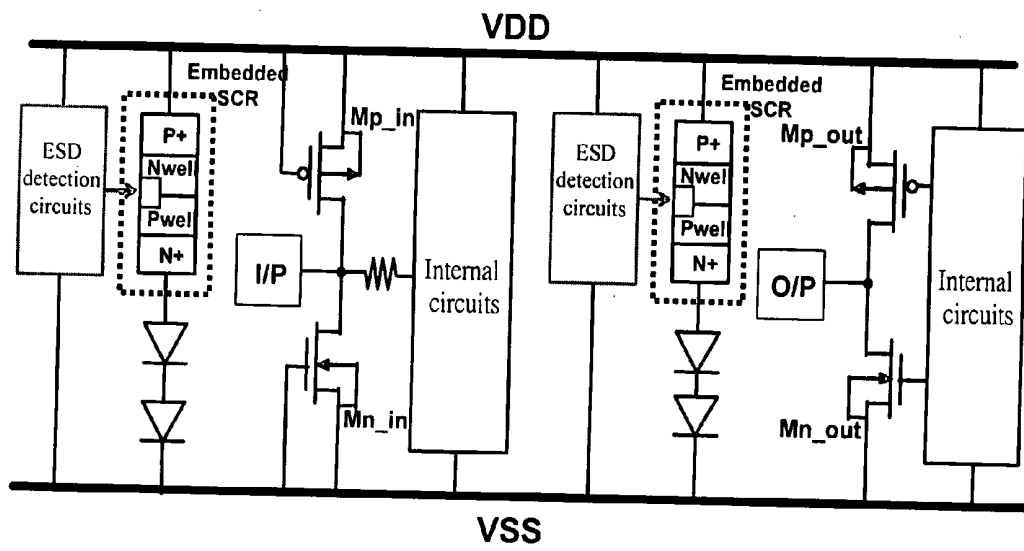


FIG.30

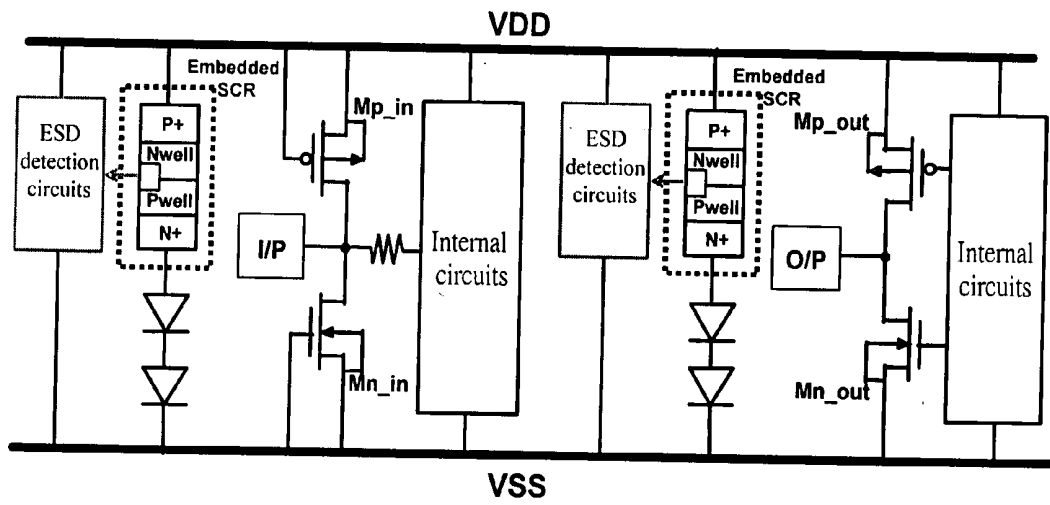


FIG.31

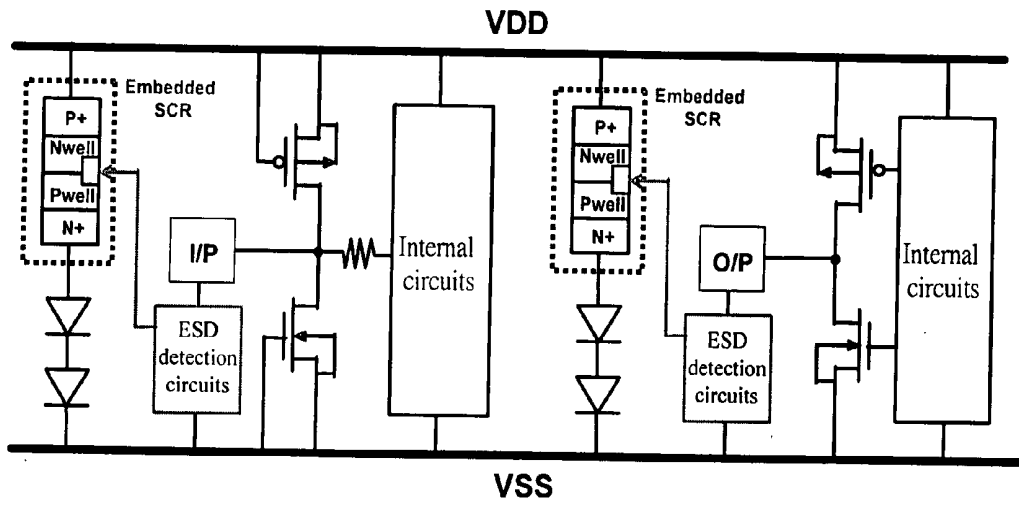


FIG.32

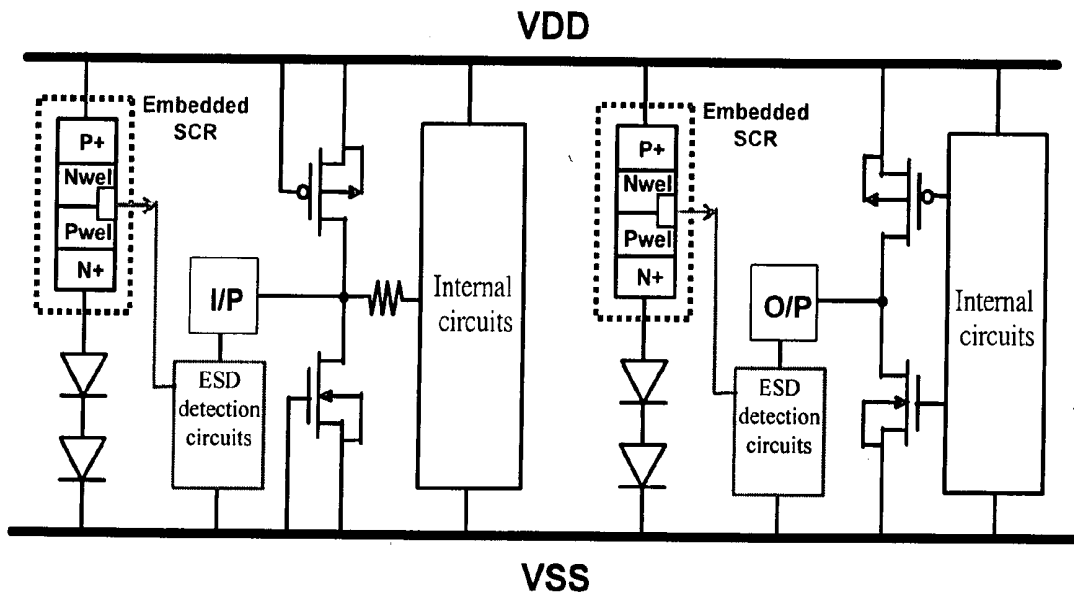


FIG.33

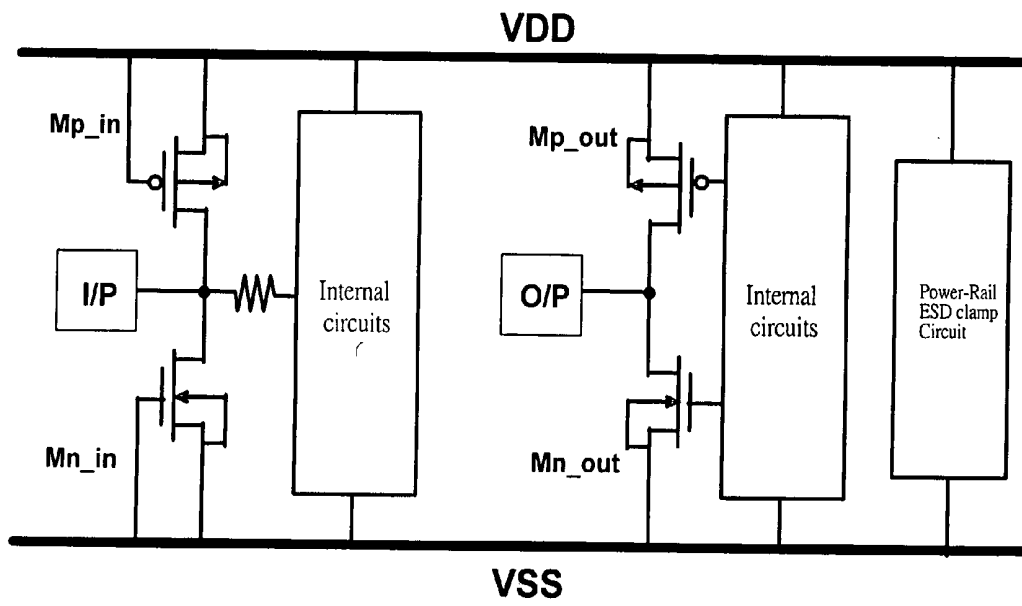


FIG.34

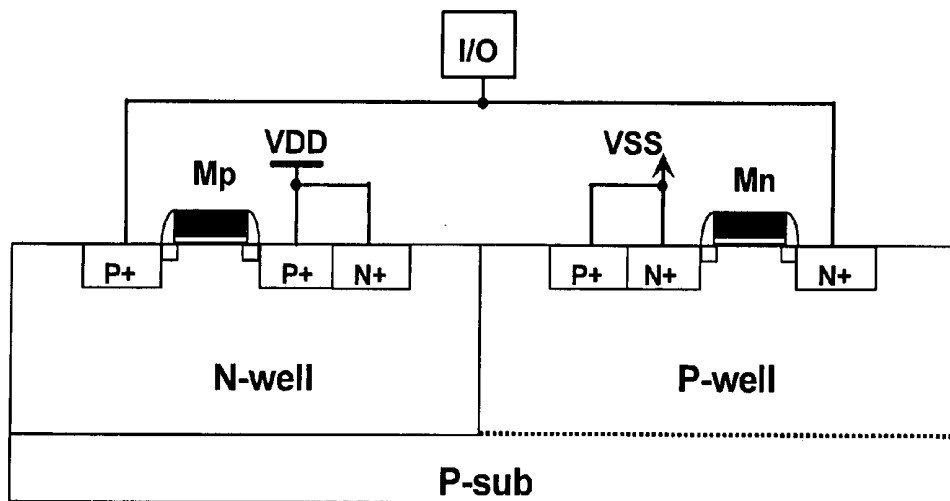


FIG.35 (a)

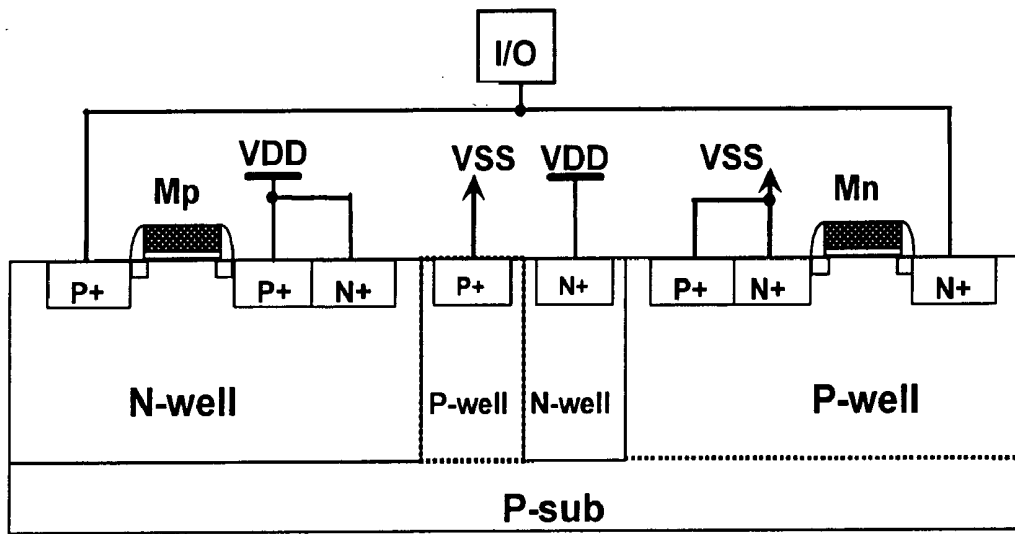


FIG.35 (b)

SILICON CONTROLLED RECTIFIER FOR THE ELECTROSTATIC DISCHARGE PROTECTION

FIELD OF THE INVENTION

[0001] The present invention relates to a silicon controlled rectifier (SCR) for the electrostatic discharge (ESD) protection. More particularly, the present invention relates to a device which utilizes embedded SCR as ESD protection device in order to achieve whole-chip ESD protection circuit design.

DESCRIPTION OF THE RELATED ART

[0002] With references to FIG. 34, FIG. 35(a) and FIG. 35(b) which are views showing related conventional techniques. FIG. 34 is a view showing an ESD protection design for Complementary Metal Oxide Semiconductor (CMOS) integrated circuit (IC) of a conventional art. FIG. 35(a) is a view showing an ESD protection device of a conventional art having a single guard ring structure inserted between the PMOS and NMOS of I/O buffers while FIG. 35(b) is a view showing an ESD protection device of a conventional art having double guard ring structures inserted between the PMOS and NMOS of I/O buffers.

[0003] In the above on-chip ESD protection, the ESD protection devices are formed by PMOS and NMOS devices connected to the VDD and VSS power lines, respectively. To avoid unexpected ESD damage in the internal circuits of CMOS ICs, the power-rail ESD clamp circuit was added between VDD and VSS power lines. Whole-chip ESD protection design of a CMOS IC can be achieved by the ESD protection devices at the I/O pads cooperating with the power-rail ESD clamp circuit. However, the ESD robustness of the whole chip is strongly dependent on the space between the I/O pad and power-rail ESD clamp circuit. In addition, extra layout area is needed to implement the power-rail ESD clamp circuit.

[0004] In CMOS technology, the SCR device has been commonly used for on-chip ESD protection. Comparing the SCR device to the other ESD protection devices such as diode, MOS, BJT, or field-oxide device which are used in the CMOS integrated circuit, the SCR device in the on-chip ESD protection circuit can sustain much higher ESD voltage within a smaller layout area due to the low holding voltage ($\sim -1V$) of the SCR device. On the other hand, while the IC is in a normal operating condition, the SCR device is susceptible to latch-up issue because the SCR device may be accidentally triggered on by the external noise pulses due to the holding voltage of the SCR device with smaller voltage than that of the power supply. Thereby, the latch-up phenomenon often leads to IC function failure or even destruction. In order to safely apply the SCR device to the on-chip ESD protection, several methods are proposed to solve the latch-up issue.

[0005] Therefore, several articles of conventional techniques which are to solve the latch-up issue caused by applying SCR device to the on-chip ESD protection are proposed, as the followings are two examples.

[0006] In "Electrostatic discharge protection circuits with latch-up prevention function", U.S. Pat. No. 6,410,963, June 2002, by C. S. Lai et al., an ESD protection is disclosed which comprises an SCR device comprising at least a first

bipolar junction transistor and a second bipolar junction transistor; a first MOS between an interface terminal and the second bipolar junction transistor; and a second MOS between the emitter and the ground of the second bipolar junction transistor. The above device is presented for an ESD protection and the elimination of the latch-up issue.

[0007] In "Cascode LVTSCR and ESD protection circuit", U.S. Pat. No. 5,959,820, September 1999, by Ming-Dou Ker et al., an ESD protection is disclosed by using two or more SCRs, each comprising an anode, a control gate, and a cathode. By the device stated above, an efficient ESD protection and the elimination of the latch-up issue can be attained.

[0008] According to the above conventional techniques, however, with the scaled-down device dimension, the VDD supply voltage is also scaled down to meet the circuit performance requirement. The VDD supply voltage is only 1.2V with 0.13- μm CMOS technology. When the holding voltage of SCR device is higher than the VDD supply voltage, latch-up issue will not occur. Therefore, the extra design on SCR device for latch-up issue is not necessary.

[0009] Subsequently, in "A new design for complete on-chip ESD protection" by A. Z. Wang et al., on pp. 87-90 of Proc. of Custom Integrated Circuits Conf., 2000, the production process is modified by adding an N⁺ buried layer (NBL), and a much higher trigger voltage is required to turn on the SCR device for achieving an efficient ESD protection.

[0010] In the present invention, the embedded SCR structure formed between PMOS and NMOS of I/O buffers is to serve as a power-rail ESD clamp circuit. Therefore, a whole-chip ESD protection design can be achieved by each individual I/O cell without an extra power-rail ESD clamp circuit.

[0011] The present invention is fully compatible with general CMOS process without adding extra fabrication or mask. According to the present invention, the ESD robustness of the whole chip can be efficiently improved with a much smaller layout area.

SUMMARY OF THE INVENTION

[0012] The main purpose of the invention is to provide a whole-chip ESD protection design with SCR which can be implemented on a single I/O cell in CMOS IC.

[0013] Another purpose of the present invention is to provide ESD robustness for the whole chip which is efficiently improved within a much smaller layout area.

[0014] The third purpose of the present invention is to provide an SCR for the ESD protection that can be applied to a sub 0.13- μm CMOS IC product.

[0015] For the above purposes, the present invention relates to a circuit and a method which utilizes an embedded SCR to provide a whole-chip ESD protection design. The present invention relates to an SCR for the ESD protection which is comprised of a first electrode having high-potential power supply voltage such as VDD and a second electrode having low-potential power supply voltage such as VSS; a PMOS; an NMOS; and an SCR structure. According to the present invention, a whole-chip ESD protection design can be implemented on a single I/O cell without extra power-rail ESD clamp circuit. In addition, the ESD robustness of the

whole chip can be efficiently improved with a much smaller layout area. Therefore, the present invention is suitable for application for integrated circuit products.

BRIEF DESCRIPTION OF THE INVENTION

[0016] The present invention will be better understood from the following detailed description of preferred embodiments of the invention, taken in conjunction with the accompanying drawings, in which:

[0017] **FIG. 1** is a view showing the structure according to the present invention;

[0018] **FIG. 2** is a view showing a first embodiment according to the present invention;

[0019] **FIG. 3** is a view showing a second embodiment according to the present invention;

[0020] **FIG. 4** is a view showing a third embodiment according to the present invention;

[0021] **FIG. 5** is a view showing a fourth embodiment according to the present invention;

[0022] **FIG. 6** is a view showing a fifth embodiment according to the present invention;

[0023] **FIG. 7** is a view showing a sixth embodiment according to the present invention;

[0024] **FIG. 8** is a view showing a seventh embodiment according to the present invention;

[0025] **FIG. 9** is a view showing an eighth embodiment according to the present invention;

[0026] **FIG. 10** is a view showing a ninth embodiment according to the present invention;

[0027] **FIG. 11** is a view showing a tenth embodiment according to the present invention;

[0028] **FIG. 12** is a view showing an eleventh embodiment according to the present invention;

[0029] **FIG. 13** is a view showing a twelfth embodiment according to the present invention;

[0030] **FIG. 14** is a view showing a thirteenth embodiment according to the present invention;

[0031] **FIG. 15** is a view showing a fourteenth embodiment according to the present invention;

[0032] **FIG. 16** is a view showing a first embodiment of circuit according to the present invention;

[0033] **FIG. 17** is a view showing a second embodiment of circuit according to the present invention;

[0034] **FIG. 18** is a view showing a third embodiment of circuit according to the present invention;

[0035] **FIG. 19** is a view showing a fourth embodiment of circuit according to the present invention;

[0036] **FIG. 20** is a view showing a fifth embodiment of circuit according to the present invention;

[0037] **FIG. 21** is a view showing a sixth embodiment of circuit according to the present invention;

[0038] **FIG. 22** is a view showing a seventh embodiment of circuit according to the present invention;

[0039] **FIG. 23** is a view showing an eighth embodiment of circuit according to the present invention;

[0040] **FIG. 24** is a view showing a ninth embodiment of circuit according to the present invention;

[0041] **FIG. 25** is a view showing the structure of another embodiment according to the present invention;

[0042] **FIG. 26** is a view showing a tenth embodiment of circuit according to the present invention;

[0043] **FIG. 27** is a view showing an eleventh embodiment of circuit according to the present invention;

[0044] **FIG. 28** is a view showing a twelfth embodiment of circuit according to the present invention;

[0045] **FIG. 29** is a view showing a thirteenth embodiment of circuit according to the present invention;

[0046] **FIG. 30** is a view showing a fourteenth embodiment of circuit according to the present invention;

[0047] **FIG. 31** is a view showing a fifteenth embodiment of circuit according to the present invention;

[0048] **FIG. 32** is a view showing a sixteenth embodiment of circuit according to the present invention;

[0049] **FIG. 33** is a view showing a seventeenth embodiment of circuit according to the present invention;

[0050] **FIG. 34** is a view showing an ESD protection design for CMOS integrated circuit (IC) of a conventional art;

[0051] **FIG. 35(a)** is a view showing an ESD protection device having a single guard ring structure inserted between the PMOS and NMOS of I/O buffers of a conventional art; and

[0052] **FIG. 35(b)** is a view showing an ESD protection device having double guard ring structures inserted between the PMOS and NMOS of I/O buffers of a conventional art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0053] The following descriptions of the preferred embodiments are provided to understand the features and the structures of the present invention.

[0054] Please refer to **FIG. 1**. **FIG. 1** is a view showing the structure according to the present invention. As shown in the **FIG. 1**, the present invention relates to an SCR (Silicon-Controlled Rectifier) for ESD (Electrostatic Discharge) protection which comprises two terminal electrodes of a first electrode **1** having high-potential power supply voltage such as VDD and a second electrode **2** having low-potential power supply voltage such as VSS, a PMOS **3**, an NMOS **4** and an SCR structure **5**. Therein, the PMOS **3** is connected to the first electrode **1** and the NMOS **4** is connected to the second electrode **2**, while the SCR structure **5** is placed between PMOS **3** and NMOS **4** for forming an ESD protection. Concerning the structure of the SCR for the ESD protection according to the present invention, the SCR structure **5** can be changed depending on different respective embodiments of the present invention, yet the remaining structures are still depending on the structure of the present invention which is stated above.

[0055] The present invention relates to an SCR for the ESD protection. More particularly, the present invention relates to a circuit and a method which utilizes an embedded SCR in order to provide whole-chip ESD protection design for achieving the effectiveness of ESD protection circuit.

[0056] Please refer to FIG. 2 through FIG. 15. FIG. 2 is a view showing a first embodiment according to the present invention. FIG. 3 is a view showing a second embodiment according to the present invention. FIG. 4 is a view showing a third embodiment according to the present invention. FIG. 5 is a view showing a fourth embodiment according to the present invention. FIG. 6 is a view showing a fifth embodiment according to the present invention. FIG. 7 is a view showing a sixth embodiment according to the present invention. FIG. 8 is a view showing a seventh embodiment according to the present invention. FIG. 9 is a view showing an eighth embodiment according to the present invention. FIG. 10 is a view showing a ninth embodiment according to the present invention. FIG. 11 is a view showing a tenth embodiment according to the present invention. FIG. 12 is a view showing an eleventh embodiment according to the present invention. FIG. 13 is a view showing a twelfth embodiment according to the present invention. FIG. 14 is a view showing a thirteenth embodiment according to the present invention. FIG. 15 is a view showing a fourteenth embodiment according to the present invention. Therein, the SCR structure of the present invention is formed respectively as illustrated in FIG. 2 through FIG. 15, while the differences among the SCR structures are described respectively as below:

[0057] Please refer to FIG. 2. The SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8 and an N-well 9. Additionally, the SCR structure 5 can be collocated with FIG. 16 to protect internal circuit, wherein FIG. 16 is a view showing a first embodiment of circuit according to the present invention.

[0058] Please refer to FIG. 3. The SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8 and an N-well 9, and is further comprised of a second P-typed high-doped region (P⁺) 10 as an anode and a second N-typed high-doped region (N⁺) 11 as a cathode. Additionally, the SCR structure 5 can be collocated with FIG. 16 to protect internal circuit, wherein FIG. 16 is a view showing a first embodiment of circuit according to the present invention.

[0059] Please refer to FIG. 4. The SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9 and a third P-typed high-doped region (P⁺) 12. Additionally, the SCR structure 5 can be collocated with FIG. 17 to protect internal circuit, wherein FIG. 17 is a view showing a second embodiment of circuit according to the present invention.

[0060] Please refer to FIG. 5. The SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9 and a third N-typed high-doped region (N⁺) 13. Additionally, the SCR structure 5 can be collocated with FIG. 18 to protect internal circuit, wherein FIG. 18 is a view showing a third embodiment of circuit according to the present invention.

[0061] Please refer to FIG. 6, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, a second P-typed high-doped region (P⁺) 10 as an anode, a second N-typed high-doped region (N⁺) 11 as a cathode and a third P-typed high-doped region (P⁺) 12. Additionally, the SCR structure 5 can be collocated with FIG. 17 to protect internal circuit, wherein FIG. 17 is a view showing a second embodiment of circuit according to the present invention.

[0062] Please refer to FIG. 7, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, a second P-typed high-doped region (P⁺) 10 as an anode, a second N-typed high-doped region (N⁺) 11 as a cathode and a third N-typed high-doped region (N⁺) 13. Additionally, the SCR structure 5 can be collocated with FIG. 18 to protect internal circuit, wherein FIG. 18 is a view showing a third embodiment of circuit according to the present invention.

[0063] Please refer to FIG. 8, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, at least one dummy gate 14 and a third P-typed high-doped region (P⁺) 12. Additionally, the SCR structure 5 can be collocated with FIG. 17 to protect internal circuit, wherein FIG. 17 is a view showing a second embodiment of circuit according to the present invention.

[0064] Please refer to FIG. 9, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, at least one dummy gate 14 and a third N-typed high-doped region (N⁺) 13. Additionally, the SCR structure 5 can be collocated with FIG. 18 to protect internal circuit, wherein FIG. 18 is a view showing a third embodiment of circuit according to the present invention.

[0065] Please refer to FIG. 10, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9 and a fourth P-typed high-doped region (P⁺) 15 as a trigger node. Additionally, the SCR structure 5 can be collocated with FIG. 19, FIG. 21 and FIG. 23 to protect internal circuit, wherein FIG. 19, FIG. 21 and FIG. 23 are views showing a fourth, a sixth and an eighth embodiments of circuit according to the present invention.

[0066] Please refer to FIG. 11, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9 and a fourth N-typed high-doped region (N⁺) 16 as a trigger node. Additionally, the SCR structure 5 can be collocated with FIG. 20, FIG. 22 and FIG. 24 to protect internal circuit, wherein FIG. 20, FIG. 22 and FIG. 24 are views showing a fifth, a seventh and a ninth embodiments of circuit according to the present invention.

[0067] Please refer to FIG. 12, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, a second P-typed high-doped region (P⁺) 10 as an anode, a second N-typed high-doped region (N⁺) 11 as a cathode and a fourth P-typed high-doped region

(P⁺) 15 as a trigger node. Additionally, the SCR structure 5 can be collocated with FIG. 19, FIG. 21 and FIG. 23 to protect internal circuit, wherein FIG. 19, FIG. 21 and FIG. 23 are views showing a fourth, a sixth and an eighth embodiments of circuit according to the present invention.

[0068] Please refer to FIG. 13, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, a second P-typed high-doped region (P⁺) 10 as an anode, a second N-typed high-doped region (N⁺) 11 as a cathode and a fourth N-typed high-doped region (N⁺) 16 as a trigger node. Additionally, the SCR structure 5 can be collocated with FIG. 20, FIG. 22 and FIG. 24 to protect internal circuit, wherein FIG. 20, FIG. 22 and FIG. 24 are views showing a fifth, a seventh and a ninth embodiments of circuit according to the present invention.

[0069] Please refer to FIG. 14, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, at least one dummy gate 14 and a fourth P-typed high-doped region (P⁺) 15 as a trigger node. Additionally, the SCR structure 5 can be collocated with FIG. 19, FIG. 21 and FIG. 23 to protect internal circuit, wherein FIG. 19, FIG. 21 and FIG. 23 are views showing a fourth, a sixth and an eighth embodiments of circuit according to the present invention.

[0070] Please refer to FIG. 15, the SCR structure 5 of the present invention is comprised of a first P-typed high-doped region (P⁺) 6, a first N-typed high-doped region (N⁺) 7, a P-well 8, an N-well 9, at least one dummy gate 14 and a fourth N-typed high-doped region (N⁺) 16 as a trigger node. Additionally, the SCR structure 5 can be collocated with FIG. 20, FIG. 22 and FIG. 24 to protect internal circuit, wherein FIG. 20, FIG. 22 and FIG. 24 are views showing a fifth, a seventh and a ninth embodiments of circuit according to the present invention.

[0071] In addition, please refer to FIG. 16 through FIG. 24. Therein, FIG. 16 is a view showing a first embodiment of circuit according to the present invention. FIG. 17 is a view showing a second embodiment of circuit according to the present invention. FIG. 18 is a view showing a third embodiment of circuit according to the present invention. FIG. 19 is a view showing a fourth embodiment of circuit according to the present invention. FIG. 20 is a view showing a fifth embodiment of circuit according to the present invention. FIG. 21 is a view showing a sixth embodiment of circuit according to the present invention. FIG. 22 is a view showing a seventh embodiment of circuit according to the present invention. FIG. 23 is a view showing an eighth embodiment of circuit according to the present invention. FIG. 24 is a view showing a ninth embodiment of circuit according to the present invention.

[0072] Please refer to FIG. 25. FIG. 25 is a view showing the structure of another embodiment according to the present invention. The another embodiment is comprised of two terminal electrodes of a first electrode 1 having high-potential power supply voltage such as VDD and a second electrode 2 having low-potential power supply voltage such as VSS, a PMOS 3, an NMOS 4, an SCR structure 17 and another protection structure 18. Therein, the SCR structure 17 is connected from first electrode 1 to another protection structure 18, while another protection structure is connected

from the SCR structure 17 to second electrode 2. The PMOS 3 is connected to the first electrode 1 and the NMOS 4 is connected to the second electrode 2, while SCR structure 17 and another protection structure 18 are placed between PMOS 3 and NMOS 4, to form a circuit protection. Furthermore, the protection structure 18 at least comprises a diode structure or an SCR structure. Additionally, with references to FIG. 26 to FIG. 33, they are views showing embodiments of the circuit for related applications according to the present invention. FIG. 26 is a view showing a tenth embodiment of circuit according to the present invention. FIG. 27 is a view showing an eleventh embodiment of circuit according to the present invention. FIG. 28 is a view showing a twelfth embodiment of circuit according to the present invention. FIG. 29 is a view showing a thirteenth embodiment of circuit according to the present invention. FIG. 30 is a view showing a fourteenth embodiment of circuit according to the present invention. FIG. 31 is a view showing a fifteenth embodiment of circuit according to the present invention. FIG. 32 is a view showing a sixteenth embodiment of circuit according to the present invention. FIG. 33 is a view showing a seventeenth embodiment of circuit according to the present invention.

[0073] In addition, in the structures of another embodiment of the present invention, the SCR structure 17 and the protection structure 18 are comprised of the structures which are shown in FIG. 10 through FIG. 15 respectively and are comprised of circuits which are shown in FIG. 26 through FIG. 29. Furthermore, the protection structure 18 can be comprised of diode which is shown in FIG. 30 through FIG. 33.

[0074] According to the above structures, the present invention relates to an SCR for the ESD protection. More particularly, the present invention relates to a device which utilizes embedded SCR in order to provide ESD protection. As a result, a whole-chip ESD protection design can be achieved by each individual I/O cell in CMOS (Complementary Metal Oxide Semiconductor) IC (Integrated Circuit) with no extra power-rail ESD clamp circuit needed.

[0075] The path of the embedded SCR for the ESD protection is formed between a first electrode 1 having high-potential power supply voltage such as VDD and a second electrode 2 having low-potential power supply voltage such as VSS. The turn-on speed of the embedded SCR can be improved by adding triggers in SCR path.

[0076] When ESD happens, the embedded SCR is quickly triggered on by ESD detection circuit. By the design according to the present invention, the ESD robustness of the whole chip can be efficiently improved with a much smaller layout area. Moreover, the present invention is suitable for applications of IC design and foundry industry. In addition, the present invention is also suitable for effective ESD protection in sub micrometer CMOS IC products.

[0077] The preferred embodiments herein disclosed are not intended to unnecessarily limit the scope of the invention. Therefore, simple modifications or variations belonging to the equivalent of the scope of the claims and the instructions disclosed herein for a patent are all within the scope of the present invention.

What is claimed is:

1. An SCR (Silicon Controlled Rectifier) for the ESD (Electrostatic Discharge) protection comprising:

two terminal electrodes of a first electrode and a second electrode;

a PMOS;

an NMOS; and

an SCR structure,

wherein said PMOS is connected to said first electrode and said NMOS is connected to second electrode, while said SCR structure is placed between said PMOS and said NMOS, to form a circuit protection.

2. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well and an N-well.

3. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

4. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a third P-typed high-doped region (P⁺).

5. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a third N-typed high-doped region (N⁺).

6. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a third P-typed high-doped region (P⁺), a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

7. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a third N-typed high-doped region (N⁺), a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

8. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a third P-typed high-doped region (P⁺).

9. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a third N-typed high-doped region (N⁺).

10. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a fourth P-typed high-doped region (P⁺) as a trigger.

11. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-

doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a fourth N-typed high-doped region (N⁺) as a trigger.

12. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a fourth P-typed high-doped region (P⁺) as a trigger, a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

13. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a fourth N-typed high-doped region (N⁺) as a trigger, a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

14. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a fourth P-typed high-doped region (P⁺) as a trigger.

15. The SCR for the ESD protection according to claim 1, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a fourth N-typed high-doped region (N⁺) as a trigger.

16. An SCR for the ESD protection comprising:

a first electrode and a second electrode as two terminal electrodes;

a PMOS;

an NMOS;

an SCR structure; and

another protection structure,

wherein said SCR structure is connected from said first electrode to said another protection structure, while said another protection structure is connected from said SCR structure to said second electrode, said PMOS is connected to said first electrode and said NMOS is connected to said second electrode, while said SCR structure and said another protection structure are placed between said PMOS and said NMOS, to form a circuit protection.

17. The SCR for the ESD protection according to claim 16, wherein said another protection structure at least comprises a diode structure or an SCR structure.

18. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well and an N-well.

19. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

20. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a third P-typed high-doped region (P⁺).

21. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a third N-typed high-doped region (N⁺).

22. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a third P-typed high-doped region (P⁺), a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

23. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a third N-typed high-doped region (N⁺), a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

24. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a third P-typed high-doped region (P⁺).

25. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a third N-typed high-doped region (N⁺).

26. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a fourth P-typed high-doped region (P⁺) as a trigger.

27. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well and a fourth N-typed high-doped region (N⁺) as a trigger.

28. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a fourth P-typed high-doped region (P⁺) as a trigger, a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

29. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, a fourth N-typed high-doped region (N⁺) as a trigger, a second P-typed high-doped region (P⁺) as an anode and a second N-typed high-doped region (N⁺) as a cathode.

30. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a fourth P-typed high-doped region (P⁺) as a trigger.

31. The SCR for the ESD protection according to claim 16, wherein said SCR structure comprises a first P-typed high-doped region (P⁺), a first N-typed high-doped region (N⁺), a P-well, an N-well, at least one dummy gate and a fourth N-typed high-doped region (N⁺) as a trigger.

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