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(54) ALGORITHM FOR A MEMORY-BASED VITERBI DECODER

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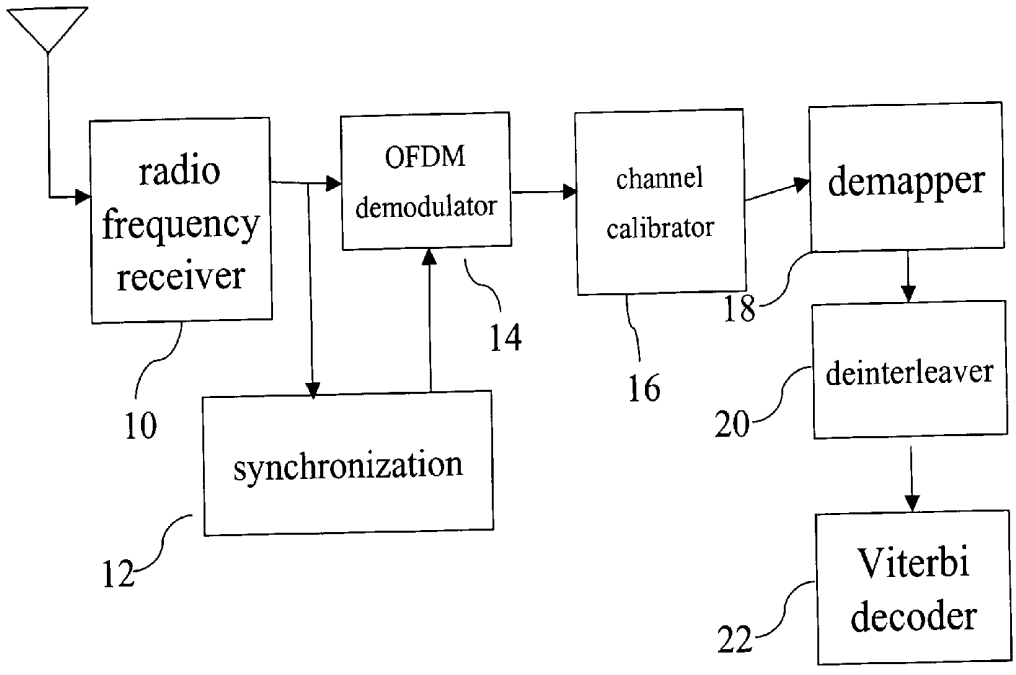
(57) **ABSTRACT**

An algorithm for a memory-based Viterbi decoder is disclosed in the invention, which employs the property of a trace-back path; that is, the similarity between two consecutive trace-back paths becomes higher as the data error rate goes down. Therefore, the algorithm of the invention is to save the previous trace-back path into a register, and as soon as the current trace-back path is found to be the same as the previous one, the demanded path is obtained. After that, the memory read operations will stop, and thus the power consumption made by the memory read operations would be largely reduced. Besides, before the path trace-back, the path prediction can be executed by utilizing the property that the minimum path metric and the path are consecutive. In conclusion, the invention is capable of reducing the number of memory access operations and the power consumption by employing the mechanisms of path matching and path prediction.



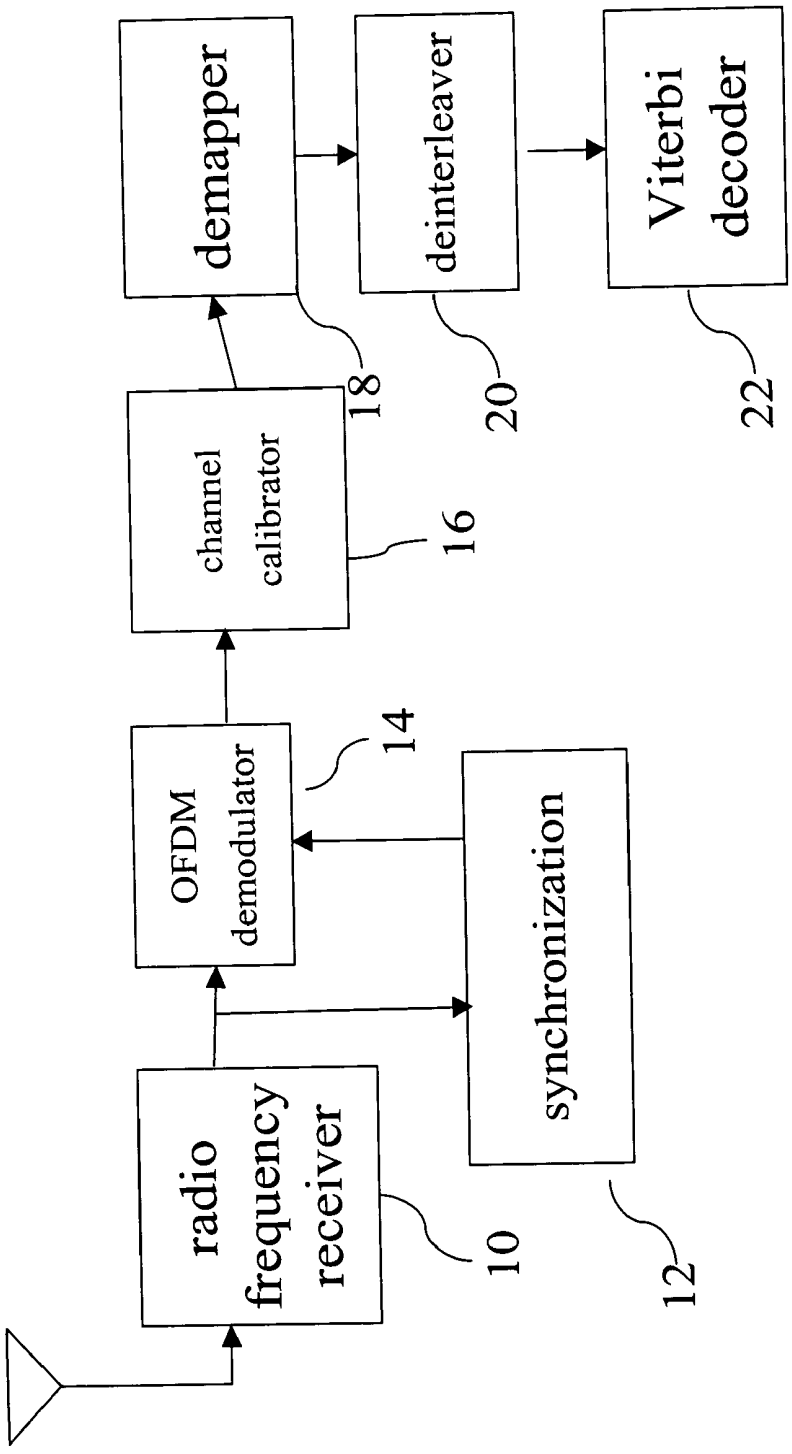

demapper
deinterleaver
Viterbi decoder
channel calibrator
OFDM demodulator
synchronization
radio frequency receiver
10
12
14
16
18
20
22

FIG. 1

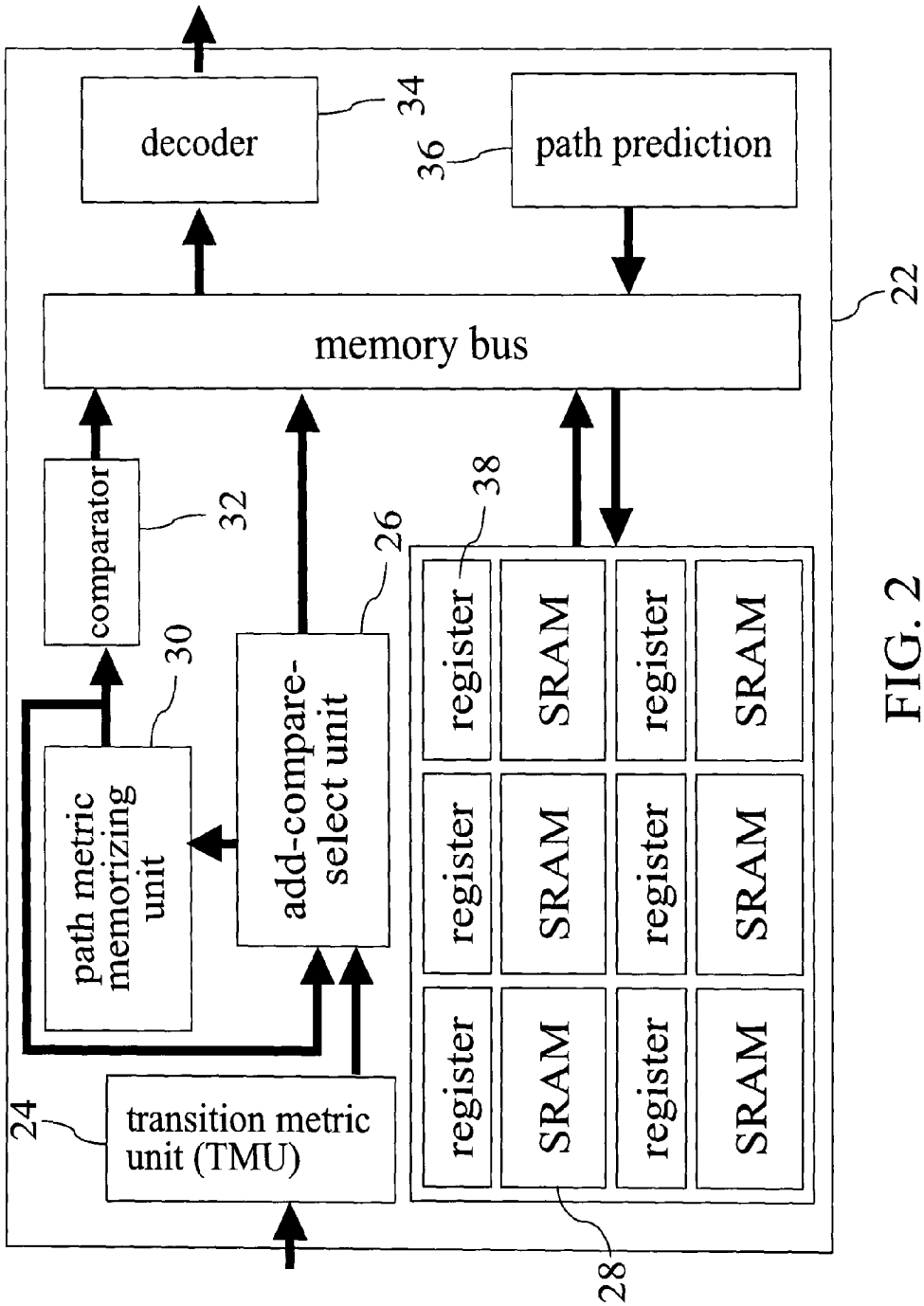

decoder
34
path prediction
36
memory bus
22
comparator
32
38
26
register
SRAM
register
SRAM
30
path metric memorizing unit
add-compare-select unit
register
SRAM
register
SRAM
register
SRAM
register
SRAM
24
transition metric unit (TMU)
28

FIG. 2

ALGORITHM FOR A MEMORY-BASED VITERBI DECODER

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to an algorithm for a memory-based Viterbi decoder and, more particularly, to an algorithm for a Viterbi decoder that applies the mechanisms of path matching and path prediction.

[0003] 2. Description of the Related Art

[0004] Error correction codes have been playing a key role in data transmission because adding them into digitalized data has been a must to ensure the correctness of data transmission. In general, error correction codes can be classified into two categories. One category is a block code, which employs a method to encode data per block, and there is no time relation between each block. The other category is a convolutional code, which, unlike the block code, has time relation existing in the encoding process.

[0005] The most common method applied to a convolutional code decoder is the Viterbi algorithm, which is also the most effective decoding algorithm for the convolutional code. A decoder that employs such algorithm is called the Viterbi decoder. During the decoding process, the existing architecture must decode a certain length of data, despite the data is correct or incorrect, in order to obtain a correct data. The length of data is called a truncation length. During the decoding, a large quantity of memory bandwidth and a large number of memory access operations are required. As for real applications, usually a decoding that is smaller than the truncation length is good enough for judging the precision of data. For this reason, a lot of power is wasted during memory access.

[0006] To illustrate the redundant power consumption, the U.S. Pat. No. 5,208,816 will be illustrated as an example. This prior art provides a memory algorithm for a high-speed Viterbi decoder, which transmits parity checking code for inspecting the Viterbi decoder and determining data reliability. When unreliable data has been detected, the second round of Viterbi estimation or retransmission will be executed to increase data precision. However, the method is only suitable for low-speed transmission. Besides, because a conventional Viterbi decoder requires a lot of memory bandwidth, the low power consumption is hard to be achieved. Moreover, another U.S. Pat. No. 4,905,317 is also disclosed, which is to synthesize the states when executing the path trace-back operation for obtaining a jumping back effect so that the memory access operations can be decreased as well as the decoding speed can be increased. Unfortunately, even though the decoding speed has been increased, it cannot satisfy the current demand for decoding speed when application is involved. Besides, the paths that have been traced back by jumping back have to be figured out again when executing the next decoding because the data in these paths is probably a solution on the next decoding, which in turn will demand a lot of redundant calculations and memory read operations.

[0007] Therefore, the invention provides an algorithm for a memory-based Viterbi decoder, which employs the mechanisms of path matching and path prediction so as to reduce the number of memory access operations and the power consumption so that the aforementioned drawback lying in the prior art can be improved.

SUMMARY OF THE INVENTION

[0008] The main and first object of the invention is to provide an algorithm for a memory-based Viterbi decoder, which can predict the possible correct path while concurrently calculating the path metrics so that the number of memory access operations can be reduced during the subsequent decoding process; meanwhile, the truncation length required by the decoding can be dynamically adjusted in accordance with the mechanism of path merging according to the different error probabilities so that the power consumption made by the memory access operations during the decoding process can be reduced.

[0009] The second object of the invention is to provide an algorithm for a memory-based Viterbi decoder, which can dynamically adjust the quantity of memory access operations during the decoding process according to the received state of data so that redundant calculations in the real applications can be discarded by employing the property of the received data codes in the error correction circuit in order to effectively reduce the power consumption of the circuits in the real operation.

[0010] The third object of the invention is to provide an algorithm for a memory-based Viterbi decoder, which can largely reduce the memory read operations so that a high-speed application with low power consumption can be achieved.

[0011] The fourth object of the invention is to provide a simple method for achieving the low power consumption so that the method can be cost competitive as well as application competitive.

[0012] The algorithm of the invention includes the following procedures: first, to calculate each path according to the inputted data; second, to calculate each path metric and obtain a minimum path metric after comparing the path metrics so as to find the state of the minimum path metric, and when the state of the minimum path metric is found to be located on a consecutive path, it means that the consecutive path is the predicted trace-back path; and finally, to find a merging point according to the predicted trace-back path while executing the trace-back path procedure, so that the decoding process can be proceeded to obtain a decoding signal.

[0013] Also, the aforementioned path prediction procedure further includes the following steps: first, to find the state of the minimum path metric at the time t; second, if the state transition sequence from the time t−1 to the time t is located within the trellis, the state of the minimum path metric of the time t will be saved in a register; third, to predict the time t+1 and save the calculated state in the register and then combine the calculated state with the state of the time t; and finally, the path prediction procedure will stop when the state of the minimum path metric are not located on a consecutive path. In particular, if the path saved in the register is ensured to be correct, the decoding process will be based on the register access.

[0014] Moreover, the path matching procedure can be executed concurrently while executing the path trace-back procedure. The path matching procedure includes the fol-

lowing steps: first, to save the trace-back path of the previous moment to the register; next, to compare the current trace-back path to the previous trace-back path; and last, when the two paths are merged, the demanded path can be obtained from the register, and the subsequent decoding process will be executed by using the register.

[0015] The objects and technical contents of the invention will be better understood through the description of the following embodiments with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] **FIG. 1** is a schematic diagram showing the Viterbi decoder being applied to a wireless local area network.

[0017] **FIG. 2** is a schematic diagram showing the architecture of the Viterbi decoder of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] The method of path trace-back is suitable for the Viterbi decoder with large number of states but low power consumption. However, as the demand for higher decoding speed increases, the demand for the bandwidth of the whole memory will become greater, which in turn will increase the power consumption made by the memory access. In addition, it is obvious that the similarity between two consecutive trace-back paths will become higher as the data error rate goes down. When in real application, the bit error rate (BER) of the inputted data will be around 10^{-2}, and ninety-five percent of the trace-back paths will be similar at this time. For this reason, the invention applies the above-mentioned properties as well as the mechanisms of path matching and path prediction so that up to seventy-five percent of the number of memory read operations can be eliminated, and the power consumption can be reduced as well.

[0019] **FIG. 1** is a schematic diagram showing the Viterbi decoder is applied to an IEEE 802.11a wireless local area network. As shown in **FIG. 1**, after the RF receiver **10** has received the radio frequency signals, the following procedures will be executed sequentially: first, the synchronizer **12** will synchronize the signals; second, the demodulator of the orthogonal frequency division multiplexing (OFDM) **14** will demodulate the signals; third, the channel calibrator **16** will calibrate the signals; fourth, the demapper **18** will demap each formatting code; fifth, the deinterleaver **20** will restore the data that has been interleaved to different symbols to its original place; and finally, the data will be transmitted to a Viterbi decoder **22** for decoding the convolutional code so as to rectify the data error generated during the transmission.

[0020] During Viterbi decoder's decoding of the convolutional code, only a decoded code length that is smaller than the truncation length will be required to determine the correct data. Therefore, the invention is capable of predicting the possible correct path concurrently while calculating the path metrics under the memory-based architecture so that the number of memory access operations can be reduced during the subsequent decoding process.

[0021] **FIG. 2** is a schematic diagram showing the architecture of the Viterbi decoder of the invention, which is to illustrate the detail steps contained in the algorithm to be applied to the memory-based Viterbi decoder **22**. As shown in **FIG. 2**, the detailed steps are: first, a transition metric unit (TMU) **24** will calculate branch metrics according to the inputted data; second, the branch metrics will be transmitted to an add-compare-select unit (ACSU) **26** for path metrics calculation and path selection; third, the derived path will be stored in the survivor memory unit **28** (SMU); fourth, each path metric will be obtained through a path metric memorizing unit **30**, and then the comparator **32** will compare the path metrics and derive a trace-back starting point to be transmitted to a decoder **34**; finally, the decoder **34** will perform path trace-back by reading the required data from the survivor memory unit **28** and continue with the decoding.

[0022] During the path calculation, the path prediction **36** can be executed concurrently, which is to find the state of the minimum path metric according to the path metrics. Then, the next step is to judge whether the state of the minimum path metric is located on a consecutive path. And in order to complete the judgment, the state of the minimum path metric at the time t must be found first. When the state transition sequence from the time t−1 to the time t is found to be located in the trellis, the state of the minimum path metric at the time t will be saved in a register **38** located inside the survivor memory unit **28** for adjusting the memory access during the decoding. Afterwards, the prediction of time t+1 will be performed, and its state will be saved in the register **38** and merged with the state value of time t. In particular, the prediction can be consecutively executed between the adjacent time points, and if the states of the minimum path metrics are located on the same consecutive path, it means that the consecutive path is the desired trace-back path. Conversely, if the values are found not locating on a consecutive path, the prediction procedure will stop. As soon as the prediction of trace-back path has been done, the decoder **34** will find a merging point to proceed with the decoding according to the trace-back path so as to obtain the demanded decoding signal without decoding to the truncation length.

[0023] If the trace-back path has been correctly predicted, it means that the path stored in the register **38** is correct, and thus the decoding will be executed by accessing the register **38**.

[0024] In addition to executing the path prediction **36**, the path matching can be performed concurrently or separately. The path matching is first to store the trace-back path calculated at the previous moment into the register **38** and then calculate the trace-back path at the current moment. Next, the two trace-back paths at the previous moment and the current moment will be compared, and when the two paths are found merged, the demanded path is obtained.

[0025] The algorithm of the invention can be implemented through software, multiprocessor, or digital signal processor. Besides, the method provided in the invention is to associate the property of path back-trace with the reliability of the inputted data of the Viterbi algorithm. Therefore, the trace-back path can be stored in the register so that there is a good chance to directly use the path in the register at the next trace-back and thus eliminate most of the memory read operations. Moreover, the invention decides the memory read operation on the basis of the reliability of inputted data so that the bandwidth ratio of the memory writing to the

memory reading can approximately reach a ratio of 1:1. Finally, the Viterbi decoder can appropriately adjust the decoding calculations according to the accuracy of the inputted data, which certainly will be a plus to the efficiency of the Viterbi decoder.

[0026] In conclusion, the invention can dynamically adjust the quantity of memory access operations during the decoding process according to the state of the received data so that the redundant calculations can be eliminated in the error correction circuit in the real application by utilizing the property of the received data codes. Therefore, when the circuits are in real operation, the number of memory access operations and the power consumption can be reduced, which in turn can achieve a high-speed application with low power consumption. Hence, the invention is able to achieve low-power consumption with a simple method, which in turn proves that the invention can be very competitive in cost saving and practical application.

[0027] The embodiments above are only intended to illustrate the invention; they do not, however, to limit the invention to the specific embodiments. Accordingly, various modifications and changes may be made without departing from the spirit and scope of the invention as described in the appended claims.

What is claimed is:

1. An algorithm for a memory-based Viterbi decoder, including the following procedures:

to calculate a path according to the inputted data;

to calculate each path metric and obtain a minimum path metric by comparing the path metrics so as to find the state of the minimum path metric;

to judge whether the state of the minimum path metric is located on a consecutive path, and if so, it means that the consecutive path is the predicted trace-back path; otherwise, the prediction will be stopped; and

to find a merging point to execute the decoding process according to the predicted trace-back path during the path trace-back procedure so as to get a decoded signal.

2. The algorithm for a memory-based Viterbi decoder as claimed in claim 1, wherein the minimum path metric can be utilized to predict the path concurrently while executing the path calculation.

3. The algorithm for a memory-based Viterbi decoder as claimed in claim 1, wherein during the decoding of the predicted trace-back path, the length of the predicted trace-back path is smaller than that of the decoding of a truncation length.

4. The algorithm for a memory-based Viterbi decoder as claimed in claim 1, wherein the procedure of judging that whether the state of the minimum path metric is located on a consecutive path further includes the following steps:

to find the state of the minimum path metric at the time t;

to save the state of the minimum path metric of the time t in a register

if the state transition sequence from the time t−1 to the time t is located within the trellis; and

to predict the time t+1, to save the calculated state in the register, and to combine the calculated state with the state of the time t; the path prediction procedure will stop as soon as the states of the minimum path metrics after combination are found not to be located on a consecutive path.

5. The algorithm for a memory-based Viterbi decoder as claimed in claim 4, wherein if the path saved in the register is correct, the decoding process will be based on the register access.

6. The algorithm for a memory-based Viterbi decoder as claimed in claim 1, wherein the path matching procedure can be executed concurrently while executing the path prediction procedure, and the path matching procedure further comprises the following steps:

to save the trace-back path of the previous moment to the register;

and

to compare the current trace-back path to the previous trace-back path, and when the two trace-back paths are merged, the demanded path can be obtained.

7. The algorithm for a memory-based Viterbi decoder as claimed in claim 6, wherein if the path saved in the register is correct, the decoding process will be based on the register access.

8. The algorithm for a memory-based Viterbi decoder as claimed in claim 4 or claim 6, wherein the register is provided inside the survivor memory unit of the Viterbi decoder to adjust the memory access during the decoding process.

9. The algorithm for a memory-based Viterbi decoder as claimed in claim 1, wherein the algorithm can be implemented through software, multiprocessor, or digital signal processor.

10. An algorithm for a memory-based Viterbi decoder, including the following procedures:

to calculate a path according to the inputted data;

to calculate each path metric and obtain the minimum path metric by comparing the path metrics so as to find the state of the minimum path metric;

to judge whether the state of the minimum path metric is located on a consecutive path, and if so, it means that the consecutive path is the predicted trace-back path; otherwise, the prediction will be stopped;

to save the trace-back path of the current moment into a register;

to find a merging point to execute the decoding process according to the predicted trace-back path during the path trace-back procedure so as to get a decoded signal; and

to calculate the current trace-back path and compare the current trace-back path to the previous trace-back path; when the two paths are merged, the demanded path is derived, and the subsequent decoding procedure can be executed.

11. The algorithm for a memory-based Viterbi decoder as claimed in claim 10, wherein the minimum path metric can be utilized to predict the path concurrently while executing the path calculation.

12. The algorithm for a memory-based Viterbi decoder as claimed in claim 10, wherein during the decoding of the

predicted trace-back path, the length of the predicted trace-back path is smaller than that of the decoding of a truncation length.

13. The algorithm for a memory-based Viterbi decoder as claimed in claim 10, wherein the procedure of judging that whether the state of the minimum path metric is located on a consecutive path further includes the following steps:

to find the state of the minimum path metric at the time t;

to save the state of the minimum path metric of the time t in a register if the state transition sequence from the time t−1 to the time t is located within the trellis; and

to predict the time t+1, to save the calculated state in the register, and to merge the calculated state with the state of the time t; the path prediction procedure will stop as soon as the states of the minimum path metrics after merging are found to be located on a consecutive path.

14. The algorithm for a memory-based Viterbi decoder as claimed in claim 10 or claim 13, wherein if the path saved in the register is correct, the decoding process will be based on the register access.

15. The algorithm for a memory-based Viterbi decoder as claimed in claim 10, wherein the register is provided inside the survivor memory unit of the Viterbi decoder to adjust the memory access during the decoding process.

16. The algorithm for a memory-based Viterbi decoder as claimed in claim 10, wherein the algorithm can be implemented through software, multiprocessor, or digital signal processor.

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