US 20040063311A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2004/0063311 A1**

Chang et al. (43) **Pub. Date: Apr. 1, 2004**

(54) **STRUCTURE OF THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF**

(75) Inventors: **Kow Ming Chang**, Taipei (TW); **Yuan Hung Chung**, Taipei (TW)

Correspondence Address:
HAVERSTOCK & OWENS LLP
162 NORTH WOLFE ROAD
SUNNYVALE, CA 94086 (US)

(73) Assignee: **National Chiao Tung University**

(21) Appl. No.: **10/259,137**

(22) Filed: **Sep. 26, 2002**

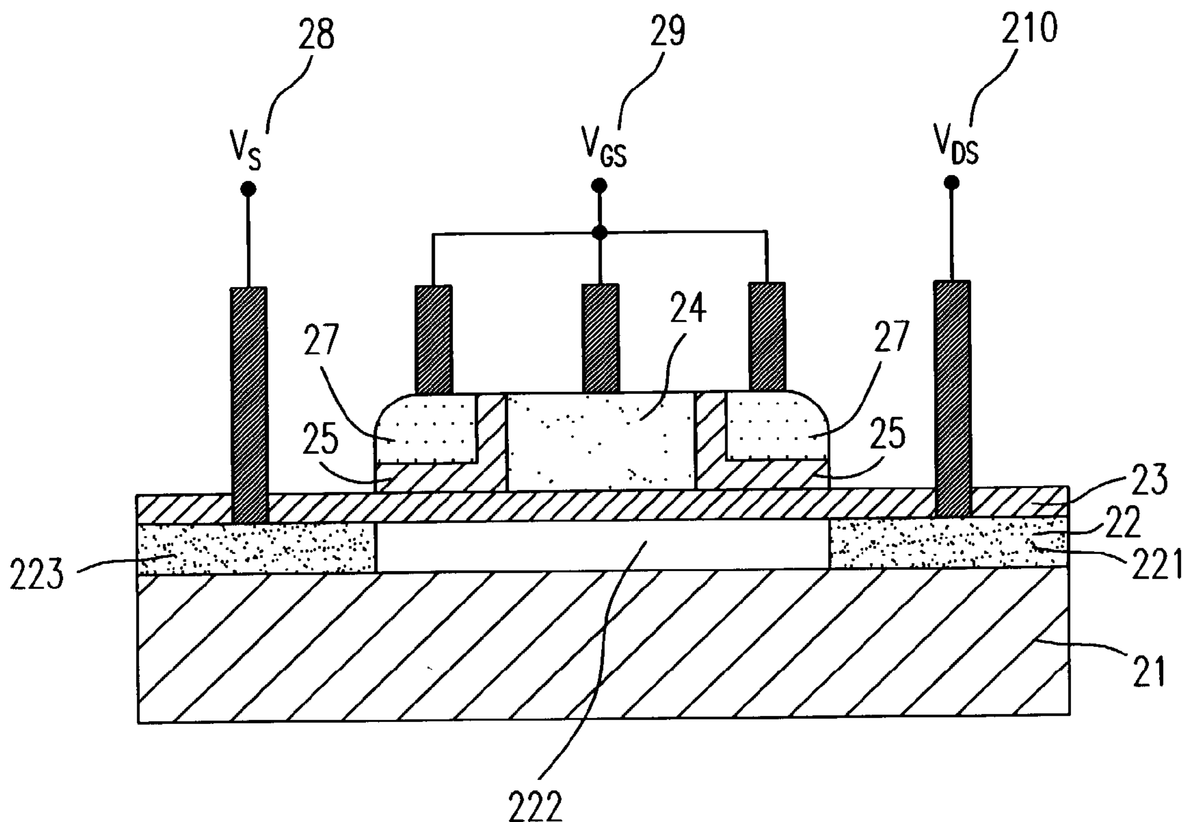
Publication Classification

(51) **Int. Cl.^{7}** **H01L 21/44**

(52) **U.S. Cl.** **438/656**

(57) **ABSTRACT**

A method of manufacturing a thin film transistor for solving the drawbacks of the prior art is disclosed. The method includes steps of providing an insulating substrate, sequentially forming a source/drain layer, a primary gate insulating layer, and a first conducting layer on the insulating substrate, etching the first conducting layer to form a primary gate; sequentially forming a secondary gate insulating layer and a second conducting layer on the primary gate; and etching the second conducting layer to form a first secondary gate and a second secondary gate.



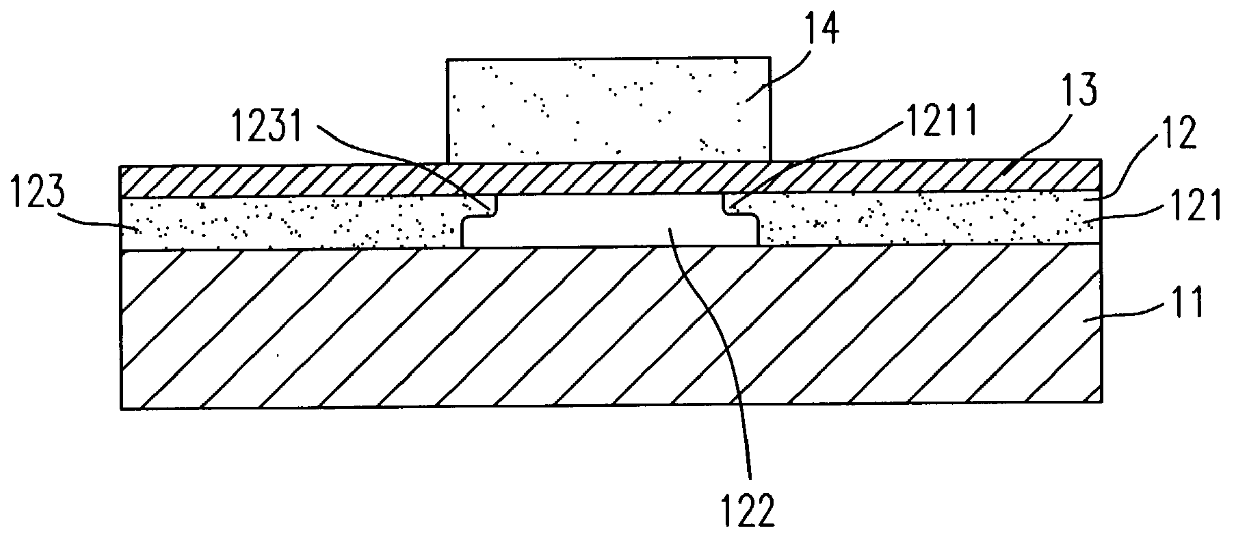


Fig. 1 (PRIOR ART)

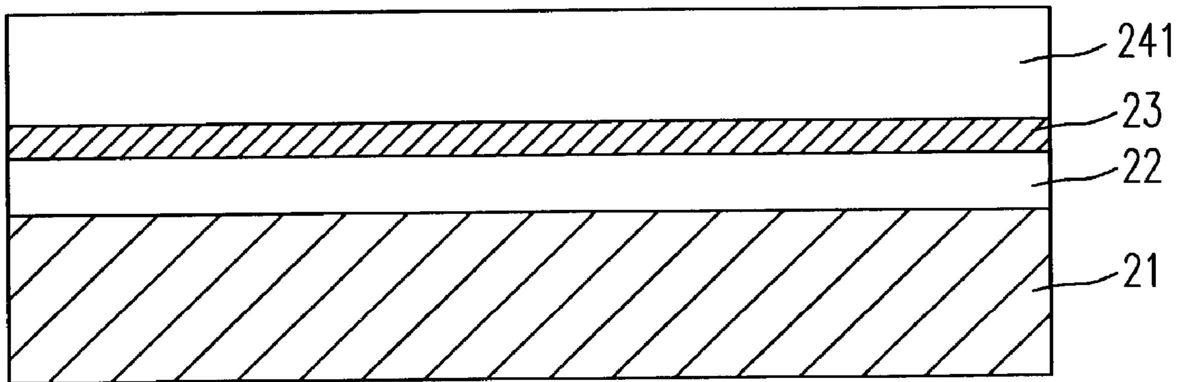


Fig. 2 (a)

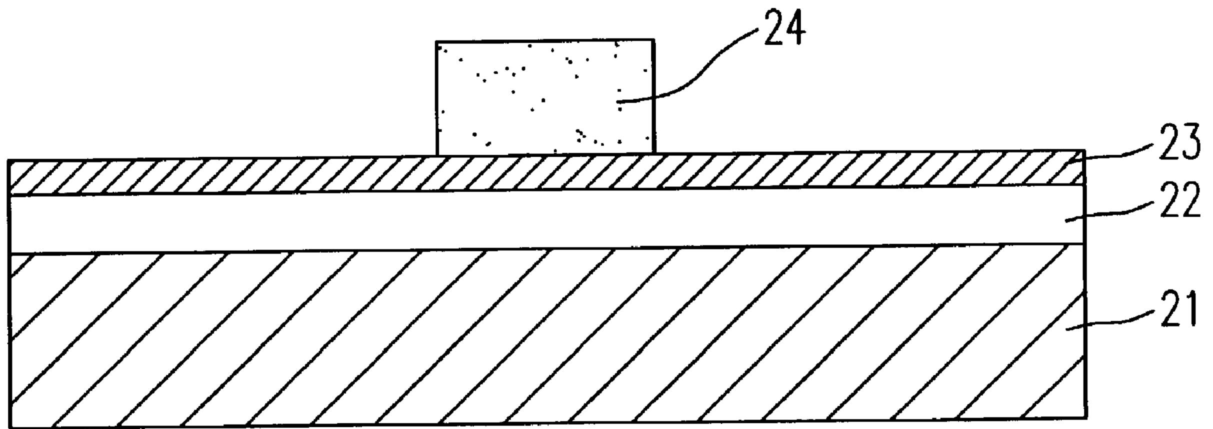


Fig. 2 (b)

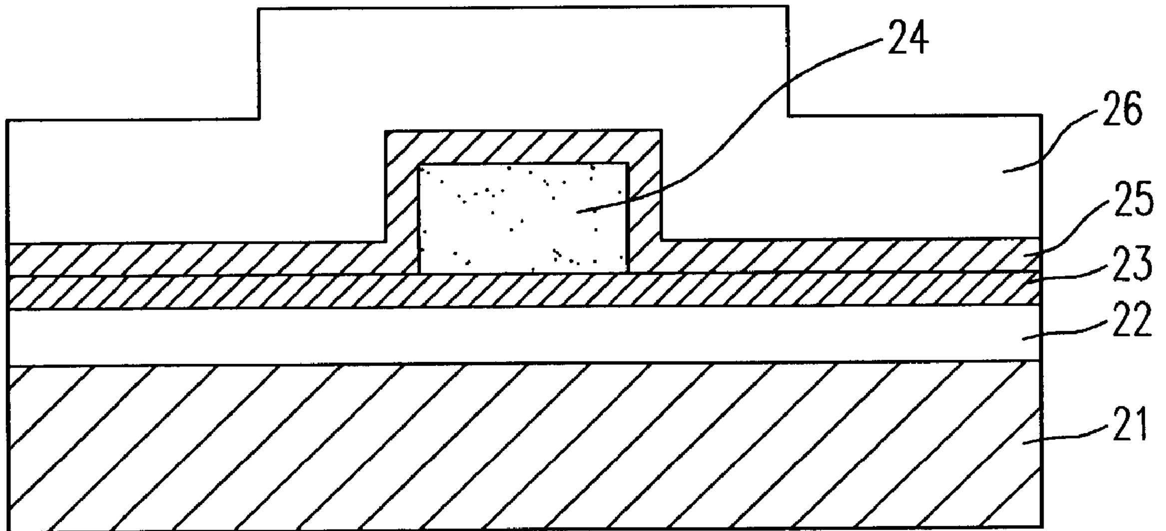


Fig. 2 (c)

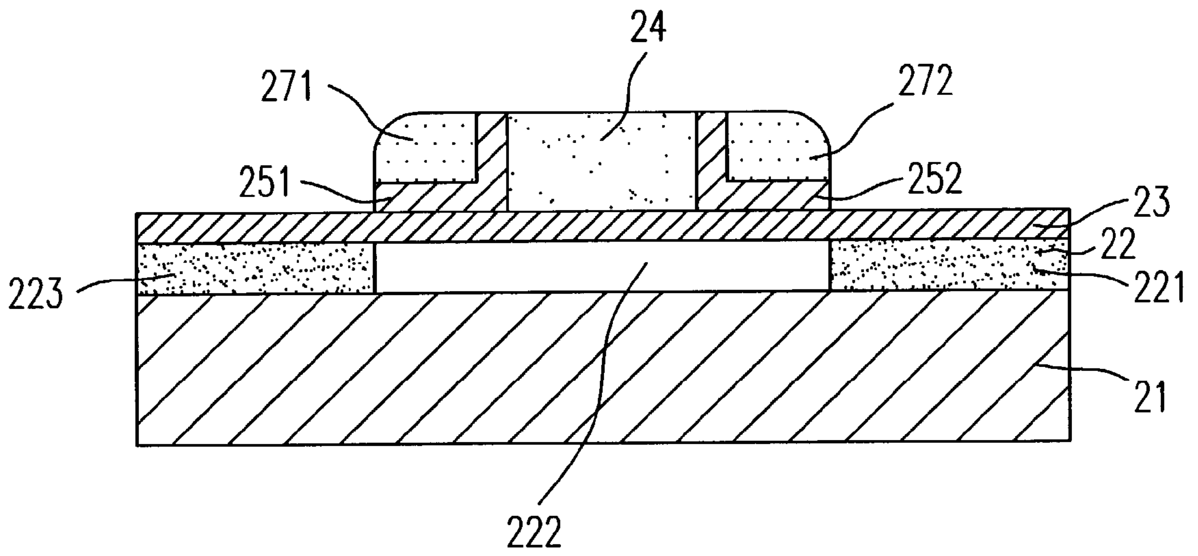


Fig. 2(d)

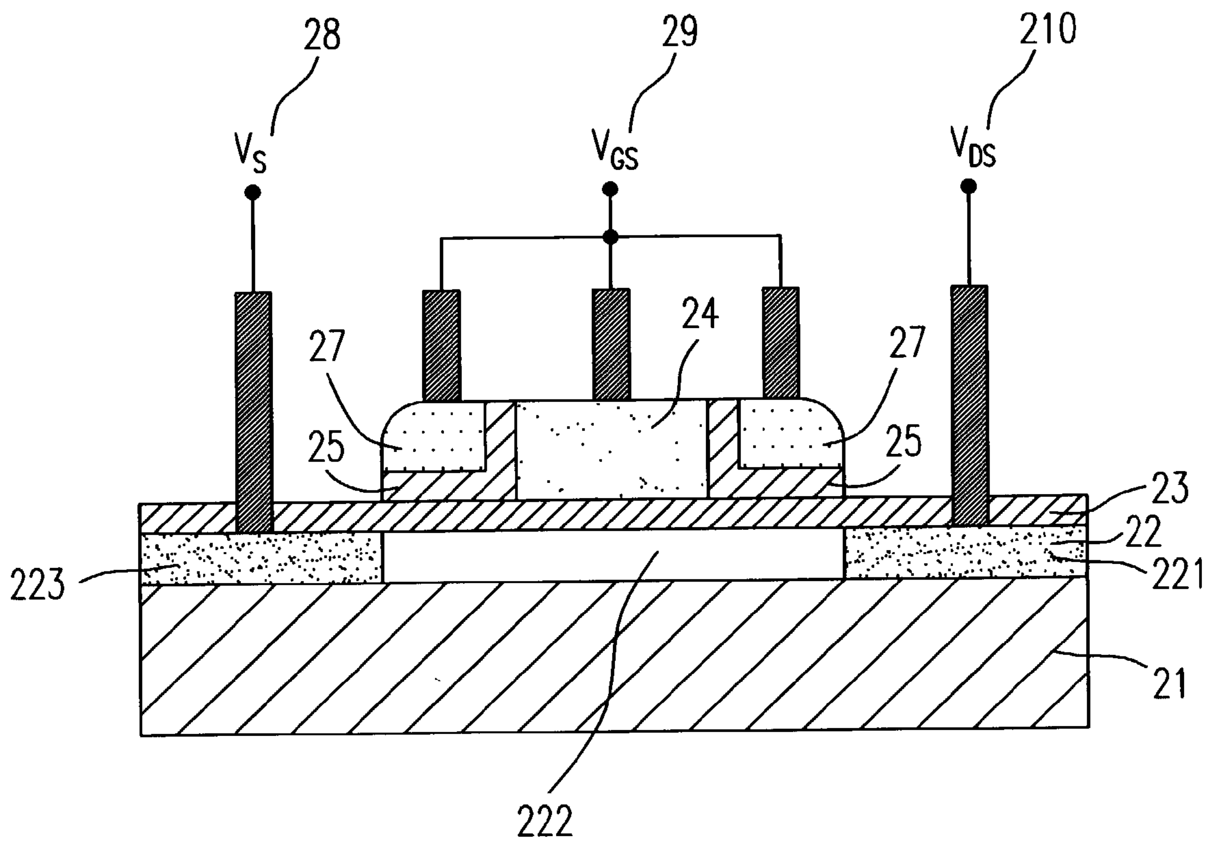


Fig. 2 (e)

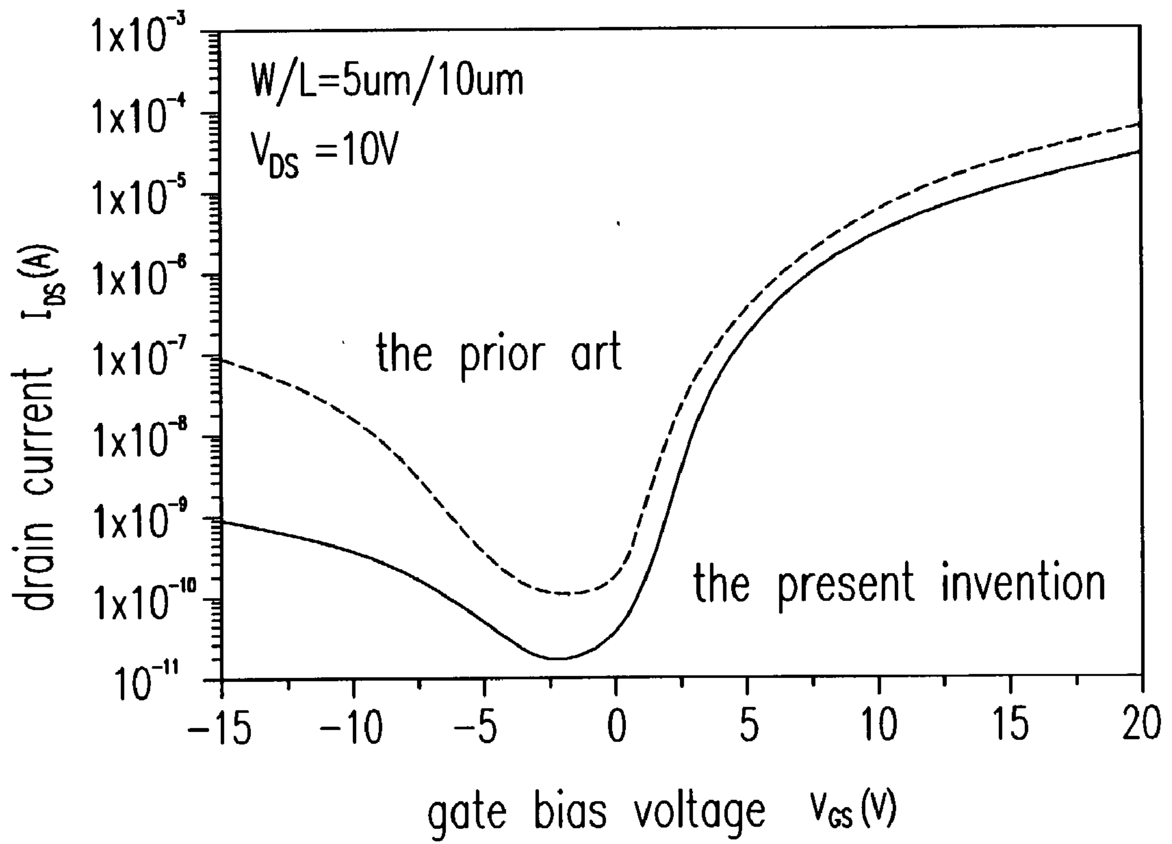


Fig. 3

STRUCTURE OF THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF

FIELD OF THE INVENTION

[0001] The present invention is related to a structure of a thin film transistor and a manufacturing method thereof, and more particularly to a structure of a thin film transistor applied to TFT-LCD and a manufacturing method thereof.

BACKGROUND OF THE INVENTION

[0002] Thin film transistor liquid crystal Display (TFT-LCD) has become one of the most popular and modem information goods. As result of being light, small and portable, having a lower operating voltage, being free of harmful radiation and suited to production on large scale, TFT-LCD substitutes for cathode ray tube display as a caressed computer display device.

[0003] In accordance with the structure of TFT-LCD, Drain of TFT has a higher electric field while TFT is operating, and there should be an off-state leakage current resulted while the device is shut down, thereby the application of TFT-LCD being limited.

[0004] Presently, someone provides a lightly doped drain structure and a field induced drain structure for preventing TFT-LCD from the off-state leakage current. **FIG. 1** illustrates a lightly doped drain structure of the prior art for solving the problem of the off-state leakage current. The structure includes an insulating substrate **11**, a source/drain layer **12**, a gate insulating layer **13** and a gate layer **14**, wherein the source/drain layer **12** further includes a drain **121**, a lightly doped drain **1211**, a channel **122**, a source **123** and a lightly doped source **1231**. The electric field of the drain **121** is reduced by means of adding lightly doped regions (i.e. the lightly doped drain **1211** and the lightly doped source **1231**) corresponding to the original source **123** and the original drain **121** respectively near the channel **122**, so as to prevent from the leakage current. However the TFT-LCD with the lightly doped regions is complex and hard to manufacture. Furthermore the resistance will increases because of the lightly doped degree. As result of the series resistance of the drain **121** and the source **123** increasing, the operating speed of the device reduces and the power dissipation increases.

[0005] Moreover, another improving structure of field-induction drain has been disclosed. However it has to add an extra photolithographic process for manufacturing the improving structure. The more photolithographic processes are introduced, the more mis-alignment and infected defects are resulted. Therefore, the cost and the manufacturing time of the improving structure must increase and the yield reduces.

[0006] Hence, the present invention is attempted to improve the prior art and provides a structure of a thin film transistor applied to a TFT-LCD and a manufacturing method thereof for preventing TFT-LCD from the leakage current.

SUMMARY OF THE INVENTION

[0007] It is one object of the present invention to provide a structure of a thin film transistor applied to TFT-LCD and a manufacturing method thereof.

[0008] It is another object of the present invention to provide a structure of a thin film transistor and a manufacturing method thereof for preventing TFT-LCD from the leakage current.

[0009] According to the present invention, the method for manufacturing a thin film transistor, includes steps of providing an insulating substrate, sequentially forming a source/drain layer, a primary gate insulating layer, and a first conducting layer on the insulating substrate, etching the first conducting layer to form a primary gate, sequentially forming a secondary gate insulating layer and a second conducting layer on the primary gate, and etching the second conducting layer to form a first secondary gate and a second secondary gate.

[0010] Certainly, the insulating substrate can be a glass.

[0011] Certainly, the source/drain layer can be a high-doping semiconductor layer.

[0012] Certainly, the high-doping semiconductor layer can be high-doping polycrystalline silicon.

[0013] Preferably, the source/drain layer includes a drain, a channel and a source.

[0014] Preferably, the channel has a length equal to a sum of a length of the primary gate, a width of the secondary insulating layer, a length of the first secondary gate and a length of the second secondary gate.

[0015] Certainly, the primary gate insulating layer can be one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

[0016] Certainly, the first conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[0017] Certainly, the step (c) can be executed by means of a reactive ion etching.

[0018] Certainly, the secondary gate insulating layer can be one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

[0019] Certainly, the second conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[0020] Certainly, the step (e) can be executed by means of a reactive ion etching.

[0021] According to the present invention, the structure of a thin film transistor includes an insulating substrate, a source/drain layer disposed on the insulating substrate, a primary insulating layer disposed on the source/drain layer, a primary gate disposed on the primary insulating layer, a secondary insulating layer disposed on the primary insulating layer, and a secondary gate disposed on the secondary insulating layer and insulated from the primary gate via the secondary insulating layer.

[0022] Preferably, the secondary insulating layer further includes a first secondary insulating layer and a second secondary insulating layer.

[0023] Preferably, the secondary gate further includes a first secondary gate and a second secondary gate disposed on the first secondary insulating layer and the second secondary insulating layer respectively.

[0024] Certainly, the insulating substrate can be a glass.

[0025] Certainly, the source/drain layer can be a high-doping semiconductor layer.

[0026] Certainly, the high-doping semiconductor layer can be high-doping polycrystalline silicon.

[0027] Preferably, the source/drain layer includes a drain, a channel and a source.

[0028] Preferably, the channel has a length equal to a sum of a length of the primary gate, a width of the secondary insulating layer, and a length of the secondary gate.

[0029] Certainly, the primary gate insulating layer can be one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

[0030] Certainly, the first conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[0031] Certainly, the primary gate can be formed by means of a reactive ion etching.

[0032] Certainly, the secondary gate insulating layer can be one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

[0033] Certainly, the second conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[0034] Certainly, the secondary gate can be formed by means of a reactive ion etching.

[0035] According to the present invention, the structure of a thin film transistor includes an insulating substrate, a source/drain layer disposed on the insulating substrate, a primary insulating layer disposed on the source/drain layer, a primary gate disposed on the primary insulating layer, at least a secondary insulating layer disposed on the primary insulating layer, and at least a secondary gate disposed on the at least a secondary insulating layer and insulated from the primary gate via the at least a secondary insulating layer.

[0036] Certainly, the insulating substrate can be a glass.

[0037] Certainly, the source/drain layer can be a high-doping semiconductor layer.

[0038] Certainly, the high-doping semiconductor layer can be high-doping polycrystalline silicon.

[0039] Preferably, the source/drain layer includes a drain, a channel and a source.

[0040] Preferably, the channel has a length equal to a sum of a length of the primary gate, a width of the at least secondary insulating layer, and a length of the at least a secondary gate.

[0041] Certainly, the primary gate insulating layer can be one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

[0042] Certainly, the at least a secondary gate insulating layer can be one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

[0043] Now the foregoing and other features and advantages of the present invention will be more clearly understood through the following descriptions with reference to the drawings, wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

[0044] **FIG. 1** illustrates a lightly doped drain structure of the prior art for solving the problem of the off-state leakage current;

[0045] FIGS. **2**(*a*)-**2**(*e*) illustrate the steps of manufacturing the thin film transistor according to the preferred embodiment of the present invention;

[0046] **FIG. 3** illustrates electricity properties of the present invention compared with those of the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0047] FIGS. **2**(*a*)-**2**(*d*) illustrate the steps of manufacturing the thin film transistor according to the preferred embodiment of the present invention. The method for manufacturing a thin film transistor includes several steps. First, an insulating substrate **21** is provided and a source/drain layer **22**, a primary gate insulating layer **23**, and a first conducting layer **241** are sequentially formed on the insulating substrate **21**, shown in **FIG. 2**(*a*). Secondly, the first conducting layer **241** is etched to form a primary gate **24**, shown in **FIG. 2**(*b*). Thirdly, a secondary gate insulating layer **25** and a second conducting layer **26** are sequentially formed on the primary gate **24**, shown in **FIG. 2**(*c*). Finally, the second conducting layer **26** and the secondary gate insulating layer **25** are etched to respectively form a first secondary gate **271** and a second secondary gate **272**, and a first secondary gate insulating layer **251** and a second secondary gate insulating layer **252**, shown in **FIG. 2**(*d*). As to **FIG. 2**(*e*), it illustrates the bias status of the thin film transistor including a source bias voltage (VS) **28**, a gate/source bias voltage (VGS) **29** and a drain/source bias voltage (VDS) **210**.

[0048] According to the above embodiment of the present invention, the insulating substrate **21** is a glass substrate, the source/drain layer **22** is a high-doping semiconductor layer, and the high-doping semiconductor layer is high-doping polycrystalline silicon. Furthermore, the source/drain layer **22** includes a drain **221**, a channel **222** and a source **223**. Meanwhile, the channel **222** has a length equal to a sum of a length of the primary gate **24**, a width of the first secondary

insulating layer **251** and the second secondary insulting layer **252**, a length of the first secondary gate **271** and the second secondary gate **272**.

[**0049**] As to the primary gate insulating layer **23** and the secondary gate insulating layer **25**, they can be one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof. However the first conducting layer **241** and the second conducting layer **26** are one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AMSi), copper (Cu) and a mixture thereof. Meanwhile, the first conducting layer **241**, the second conducting layer **26** and the secondary gate insulating layer **25** are etched by means of a reactive ion etching.

[**0050**] Referring to **FIG. 3**, it illustrates electricity properties of the present invention compared with those of the prior art. As result of operating the thin film transistor according to the bias status of **FIG. 2**(*e*), the thin film transistor of the present invention causes a lower leakage current. In **FIG. 3**, when the thin film transistor of the present invention and the thin film transistor of the prior art are operated in the same condition (VDS=10V), the leakage current caused by the present invention is lower than that caused by the prior art. While VDS=15V, the leakage current (1×10^{-9}A) of the present invention is 100 times as that (1×10^{-7}A) of the prior art.

[**0051**] Accordingly, the present invention reduces the electric field of the drain region by means of providing a thicker gate insulating layer, so as to improve the problem of the high off-state leakage current of a thin film transistor. Comparing with the prior art, the present invention introduces four photolithographic processes equal to the traditional one, but doesn't have to add an extra photolithographic process. Therefore, the present invention can solve the drawbacks of the prior art and be practicability.

[**0052**] Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by the way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. A method for manufacturing a thin film transistor, comprising steps of:

(a) providing an insulating substrate;

(b) sequentially forming a source/drain layer, a primary gate insulating layer, and a first conducting layer on said insulating substrate;

(c) etching said first conducting layer to form a primary gate;

(d) sequentially forming a secondary gate insulating layer and a second conducting layer on said primary gate; and

(e) etching said second conducting layer to form a first secondary gate and a second secondary gate.

2. The method according to claim 1, wherein said insulating substrate is a glass.

3. The method according to claim 1, wherein said source/drain layer is a high-doping semiconductor layer.

4. The method according to claim 3, wherein said high-doping semiconductor layer is high-doping polycrystalline silicon.

5. The method according to claim 1, wherein said source/drain layer comprises a drain, a channel and a source.

6. The method according to claim 5, wherein said channel has a length equal to a sum of a length of said primary gate, a width of said secondary insulating layer, a length of said first secondary gate and a length of said second secondary gate.

7. The method according to claim 1, wherein said primary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

8. The method according to claim 1, wherein said first conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

9. The method according to claim 1, wherein said step (c) is executed by means of a reactive ion etching.

10. The method according to claim 1, wherein said secondary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

11. The method according to claim 1, wherein said second conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

12. The method according to claim 1, wherein said step (e) is executed by means of a reactive ion etching.

13. A structure of a thin film transistor comprising:

an insulating substrate;

a source/drain layer disposed on said insulating substrate;

a primary insulating layer disposed on said source/drain layer;

a primary gate disposed on said primary insulating layer;

a secondary insulating layer disposed on said primary insulating layer; and

a secondary gate disposed on said secondary insulating layer and insulated from said primary gate via said secondary insulating layer.

14. The structure according to claim 13, wherein said secondary insulating layer further comprises a first secondary insulating layer and a second secondary insulating layer.

15. The structure according to claim 14, wherein said secondary gate further comprises a first secondary gate and a second secondary gate disposed on said first secondary insulating layer and said second secondary insulating layer respectively.

16. The structure according to claim 13, wherein said insulating substrate is a glass.

17. The structure according to claim 13, wherein said source/drain layer is a high-doping semiconductor layer.

18. The structure according to claim 17, wherein said high-doping semiconductor layer is high-doping polycrystalline silicon.

19. The structure according to claim 13, wherein said source/drain layer comprises a drain, a channel and a source.

20. The structure according to claim 19, wherein said channel has a length equal to a sum of a length of said primary gate, a width of said secondary insulating layer, and a length of said secondary gate.

21. The structure according to claim 13, wherein said primary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

22. The structure according to claim 13, wherein said first conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

23. The structure according to claim 13, wherein said primary gate is formed by means of a reactive ion etching.

24. The structure according to claim 13, wherein said secondary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

25. The structure according to claim 13, wherein said second conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

26. The structure according to claim 13, wherein said secondary gate is formed by means of a reactive ion etching.

27. A structure of a thin film transistor comprising:

an insulating substrate;

a source/drain layer disposed on said insulating substrate;

a primary insulating layer disposed on said source/drain layer;

a primary gate disposed on said primary insulating layer;

at least a secondary insulating layer disposed on said primary insulating layer; and

at least a secondary gate disposed on said at least a secondary insulating layer and insulated from said primary gate via said at least a secondary insulating layer.

28. The structure according to claim 27, wherein said insulating substrate is a glass.

29. The structure according to claim 27, wherein said source/drain layer is a high-doping semiconductor layer.

30. The structure according to claim 29, wherein said high-doping semiconductor layer is high-doping polycrystalline silicon.

31. The structure according to claim 27, wherein said source/drain layer comprises a drain, a channel and a source.

32. The structure according to claim 31, wherein said channel has a length equal to a sum of a length of said primary gate, a width of said at least secondary insulating layer, and a length of said at least a secondary gate.

33. The structure according to claim 27, wherein said primary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

34. The structure according to claim 29, wherein said at least a secondary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

* * * * *