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(54) **FERROELECTRIC THIN FILM PROCESSING FOR FERROELECTRIC FIELD-EFFECT TRANSISTOR**

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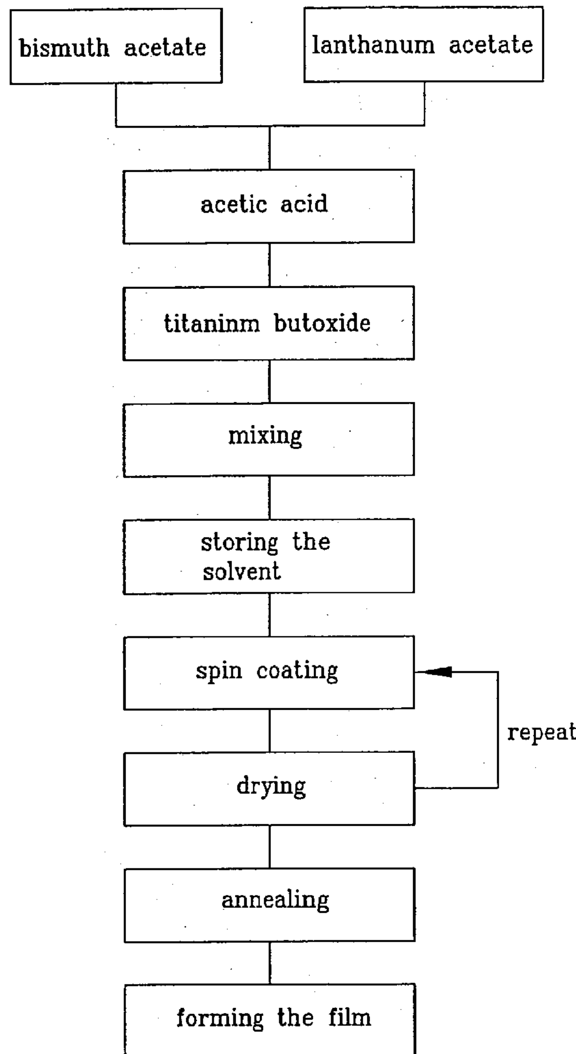
(57) **ABSTRACT**

The present invention relates to a method for manufacturing a ferroelectric field-effect transistor, particularly to a ferroelectric field-effect transistor with a metal/ferroelectric/insulator/semiconductor (MFIS) gate capacitor structure. The method comprises steps of depositing a bismuth layered ferroelectric film on the insulator buffered Si, after a high-temperature thermal treatment, depositing an upper electrode on the bismuth layered ferroelectric film.



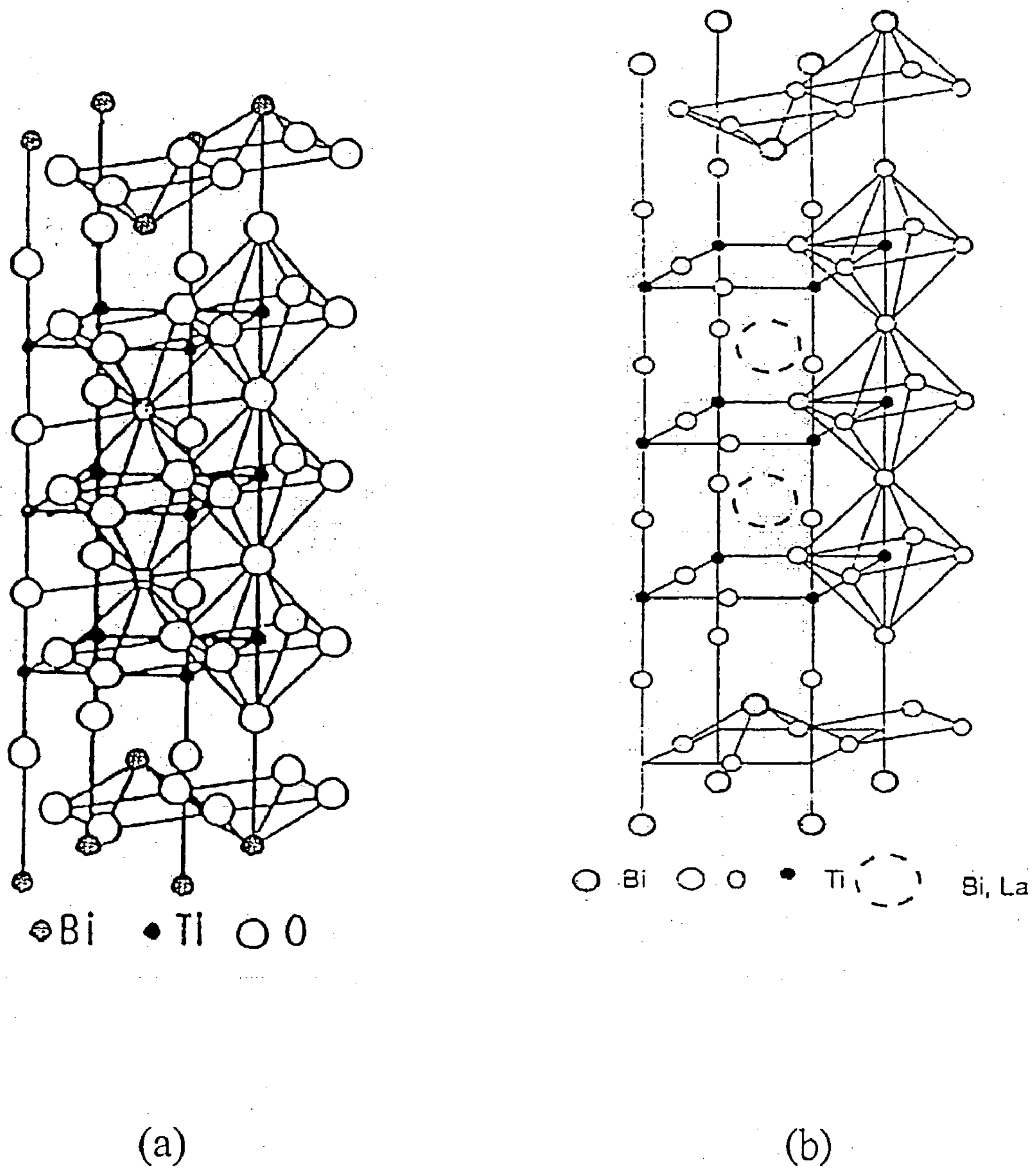


Fig. 1 (PRIOR ART)

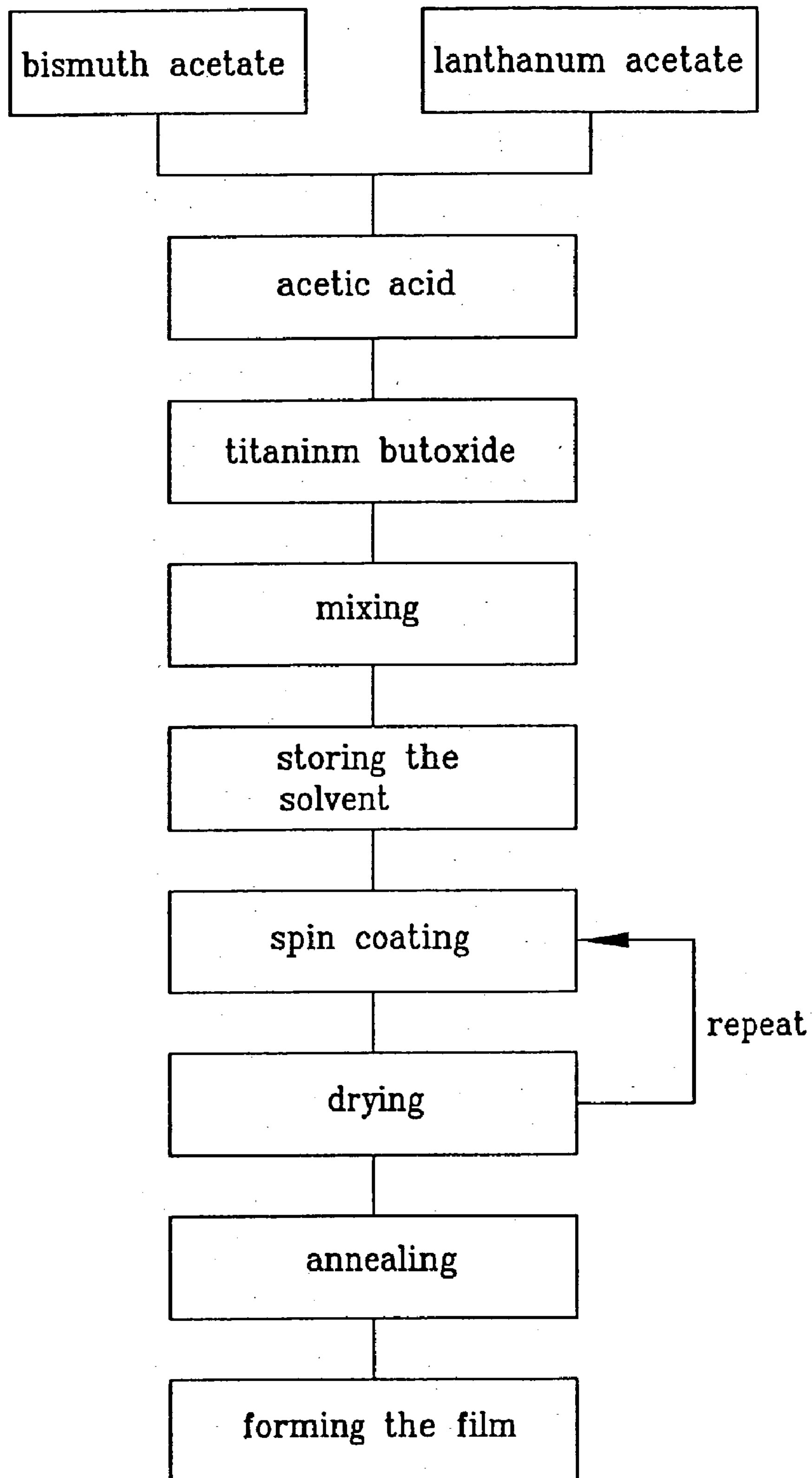
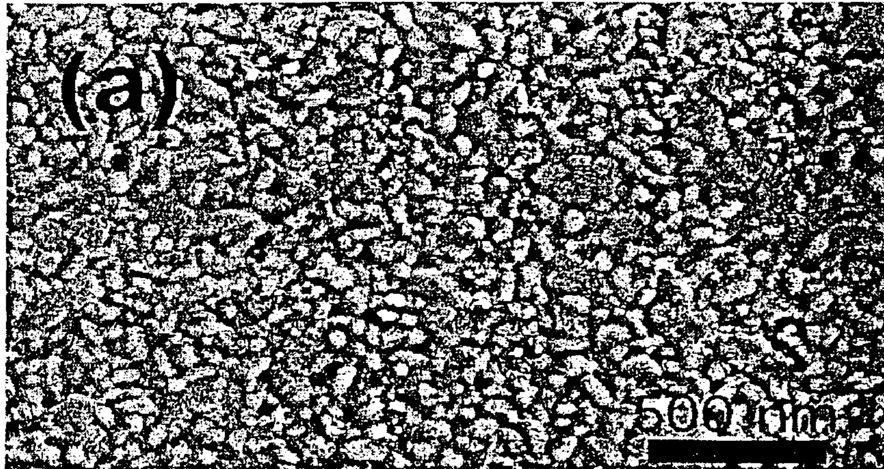


Fig. 2



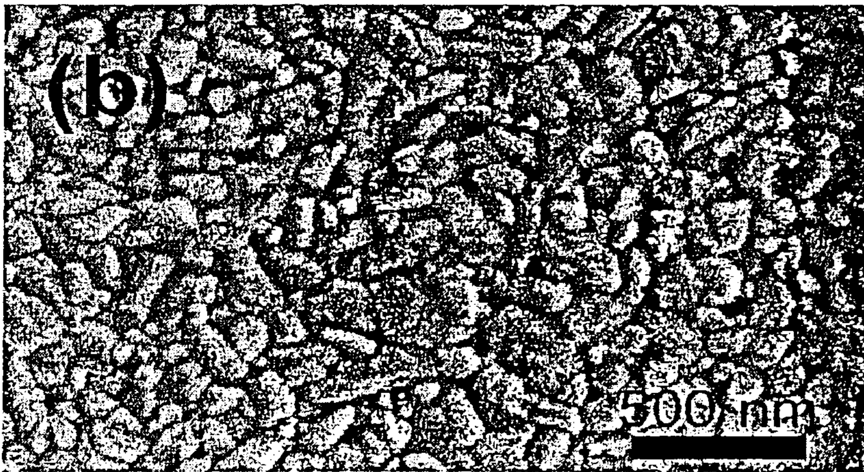


Fig. 3

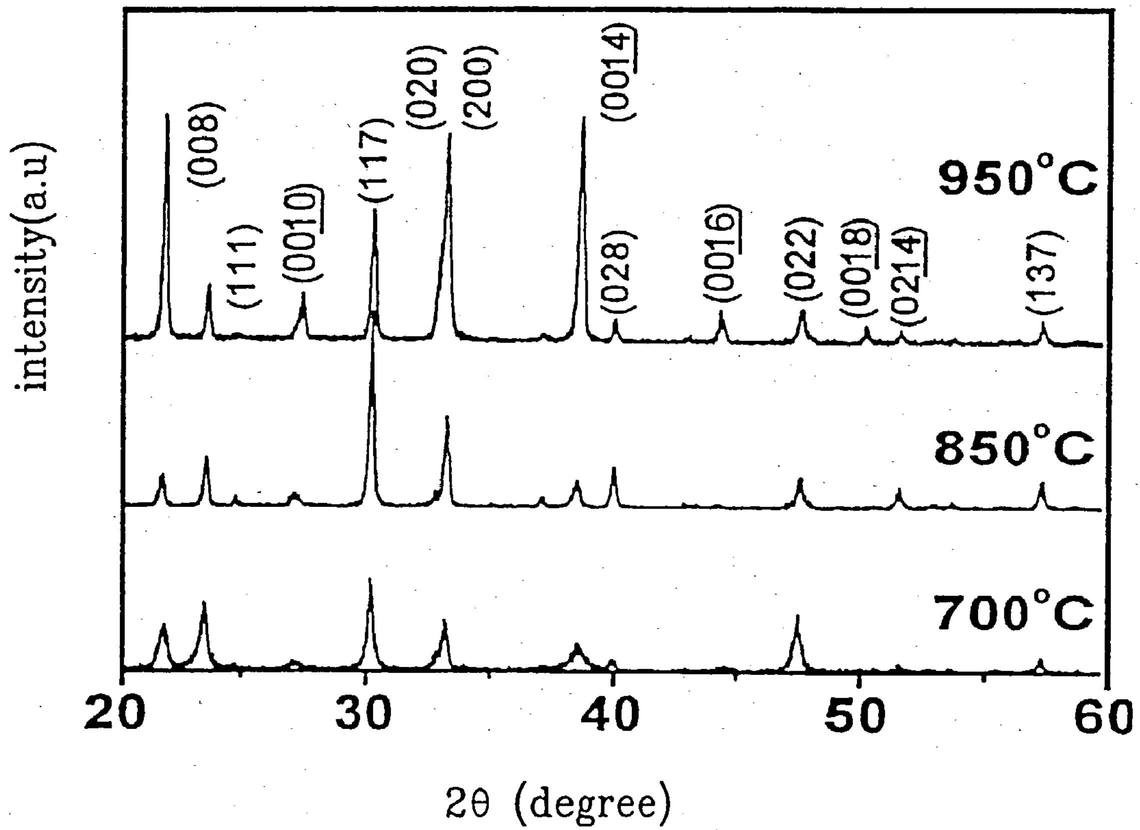


Fig. 4

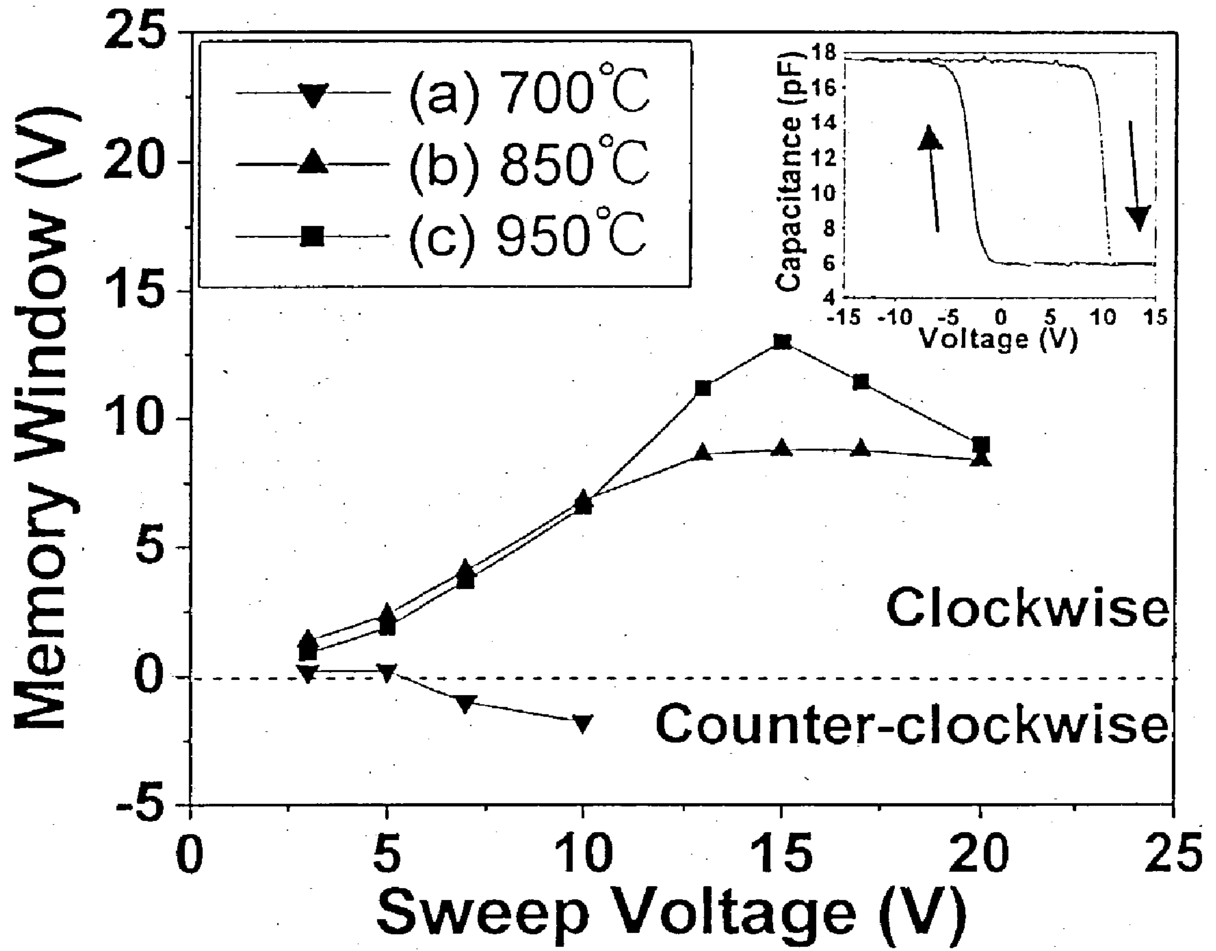


Fig. 5

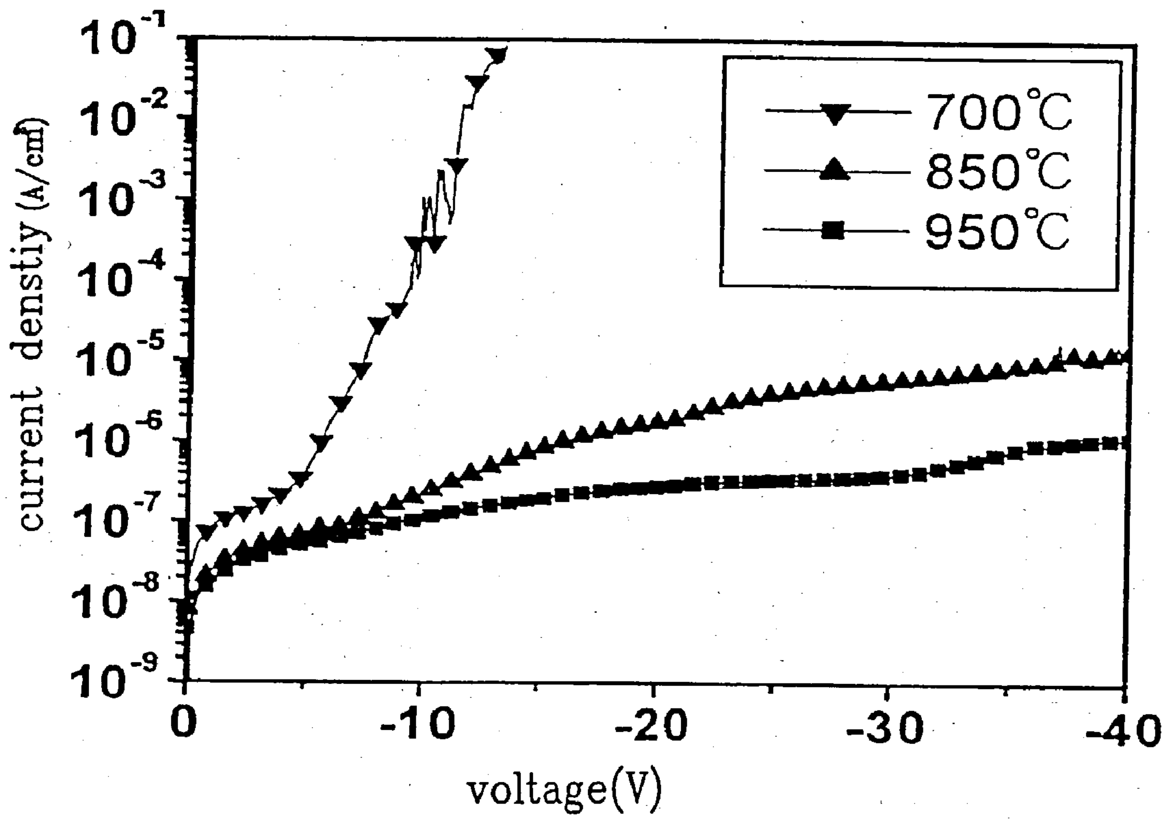


Fig. 6

FERROELECTRIC THIN FILM PROCESSING FOR FERROELECTRIC FIELD-EFFECT TRANSISTOR

FIELD OF THE INVENTION

[0001] The present invention relates to a method of manufacturing a semiconductor, and more particularly to a transistor with a metal/ferroelectric thin film/insulator/semiconductor (MFIS) gate capacitor structure.

BACKGROUND OF THE INVENTION

[0002] The present silicon memory devices can be sorted by the storage state of the data. One type of the silicon memory devices is the random access memory (RAM), such as DRAM and SRAM. This type of memory device with data reading/writing speed below several ten nanoseconds is generally called quick-access memory. However, the data saved therein will disappear while the power is shut down. Therefore, the storage state of the RAM is volatile. Another type is the read only memory (ROM), such as electrical erasable programmable read only memory (EEPROM) and flash memory. On the contrary, this type of memory device can save the data permanently but has longer reading/writing speed than the RAM. Because the data do not disappear while the power is shut down, the storage state of the RAM is nonvolatile.

[0003] Although the current memory devices all have high density (>64 Mbit), the important properties, non-volatility and quick speed, cannot be performed at the same time. Since the demand for ferroelectric random access memory (FRAM) consisting these two merits becomes urgent.

[0004] The FRAM has the same speed in reading/writing data with the conventional RAM, so it belongs to the quick-access memory. When writing data, the ferroelectric film is polarized permanently by a electrical pulse so that the data written in is saved forever even that the power is shut down. Therefore, the FRAM is a non-volatile memory device with quick and non-disappeared properties. Moreover, the design of ROM+RAM can be replaced by one FRAM and then the efficiency will be promoted greatly.

[0005] Principle of non-volatile ferroelectric memory device for application is using the polarization-electric field (P-E) hysteresis of the ferroelectric film. Because the ferroelectric film has remnant polarization while no external electric field exists, the data do not disappear when shutting down the power. In the practical application, the ferroelectric film capacitor replaces the storage capacitor of SiO_2 to distinct the logic "0" and "1" by different remnant polarization (Pr). When the logic is "0", adding a positive voltage has a difference between Pr and saturation polarization (Ps). While the logic is "1", the difference is between −Pr and Ps. The current of logic "1" is larger than that of logic "0" so that it is able to be used for determining the data logic.

[0006] In the development of the FRAM, how to combine the manufacture process of ferroelectric and silicon integrated circuit is a key point. Especially when the high density memory is developed, the ferroelectric capacitor formed on the gate of the metal oxide semiconductor field-effect transistor (MOSFET) is imperative, so the research in this aspect is extensively noted. In 1950~1960, scientists use the natural polarization of the ferroelectric ceramics to control (or change) the electric conduction coefficient on the surface of the semiconductor for producing the ferroelectric field-effect transistor memory. Recently, owing to the excellent characteristics of the ferroelectric film, and requirements of both high density G-bite DRAM and non-volatile memory devices so that the FRAM is noted and studied once again.

[0007] In view of foregoing reasons, the present invention provides the ultra-thin aluminum oxide to be the insulator for solving charge-injection problem and the material with bismuth layered perovskite structure to be the ferroelectric film due to its non-fatigue behavior and compatibility to the other high-temperature semiconductor process so that excellent memory characteristics can be reached in the MFIS stacked gate capacitor structure.

SUMMARY OF THE INVENTION

[0008] It is an object of the present invention to provide a production process for manufacturing a bismuth layered ferroelectric film on the ultra-thin aluminum oxide. The single ferroelectric field-effect transistor is produced by the process of the present invention having superior memory property which is due to the ferroelectricity of the ferroelectric film. By appropriately controlling the high-temperature process, the large memory window due to the ferroelectricity and low leakage current are observed in single ferroelectric transistor with a metal/ferroelectric/insulator/Si (MFIS) gate capacitor structure. The low leakage current density matches ULSI device requirement and further the high-temperature process is compatible with CMOS and other post-end semiconductor process.

[0009] It is another object of the present invention to provide a method for manufacturing a semiconductor applied to a ferroelectric memory device, including steps of providing an insulator, forming a bismuth ferroelectric film with bismuth layered perovskite structure on the insulator, wherein the bismuth is partially substituted by one of lanthanum and vanadium, treating the insulator and the bismuth ferroelectric thin film at a relatively high temperature, and plating a metal layer on the bismuth ferroelectric film.

[0010] Preferably, the insulator is aluminum oxide.

[0011] Preferably, the insulator further includes one selected from a group consisting of aluminates, silicides, zirconium oxides, bismuth oxides and a mixture thereof.

[0012] Preferably, the insulator is a gate dielectric layer having a relatively high dielectric constant.

[0013] Preferably, the insulator is formed by means of sputtering.

[0014] Preferably, the insulator is formed by means of metalorganic chemical vapor deposition (MOCVD).

[0015] Preferably, the insulator is formed by means of molecular beam epitaxy (MBE).

[0016] Preferably, the insulator is formed by means of jet vapor deposition (JVD).

[0017] Preferably, the insulator is formed by means of electron beam evaporation and following oxidation process.

[0018] Preferably, the bismuth ferroelectric film includes bismuth ion precursors, titanium ion precursors and one of lanthanum ion precursors and vanadium ion precursors.

[0019] Preferably, the bismuth ion precursors, titanium ion precursors and one selected from a group consisting of lanthanum ion precursors, vanadium ion precursors and the mixture thereof are at a molar ratio of (4−X):3:X (Bi^{3+}:Ti^{4+}:La^{3+}/V^{3+}), wherein 0<X<1.9.

[0020] Preferably, the bismuth layered ferroelectric film is formed by means of spin coating of a chemical solution.

[0021] Preferably, the chemical solution is one selected from a group consisting of bismuth acetate, lanthanum acetate, titanium n-butoxide and the mixture thereof dissolving in a mixing solvent of acetic acid and 2-methoxyethanol.

[0022] Preferably, the chemical solution includes an metallo-organic precursor and an organic solvent.

[0023] Preferably, the metallo-organic precursor is one selected from a group of bismuth, lanthanum and titanium with carbon chains, respectively.

[0024] Preferably, the organic solvent is used for dissolving said metallo-organic precursors.

[0025] Preferably, the organic solvent includes alcohols and carboxylic acids.

[0026] Preferably, the bismuth layered ferroelectric film is formed by means of sputtering.

[0027] Preferably, the bismuth layered ferroelectric film is formed by means of pulsed laser deposition (PLD).

[0028] Preferably, the bismuth layered ferroelectric film is formed by means of MOCVD.

[0029] Preferably, the relatively high temperature is ranged from 600 to 1000° C.

[0030] The above objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] **FIG. 1**(*a*) is a schematic diagram of bismuth titanate ceramic structure according to the prior art.

[0032] **FIG. 1**(*b*) is a schematic diagram of lanthanum substituted bismuth titanate ceramic structure according to the prior art.

[0033] **FIG. 2** is a flow chart of forming the lanthanum substituted bismuth titanate ferroelectric film.

[0034] **FIG. 3** is a surface image of lanthanum substituted bismuth titanate ceramics after thermal treatment at (a) 700° C. (b) 850° C. (c) 950° C.

[0035] **FIG. 4** is an X-ray diffraction diagram of lanthanum substituted bismuth titanate after thermal treatment at 700-950° C.

[0036] **FIG. 5** is a diagram showing memory window value vs. added potential of lanthanum substituted bismuth titanate ceramics with ferroelectic film/aluminum oxide insulator/silicon substrate structure after thermal treatment at 700-950° C.

[0037] **FIG. 6** is a diagram showing leakage current density vs. added voltage of lanthanum substituted bismuth titanate ceramics with ferroelectic film/aluminum oxide insulator/silicon substrate structure after thermal treatment at 700-950° C.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0038] In order to solve the charge injection problem, aluminum oxide layer is used to be the insulator. For testing the application of ferroelectric material in the present invention, the bismuth layer structured ferroelectric is considered and used as the ferroelectric material which chemical formula can be represented as $(Bi_2O_2)^{2+}(A_{m-1}B_mO_{3m+1})^{2+}$. The present invention takes $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (m=3) for example, $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) is used to be the material and produce the capacitor having BLT/Al_2O_3/Si MFIS structure.

[0039] Preparation of Buffer Layer

[0040] After dealing silicon substrate cleaned with RCA and treated by hydrofluoric acid vapor, then the metal aluminum is deposited on the surface of the silicon substrate in the electron beam evaporation system to form a metal film with several ten nanometer thereon. After thermal oxidation at 900° C., the aluminum film converts to the aluminum oxide film with thickness below 10 nm.

[0041] Preparation of Chemical Solution

[0042] Take BLT ($Bi_{4-X}La_XTi_3O_{12}$) for example, dissolving bismuth acetate, lanthanum acetate and titanium n-butoxide in acetic acid and 2-methoxythanol mixture, the molar ratio of Bi^{3+}:La^{3+}:Ti^{4+} is (4−X):X:3, wherein 0<X<1.9. After the chemical solution is clear, the chemical solution must be stirred at least ten hours to carry out the hydrolysis condensation of the different metallo-organic precursors.

[0043] Preparation of Ferroelectric Film

[0044] The synthesized chemical solution is spin coated uniformly on the silicon substrate having the insulator thereon by means of rotary plating in 4000 rpm for 30 seconds. After each step of plating gel, the silicon substrate have to remove the organic solvent on hot plate at 400° C. Repeat the above-mentioned steps of coating and drying several times and then raise the temperature to the desired temperature in oxygen atmosphere. Keep the temperature one hour so as to finish the thermal treatment.

[0045] FIGS. **1**(*a*) and **1**(*b*) display the structures of bismuth titanate ceramics ($Bi_4Ti_3O_{12}$) and lanthanum substituted bismuth titanate ceramics ($Bi_{4-X}La_XTi_3O_{12}$), respectively. As shown in **FIG. 1**(*a*), bismuth titanate ceramics have bismuth layered perovskite structure ($(Bi_2O_2)^{2+}(A_{m-1}B_mO_{3m+1})^{2+}$). As shown in **FIG. 1**(*b*), according to the prior art, the A-sites in the bismuth layered perovskite structure are occupied by lanthanum. Furthermore, because the stability of the lanthanum substituted bismuth layered perovskite structure is improved and the antiphase boundary is formed easily, the BLT ferroelectric film is non-fatigue on the noble metal electrode.

[0046] **FIG. 2** is a flow chart showing how to form the BLT ferroelectric film, wherein the statement is the same with preparation of chemical solution in above section. The precursors capable to synthesize the chemical solution are not only the example mentioned therein but also the bis-

muth, lanthanum and titanium precursors with various carbon chains. The organic solvents used for dissolving the metallo-organic precursors further includes alcohols, carboxylic acids and other organic solvent. Because the metal bismuth has high vapor pressure and evaporates easily, it is necessary to increase the content about 10%. In addition, the chemical solution can be added various chelating agents, e.g. glycerol, or other solvents to adjust the chemical solvent. The chelating agent can adjust the degree of hydrolysis condensation between molecules in the chemical solution or the bonding state between metal ions and organic molecules around the metal ions. Adding the chelating agent can directly influence crystallization temperature and the grain size of the ferroelectric film. Moreover, the thermal treatment condition can be referred to the results of thermal analysis, and carried out in the different atmosphere, such as NO or N_2O, and different temperature during different time period, even by means of rapid thermal annealing (RTA) or other energy resources.

[0047] **FIG. 3** is surface image of lanthanum substituted bismuth titanate ferroelectric film after thermal treatment at 700-950° C. As shown in **FIG. 3**, the ferroelectric film formed by means of chemical solution deposition is very smooth and has no cracks. The crystalline size of BLT ferroelectric film are increasing with the increasing temperature, besides, there are many plate-shaped grain having a size over 500 nm. This may relates to the preferred orientation of BLT at high temperature shown in the X-ray diffraction diagram of **FIG. 4**.

[0048] **FIG. 4** is the X-ray diffraction diagram of the BLT ferroelectric film after thermal treatment at 700-950° C. Comparing with the well-known SBT ($SrBi_2Ta_2O_9$) film, the temperature for forming the layered perovskite structure of the BLT film is lower about 150° C. The BLT film will form the layered perovskite structure at 700° C. rather than the second phase, and the strongest diffraction peak is (117). With the increasing temperature at 950° C., (008) and (0014) become the strongest diffraction peaks and still no second phase existed. Therefore, after thermal treatment at relatively high temperature, the BLT film has no changes in the structure and obviously has the preferred orientation at 950° C.

[0049] **FIG. 5** is the diagram showing memory window value vs. external applied voltage of the MFIS capacitor with BLT/Al_2O_3/Si structure after thermal treatment at 700-950° C. As measuring the high frequency capacitance versus applied voltage for MFIS capacitor with p-type Si substrate, the obtained hysteresis curve in clockwise direction (the curve in the region up to the dotted line shown in **FIG. 5**) represents that the memory property results from the ferroelectric property of the ferroelectric film, and the opening of the memory window in the upper region of **FIG. 5** is defined as positive. On the contrary, when the hysteresis curve presents the counterclockwise direction, that indicates that the memory property results from the charge-injection effect and the opening of the memory window in the region under the dotted line of **FIG. 5** is defined as negative. According to **FIG. 5**, the memory window value of the ferroelectric effect is not good after thermal treatment the capacitor with BLT/Al_2O_3/Si structure at 700° C. When increasing applied voltage, the charge-injection effect still makes the hysteresis curve turn to negative. However, when the temperature of thermal treatment increases to 850° C., obviously, the memory window property results from ferroelectric effect. Even if the operating potential is over ±20 V, the memory window property is not of inferior quality, especially when the temperature of thermal treatment increases to 950° C., adding ±15 V can obtain the memory window property over 13 V. That is to say, when raising the temperature of thermal treatment, the obtained property of BLT/Al_2O_3/Si capacitor structure becomes more superior.

[0050] **FIG. 6** is the leakage current density vs. added voltage diagram of MFIS capacitor with BLT/Al_2O_3/Si structure after thermal treatment at 700-950° C. According to **FIG. 6**, when the temperature of thermal treatment is 700° C., the leakage current density is 4.7×10^{-7} A/cm^2 at potential of −100 kV/cm and similar to the leakage current density of vanadium-doped $Bi_4Ti_3O_{12}$, but the leakage current is still highest at relatively lower temperature among various annealing conditions. With increasing temperature, the curve of current density vs. applied voltage is gradually down, when the temperature is 950° C., the leakage current at −100 kV/cm is smaller than that at 700° C. by three grades of magnitude. Therefore, with increasing the temperature of thermal treatment, the leakage current density is much reduced and due to the reduction of the charge injection, the memory effect of ferroelectric property still maintains 8 V even when the added potential is ±20 V.

[0051] While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. A method for manufacturing a semiconductor applied to a one-transistor ferroelectric memory device, comprising steps of:

providing an insulator;

forming a bismuth ferroelectric film with bismuth layered perovskite structure on said insulator, wherein said bismuth is partially substituted by one of lanthanum and vanadium;

treating said insulator and said bismuth ferroelectric film at a relatively high temperature; and

depositing a metal upper electrode layer on said bismuth ferroelectric film.

2. The method according to claim 1 wherein said insulator is aluminum oxide.

3. The method according to claim 2 wherein said insulator further comprises one selected from a group consisting of aluminates, silicides, zirconium oxides, bismuth oxides and a mixture thereof.

4. The method according to claim 3 wherein said insulator is a gate dielectric layer having a relatively high dielectric constant.

5. The method according to claim 1 wherein said insulator is formed by means of sputtering.

6. The method according to claim 1 wherein said insulator is formed by means of metalorganic chemical vapor deposition (MOCVD).

7. The method according to claim 1 wherein said insulator is formed by means of molecular beam epitaxy (MBE).

8. The method according to claim 1 wherein said insulator is formed by means of jet vapor deposition (JVD).

9. The method according to claim 1 wherein said insulator is formed by means of electron beam evaporation and following oxidation process.

10. The method according to claim 1 wherein said bismuth ferroelectric film comprises bismuth ion precursors, titanium ion precursors and one of lanthanum ion precursors and vanadium ion precursors.

11. The method according to claim 8 wherein said bismuth ion precursors, titanium ion precursors and one selected from a group consisting of lanthanum ion precursors, vanadium ion precursors and the mixture thereof are at a molar ratio of (4−X):3:X (Bi^{3+}:Ti^{4+}:La^{3+}/V^{3+}), wherein 0<X<1.9.

12. The method according to claim 1 wherein said bismuth layered ferroelectric film is formed by means of spin coating of a chemical solution.

13. The method according to claim 10 wherein said chemical solution is one selected from a group consisting of bismuth acetate, lanthanum acetate, titanium n-butoxide and the mixture thereof dissolving in a mixing solvent of acetic acid and 2-methoxyethanol.

14. The method according to claim 10 wherein said chemical solution comprises an metallo-organic precursor and an organic solvent.

15. The method according to claim 12 wherein said metallo-organic precursor is one selected from a group of bismuth, lanthanum and titanium with carbon chains, respectively.

16. The method according to claim 12 wherein said organic solvent is used for dissolving said metallo-organic precursors.

17. The method according to claim 14 wherein said organic solvent comprises alcohols and carboxylic acids.

18. The method according to claim 1 wherein said bismuth layered ferroelectric film is formed by means of sputtering.

19. The method according to claim 1 wherein said bismuth layered ferroelectric film is formed by means of pulsed laser deposition (PLD).

20. The method according to claim 1 wherein said bismuth layered ferroelectric film is formed by means of MOCVD.

21. The method according to claim 1 wherein said relatively high temperature is ranged from 600 to 1000° C.

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