# SiGe HBT's Small-Signal Pi Modeling

Tian-Ren Yang, Julius Ming-Lin Tsai, Chih-Long Ho, and Robert Hu

***Abstract*—This paper presents the derivation procedure used in determining the parameters in SiGe HBT's small-signal model where the Pi circuit configuration is employed. For both the transistor's external base–collector capacitor and its base spreading resistor, new close-form expressions have been derived. Comparisons with existing approaches vindicate the feasibility and effectiveness of our formulations. With the impact of the lossy substrate effectively modeled and the frequency dependency of the transconductance properly addressed, this proposed extraction approach demonstrates accurate results up to 30 GHz with different bias conditions.**

***Index Terms*—Base spreading resistor, HBT, Pi model, SiGe.**

## I. Introduction

FOR THE small-signal modeling of an HBT, either Tee or Pi circuit configuration can be used [1]–[5]. Though the Tee circuit reflects the device-physics aspect of this transistor, the Pi circuit in general provides better insight into designing circuits [6], [7] and, thus, will be explored in this paper. As shown in Fig. 1, the SiGe HBT's Pi model consists of the intrinsic transistor, which is enclosed by the dotted box, the base spreading resistor $R_{bb}$, the lossy substrate network $C_{\rm sub1}$, $C_{\rm sub2}$, and $R_{\rm sub}$[8]–[10], the external parasitic capacitor $C_{\rm ext}$, the base, emitter, and collector resistors $R_b$, $R_e$, and $R_c$, and the input and output pad capacitors $C_{\rm pad1}$ and $C_{\rm pad2}$. Two time constants $\tau_1$ and $\tau_2$ are added on to the transconductance $G_m$ to account for its magnitude and phase frequency dependency [5], [11]–[15]. Output impedance of this voltage-induced current source is assumed infinite. As is well known, one challenge in SiGe HBT's small-signal Pi modeling comes from the presence of $R_{bb}$, whose location between $C_{\rm ext}$ and the intrinsic transistor makes the reliable derivation of both $C_{\rm ext}$ and $R_{bb}$, so far, largely by way of additional test structures or numerically [3], [16]–[19]. In this paper, proper close-form expressions for these two parameters have been worked out and will be compared with existing approaches [20]–[22].

Fig. 2 shows the HBT under test, which is fabricated using a commercial 0.35-$\mu$m SiGe–BiCMOS process and has bulk resistivity of 8 $\Omega \cdot$ cm for the substrate. The base poly resistance is 200 $\Omega$/square, while the silicided base poly for inter-connection has a much lower resistance of a few $\Omega$/square. The emitter layout consists of four fingers, with each 5.1-$\mu$m long. Two-port short, open, load, and thru (SOLT) calibration is performed using 100-$\mu$m Cascade probes on the ceramic substrate provided by the same vendor. With the Agilent network analyzer's output power set to $-10$ dBm, losses due to the additional cables and bias-Ts' will pull the power level down by 0.2 dB/GHz. DC bias for this transistor comes from HP4142B modular dc source/monitor. The 30-GHz upper frequency is mainly determined by the available frequency range of the coaxial cables used in the measurement.

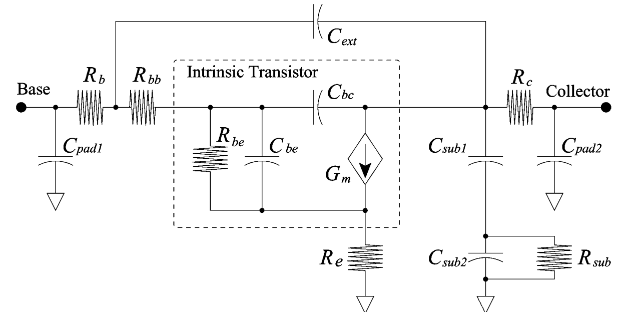


Fig. 1. HBT's small-signal Pi model where the substrate network consists of $C_{\rm sub1}$, $C_{\rm sub2}$, and $R_{\rm sub}$. Transconductance $G_m$ is set to $G_{m0}e^{-j\omega\tau_1}/(1+j\omega\tau_2)$.

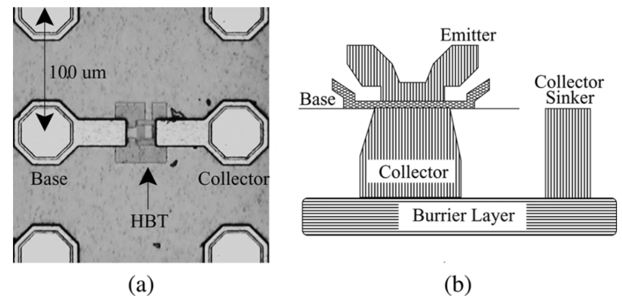


Fig. 2. SiGe HBT under test. (a) Photograph. (b) Schematic of the transistor where the emitter is connected to ground, the base is the input, and the collector is the output.

## II. HBT Small-Signal Pi Modeling

### A. *Determination of $C_{\rm pad1}$, $C_{\rm pad2}$, $R_b$, $R_e$, and $R_c$*

Fig. 3 shows the flowchart in determining the transistor's small-signal parameters. To find out the parasitics of the input and output pads, an open-pad test structure is designed where the transistor itself has been removed. Frequency-independent capacitance can, therefore, be obtained as $C_{\rm pad1} = 43$ fF, $C_{\rm pad2} = 46$ fF. The measured cross-coupling capacitance between input and output is three orders less and can be neglected. Using an appropriate deembedding procedure, these capacitors can be removed from the transistor's model. Since $R_b$, $R_e$,

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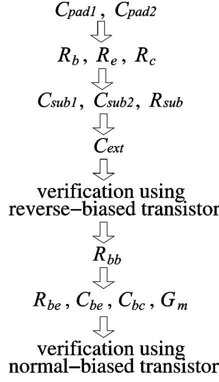


Fig. 3. Flowchart for the determination of the transistor's small-signal parameters.

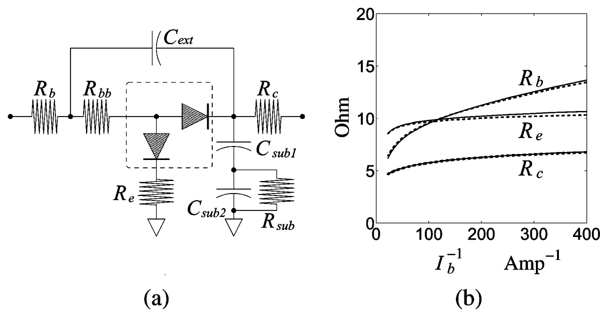


Fig. 4. Saturated HBT for the determination of $R_b$, $R_e$, and $R_c$. (a) Schematic. (b) By extrapolating the measured resistance to those corresponding to infinite base current, we have $R_b = 7.5\ \Omega$, $R_e = 4.1\ \Omega$, and $R_c = 4.3\ \Omega$. The solid curves are measured at 2 GHz; the dashed ones are at 5 GHz.

and $R_c$ are beneath the first-layer metal, they are beyond the reach of a short-circuit test structure, but can be determined by forcing the transistor into saturation [23]. By setting the current flowing out of the collector to be half of the base current, we slowly increase the base current and voltage, from 1 and 18.8 mV, respectively, to 11 and 95 mV, respectively. Since this saturated intrinsic transistor can now be modeled as two conducting diodes, as shown in Fig. 4(a), a Tee circuit configuration, especially at low frequency, emerges. By extrapolating the measured resistance to that corresponding to infinite base current, we have the frequency-independent $R_b$, $R_e$, and $R_c$ equal to 7.5, 4.1, and 4.3 $\Omega$, respectively, as illustrated in Fig. 4(b). Here, the solid curves are those corresponding to 2 GHz, and the dashed curves are for 5 GHz. The impacts of both $R_b$ and $R_c$ on the transistor's Pi model are ready to be removed now; $R_e$, however, will be temporarily retained for the determination in Section II-B of the substrate network.

### B. Determination of Substrate Network

Though mathematically the substrate network can be decided when the transistor is in saturation, the small in-parallel $R_e$ renders the derived substrate parameter values highly susceptible to measurement uncertainties. Reliable results can be obtained by reverse-biasing the transistor. With $V_c = 0$ V, $I_c = -1.019 \cdot 10^{-2}\ \mu$A, $V_b = -1.05$ V, and $I_b = -2.22 \cdot 10^{-2}\ \mu$A,

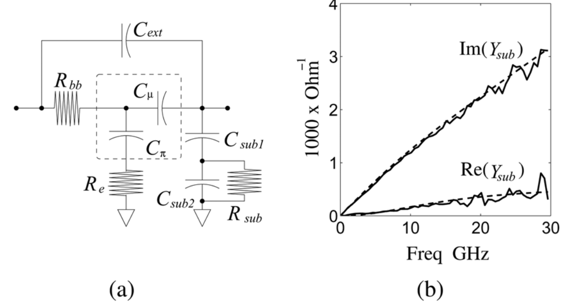


Fig. 5. Reverse-biased HBT for the determination of substrate network. (a) Schematic. (b) Measured and simulated substrate admittance $Y_{\rm sub}$ versus frequency. The solid curves are the measured results; the dashed curves are the simulated ones with $C_{\rm sub1} = 21.4$ fF, $C_{\rm sub2} = 57.5$ fF, and $R_{\rm sub} = 128\ \Omega$.

the reverse-biased intrinsic transistor resembles two separate capacitors, as shown in Fig. 5(a). As far as $Y_{22}$ and $Y_{12}$ are concerned, port 1 on the left of the schematic can be connected to ground and the signal is injected into port 2 on the right. If $R_{bb}$ is much smaller than the impedance of the series $C_\pi R_e$ circuit, then most of the current passing through $C_\mu$ from port 2 will flow down the $R_{bb}$ branch rather than the $C_\pi R_e$ branch. By treating this $C_\pi R_e$ as open circuit, we then have $Y_{\rm sub} = Y_{22} + Y_{12}$, where

$$Y_{\rm sub} = j\omega C_{\rm sub1} + \frac{1}{j\omega C_{\rm sub2} + \dfrac{1}{R_{\rm sub}}}. \tag{1}$$

Since the complex-number $Y_{22} + Y_{12}$ can provide only two constraints at each frequency point, analytical solutions (of genuinely frequency independent) for the three parameters constructing the substrate network cannot be obtained; rather, numerical algorithms need to be used. As

$$\frac{-1}{\omega} \frac{{\rm Re}\left[\dfrac{1}{(Y_{22} + Y_{12})}\right]}{{\rm Im}\left[\dfrac{1}{(Y_{22} + Y_{12})}\right]} = C_{\rm sub1} R_{\rm sub} \tag{2}$$

and

$$\omega^2 \frac{C_{\rm sub1} R_{\rm sub}}{{\rm Re}\,(Y_{22} + Y_{12})} = \frac{1}{C_{\rm sub1}} \left[1 + \omega^2 \left(C_{\rm sub1} + C_{\rm sub2}\right)^2\right]. \tag{3}$$

Least squares fit over the whole frequency range then gives $C_{\rm sub1} = 21.4$ fF, $C_{\rm sub2} = 57.5$ fF, and $R_{\rm sub} = 128\ \Omega$, respectively. Fig. 5(b) shows the admittance of the substrate network. Here, the solid curves are the measured results; the overlapping dashed curves are their simulated counterparts. Of course, other similar formulations can also be employed for the derivation of $C_{\rm sub1}$, $C_{\rm sub2}$, and $R_{\rm sub}$ [9], [10]. If only series [24], or parallel, $RC$ circuit is used to model the substrate network, close-form analytical expressions can indeed be written, but the resulting parameters will be highly frequency dependent and, thus, are not useful.

### C. Determination of $C_{\rm ext}$

With both the substrate network and $R_e$ readily removed from the schematic of the reverse-biased transistor, analytical

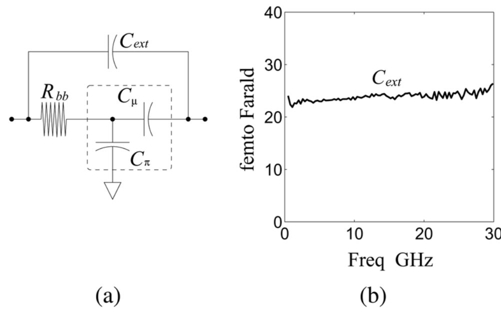


Fig. 6. Reverse-biased HBT where the substrate network and $R_e$ in the previous schematic have been deembedded for the purpose of determining $C_{\rm ext}$. (a) Schematic. (b) Measured $C_{\rm ext}$ versus frequency.

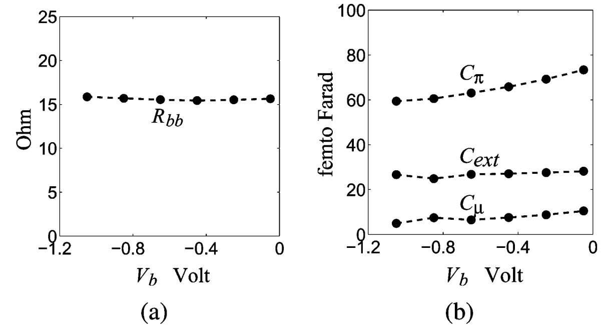


Fig. 7. Parameter values of the reverse-biased transistor with different base voltages. (a) $R_{bb}$ versus $V_b$ where the circle markers are the derived results. (b) $C_\pi$, $C_{\rm ext}$, and $C_\mu$ versus $V_b$.

solutions for the remaining circuit components, as shown in Fig. 6(a), can be obtained once $Y_{11}$ and $Y_{12}$ are known where

$$Y_{11} = j\omega C_{\rm ext} + \left[R_{bb} + \frac{1}{j\omega\left(C_\pi + C_\mu\right)}\right]^{-1}$$
$$Y_{12} = -j\omega C_{\rm ext} - \frac{C_\mu}{C_\mu + C_\pi} \cdot \left[R_{bb} + \frac{1}{j\omega\left(C_\pi + C_\mu\right)}\right]^{-1}. \quad (4)$$

By defining $H$ as

$$H = \frac{1}{Y_{11} + Y_{12}} = \left[R_{bb} + \frac{1}{j\omega\left(C_\pi + C_\mu\right)}\right] \frac{C_\mu + C_\pi}{C_\pi} \quad (5)$$

we have

$$C_\pi = \frac{-1}{\omega \cdot {\rm Im}(H)}$$
$$R_{bb} = \frac{1}{{\rm Re}\left(Y_{11}\right)} \left[\frac{{\rm Re}\left(H\right)}{|H|}\right]^2$$
$$C_\mu = \left[1 - \frac{{\rm Re}(Y_{11}) \cdot |H|^2}{{\rm Re}(H)}\right] \frac{1}{\omega \cdot {\rm Im}(H)}. \quad (6)$$

If the admittance matrix of the $R_{bb}$, $C_\pi$, and $C_\mu$ sub-circuit is designated as $[Y']$, then

$$[Y] - [Y'] = j\omega C_{\rm ext} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (7)$$

and, thus,

$$C_{\rm ext} = \frac{1}{\omega} \cdot {\rm Im}\left[R_{bb} + \frac{1}{j\omega\left(C_\mu + C_\pi\right)} - Y_{11}\right]. \quad (8)$$

The measured results are $C_\pi = 59.4$ fF, $R_{bb} = 14.5\ \Omega$, $C_\mu = 4.9$ fF, and as shown in Fig. 6(b), $C_{\rm ext} = 26$ fF. The three other $C_{\rm ext}$ expressions derived using (7) also give the same value. If we change the base voltage while keeping the collector node grounded, different reverse-biased parameter values can be obtained, as illustrated in Fig. 7, where both $R_{bb}$ and $C_{\rm ext}$ are independent of the base voltage in this reverse-biased condition. Now, the impact of $C_{\rm ext}$ on the transistor's Pi model can be removed, i.e., deembedded.

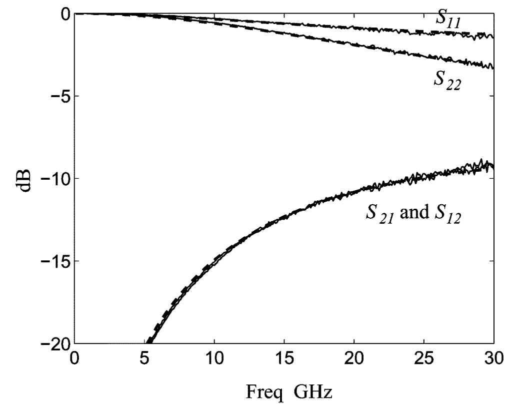


Fig. 8. Measured and simulated $S$-parameters of the reverse-biased HBT. The solid curves are the measured results; the overlapping dashed curves are their simulated counterparts.

In the conventional approach using IC-CAP, detailed layout information, dc capacitance measurement, and numerical fine tuning have to be employed for the determination of $C_{\rm ext}$ (and $C_{bc}$). Besides, it postulates that $C_{\rm ext}$ has to be independent of frequency. Recently, an analytical formulation for $C_{\rm ext}$ of a normal-biased transistor has been proposed [20]. However, the extensive use of least squares fits makes it to a large degree resemble a numerical approach. In our case, $C_{\rm ext}$ at each frequency point can be directly calculated and compared. Indeed, as demonstrated in Section II-D on $R_{bb}$, sometimes more than one analytical solutions can be written for a certain parameter; however, not all of them render the same result over the intended frequency range.

Figs. 8 and 9 show the $S$-parameters of the reverse-biased transistor. Here, the solid curves are the measured results; the overlapping dashed curves are their simulated counterparts. Bias condition and the component values used in the simulation are tabulated in Table I.

### D. Determination of Normal-Biased $R_{bb}$

Now, with the bias of the transistor being set at $V_c = 2$ V, $I_c = 6.9$ mA (current density $1.13\ {\rm mA}/\mu{\rm m}^2$), $V_b = 0.95$ V, and

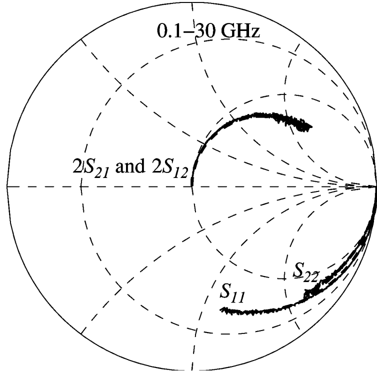


Fig. 9. Measured (solid) and simulated (dashed) $S$-parameters of the reverse-biased HBT on the Smith chart.

TABLE I
REVERSE-BIASED TRANSISTOR

| $V_c$ = 0Volt | $I_c$ = -10.19nA | $V_b$ = -1.05Volt | $I_b$ = -22.2nA |
|---|---|---|---|
| $R_{bb}$ = 14.5Ω | $C_\pi$ = 59.4fF | $C_\mu$ = 4.9fF | $C_{ext}$ = 26fF |
| $R_b$ = 7.5Ω | $R_c$ = 4.3Ω | $C_{pad1}$ = 43fF | $C_{pad2}$ = 46fF |
| $R_e$ = 4.1Ω | $R_{sub}$ = 128Ω | $C_{sub1}$ = 21.4fF | $C_{sub2}$ = 57.5fF |

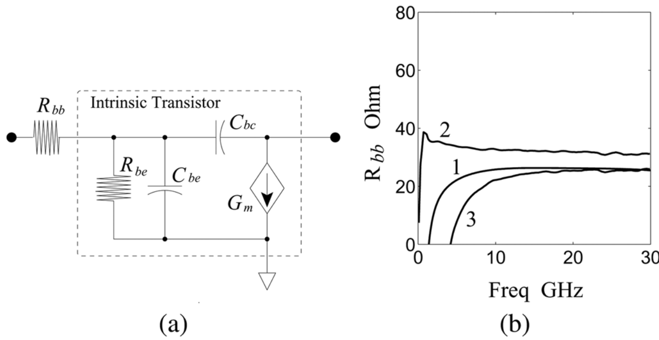


Fig. 10. $R_{bb}$ and the normal-biased intrinsic transistor. (a) Schematic. (b) Measured $R_{bb}$ where curve 1 is derived using (11), curve 2 is using (12), and curve 3 is using the algorithm suggested in [20].

$I_b = 58.4\ \mu$A, the normal-biased $R_{bb}$, as shown in Fig. 10(a), can be determined when both $Y_{11}$ and $Y_{12}$ are known. As

$$Y_{11} = \left[R_{bb} + \frac{1}{j\omega\left(C_{be}+C_{bc}\right)+\frac{1}{R_{be}}}\right]^{-1}$$
$$Y_{12} = -j\omega C_{bc}\cdot\left[1+\frac{R_{bb}}{R_{be}}+j\omega\left(C_{bc}+C_{be}\right)R_{bb}\right]^{-1} \tag{9}$$

i.e.,

$$\frac{Y_{11}}{Y_{12}} = \left[j\omega\left(C_{be}+C_{bc}\right)+\frac{1}{R_{be}}\right]\cdot\frac{j}{\omega C_{bc}} \tag{10}$$

therefore,

$$R_{bb} = \mathrm{Re}\left(\frac{1}{Y_{11}}\right)+\frac{1}{\omega(C_{be}+C_{bc})R_{be}}\cdot\mathrm{Im}\left(\frac{1}{Y_{11}}\right)$$
$$= \mathrm{Re}\left(\frac{1}{Y_{11}}\right)-\frac{\mathrm{Im}\left(\frac{Y_{11}}{Y_{12}}\right)}{\mathrm{Re}\left(\frac{Y_{11}}{Y_{12}}\right)}\cdot\mathrm{Im}\left(\frac{1}{Y_{11}}\right). \tag{11}$$

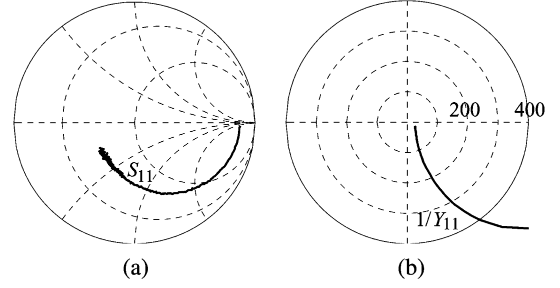


Fig. 11. $S_{11}$ and $1/Y_{11}$ curves used in deriving $R_{bb}$. (a) $S_{11}$ used for the extrapolation of (16) from 0.1 to 30 GHz. (b) $1/Y_{11}$ used for the extrapolation of (17) from 0.5 to 30 GHz. Both curves move clockwise as frequency increases.

On the other hand, if the transconductance can be treated as a real number, we can also express $R_{bb}$ in terms of $Y_{11}$ and $Y_{21}$[21], i.e.,

$$R_{bb} = \mathrm{Re}\left(\frac{1}{Y_{11}}\right)+\frac{1}{\omega(C_{be}+C_{bc})R_{be}}\cdot\mathrm{Im}\left(\frac{1}{Y_{11}}\right)$$
$$= \mathrm{Re}\left(\frac{1}{Y_{11}}\right)-\frac{\mathrm{Re}\left(\frac{Y_{21}}{Y_{11}}\right)}{\mathrm{Im}\left(\frac{Y_{21}}{Y_{11}}\right)}\cdot\mathrm{Im}\left(\frac{1}{Y_{11}}\right) \tag{12}$$

with

$$Y_{21} = \frac{-G_m}{R_{bb}}\left[\frac{1}{R_{bb}}+j\omega(C_{be}+C_{bc})+\frac{1}{R_{be}}\right]^{-1} \tag{13}$$

and

$$\frac{Y_{21}}{Y_{11}} = G_m\cdot\frac{j\omega(C_{be}+C_{bc})-\frac{1}{R_{be}}}{\omega^2(C_{be}+C_{bc})^2+\frac{1}{R_{be}^2}}. \tag{14}$$

Here, the current flowing through $G_m$ needs to be assumed much larger than that on the $C_{bc}$ branch. Fig. 10(b) displays the derived $R_{bb}$ where curve 1 comes from our proposed (11), the upper bound curve 2 is from (12), and the somehow lower bound curve 3 is using the algorithm suggested in [20]. The discrepancy between these three curves instigates a further numerical survey as follows.

As suggested in the IC-CAP user's manual, by assuming the transconductance to be a real number $G_{m0}$ and

$$\frac{1}{\omega C_{bc}} \gg Z_0$$
$$R_{be} \gg \frac{1}{\omega C_{be}}$$
$$G_m Z_0 \gg |1+j\omega C_{bc}Z_0| \tag{15}$$

then the input impedance (with 50-Ω output loading) can be expressed as

$$Z_{\mathrm{in}} \approx R_{bb}+\frac{1}{j\omega\left(C_{be}+G_{m0}Z_0C_{bc}\right)}. \tag{16}$$

Extrapolation of the corresponding $S_{11}$ contour on the Smith chart to infinite frequency results in a $R_{bb}$ of 25 Ω, as illustrate in Fig. 11(a). Alternatively, by assuming $R_{be}$ to be much larger

than the impedance of $C_{be}$ at high enough frequency, the intended $R_{bb}$ can be obtained by extrapolating the $1/Y_{11}$ curve to the $X$-axis [22], as

$$\frac{1}{Y_{11}} \approx R_{bb} + \frac{1}{j\omega\left(C_{be} + C_{bc}\right)}. \tag{17}$$

In Fig. 11(b), this $R_{bb}$ is around 25 Ω. Both numerical approaches, therefore, confirm our analytical method.

Regarding the derivation of $R_{bb}$, though the numerical approaches render correct results, they are incapable of revealing the frequency dependence (or independence) of $R_{bb}$ and, thus, cannot be viewed as wideband modeling in this respect. Strictly speaking, a valid $R_{bb}$ exists only at infinite frequency. On the other hand, since the frequency variable is not used in the three discussed analytical (and, thus, wideband) methods, $R_{bb}$ at every frequency point can be independently obtained and compared. Among the three, (12) has a near-constant $R_{bb}$ over the widest bandwidth; however, the 6-Ω offset relative to all the other discussed approaches limits its application. While the one suggested in [20] gives valid results for frequency from 15 to 30 GHz, our proposed (11) can have satisfying $R_{bb}$ for frequency from down below 10 to 30 GHz and, thus, is the most preferred.

Furthermore, since this $R_{bb}$ is directly derived at the intended bias point, rather than adopted from values using other bias conditions, the current crowding effect [25]–[28], even if exists, will not affect the validity of our proposed formulation, and since the simulated $S$-parameters agree with their measured counterparts, as demonstrated in Section II-E, it is just fine using a single $R_{bb}$, rather than a more complicated sub-circuit [29], in modeling this part of the transistor.

### *E. Determination of Normal-Biased Intrinsic Parameters*

With $R_{bb}$ deembedded, parameters of the normal-biased intrinsic transistor can, therefore, be determined as $C_{be} = 333.5$ fF, $R_{be} = 737\ \Omega$, and $C_{bc} = 3.9$ fF. With the transconductance defined as [5], [11]–[13]

$$G_m = G_{m0} \cdot \frac{e^{-j\omega\tau_1}}{1 + j\omega\tau_2} = Y_{21} - Y_{12} \tag{18}$$

where $\omega$ is the angular frequency, we then have $G_{m0} = 158$ mS, $\tau_1 = 1.5$ ps, and $\tau_2 = 1.2$ ps. In Fig. 12(a), the solid curve is the magnitude of the measured $G_m$ and the overlapping dashed curve is its simulated counterpart. Apparently, $\tau_2$ is needed for explaining this magnitude frequency dependency. In Fig. 12(b), the solid curve is the phase of the measured $G_m$, the overlapping dashed curve 1 is its simulated counterpart with both $\tau_1$ and $\tau_2$ employed. If we retain the time constant $\tau_1$ while omitting $\tau_2$, or retain $\tau_2$, but omitting $\tau_1$, shown as dashed curves 2 and 3, respectively, phase discrepancy can be observed.

Knowing the intrinsic transistor's parameters now enables the calculation of the cutoff frequency $f_T$, which is the frequency where the magnitude of the current gain $h_{21}$ is equal to 1. With

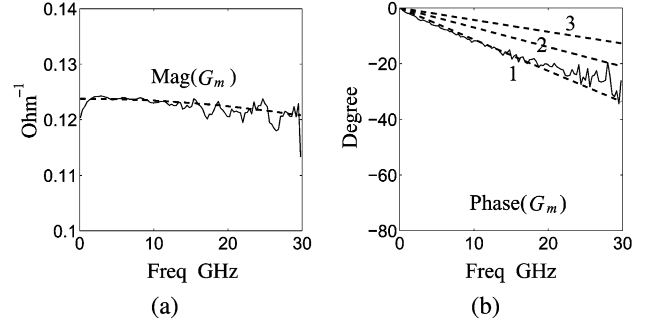


Fig. 12. Measured and simulated transconductance. (a) Magnitude of the transconductance where the solid curve is the measured result, i.e., $Y_{21} - Y_{12}$; the overlapping dashed curve is its simulated counterpart with $G_{m0} = 123.8$ mS, $\tau_1 = 1.5$ ps, and $\tau_2 = 1.2$ ps. (b) Phase of the transconductance where the solid curve is the measured result; the overlapping dashed curve 1 is its simulated counterpart; dashed curve 2 is the simulated phase with only $\tau_1$, but no $\tau_2$; dashed curve 3 is with $\tau_2$ only.

nonzero $\tau_2$ in the transconductance, the conventional $f_T$ expression needs to be revised. As

$$h_{21} = \frac{\dfrac{-j\omega C_{bc} + G_{mo} \cdot e^{-j\omega\tau_1}}{(1 + j\omega\tau_2)}}{j\omega\left(C_{be} + C_{bc}\right) + \dfrac{1}{R_{be}}} \approx \frac{\dfrac{G_{mo} \cdot e^{-j\omega\tau_1}}{(1 + j\omega\tau_2)}}{j\omega\left(C_{be} + C_{bc}\right)} \tag{19}$$

where the leakage currents flowing through $C_{bc}$ and $R_{be}$ are assumed negligible at high frequency in the approximation, we then have

$$f_T = \frac{1}{2\pi}\left[\frac{-1 + \sqrt{\dfrac{1 + 4\tau_2^2 G_{m0}^2}{\left(C_{be} + C_{bc}\right)^2}}}{2\tau_2^2}\right]^{1/2} \tag{20}$$

and

$$\lim_{\tau_2 \to 0} f_T = \frac{G_{m0}}{2\pi\left(C_{be} + C_{bc}\right)}. \tag{21}$$

Fig. 13 shows the $h_{21}$ curves in logarithmic and linear scales. In Fig. 13(a), solid curve 1 corresponds to the total transistor, solid curve 2 is with the intrinsic transistor only, the dashed straight lines are their high-frequency linear approximations in this logarithmic scale. Fig. 13(b) has the same results, but expressed in linear scale. Thus, $f_T$ is 42 GHz when the total transistor is employed, as by extrapolating the logarithmic curve to the $X$-axis, and we have $f_T$ equal to 56 GHz for the intrinsic resistor, which agrees with the 54.1 GHz calculated using (20); it is 58.4 GHz using (21), also a valid approximation. Likewise, by defining the gain $U$ as [30]

$$U = \frac{\left|\left(\dfrac{S_{21}}{S_{12} - 1}\right)\right|^2}{2k\left|\dfrac{S_{21}}{S_{12}}\right| - 2\mathrm{Re}\left(\dfrac{S_{21}}{S_{12}}\right)} \tag{22}$$

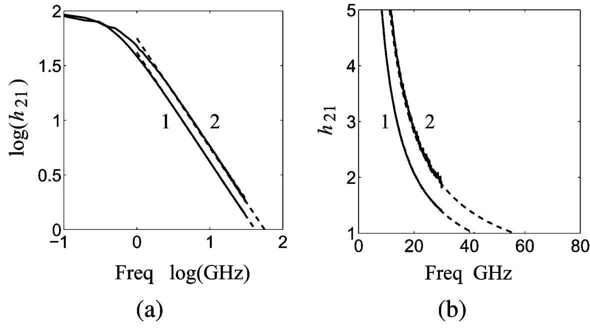


Fig. 13. Magnitude of $h_{21}$ versus frequency. (a) In logarithmic scale where the solid curve 1 is with the total transistor; solid curve 2 is with the intrinsic transistor only. The two dashed curves are their high-frequency linear approximation for deriving $f_T$. (b) In linear scale.

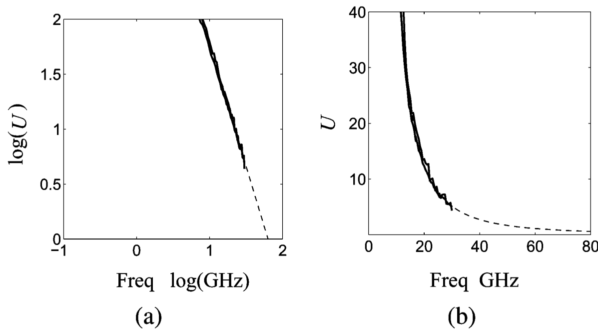


Fig. 14. Magnitude of gain $U$ versus frequency. (a) In logarithmic scale where the two overlapping solid curves are the measured and simulated results with the total transistor; the dashed curve is the high-frequency linear approximation for deriving $f_{\max}$. (b) In linear scale.

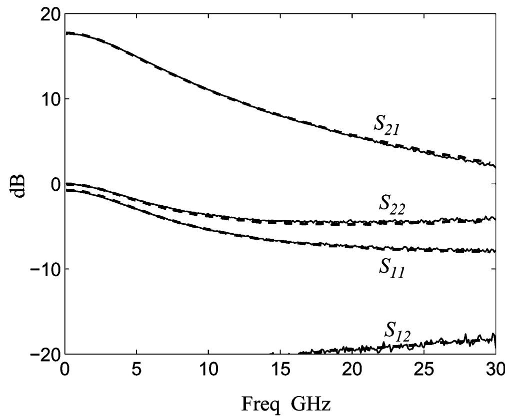


Fig. 15. Measured and simulated $S$-parameters of the normal-biased HBT. The solid curves are the measured results; the overlapping dashed curves are the simulated ones. The error $\epsilon^2$ defined in (23) is 0.13%.

where $k$ is the stability factor, the maximum oscillation frequency $f_{\max}$, which is the frequency at which $U$ is equal to 1, can be easily obtained. Both the measured $S$-parameters and the model-based $S$-parameters give the same $f_{\max} = 63$ GHz, as shown in Fig. 14.

Accuracy of the HBT's small-signal Pi modeling can be verified by comparing the measured and simulated $S$-parameters,

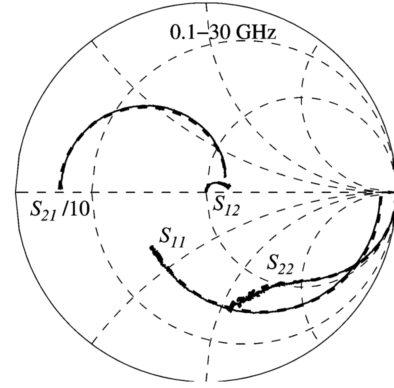


Fig. 16. Measured (solid line) and simulated (dotted line) $S$-parameters of the normal-biased HBT on the Smith chart.

TABLE II
NORMAL-BIASED TRANSISTOR

| $V_c$ = 2Volt | $I_c$ = 6.9mA | $V_b$ = 0.95Volt | $I_b$ = 58.4$\mu$A |
|---|---|---|---|
| $R_{bb}$ = 25Ω | $G_{m0}$ = 123.8mS | $\tau_1$ = 1.5pSec | $\tau_2$ = 1.2pSec |
| $R_{be}$ = 737Ω | $C_{be}$ = 333.5fF | $C_{bc}$ = 3.9fF | $C_{ext}$ = 26fF |
| $R_b$ = 7.5Ω | $R_c$ = 4.3Ω | $C_{pad1}$ = 43fF | $C_{pad2}$ = 46fF |
| $R_e$ = 4.1Ω | $R_{sub}$ = 128.4Ω | $C_{sub1}$ = 21.5fF | $C_{sub2}$ = 57.5fF |

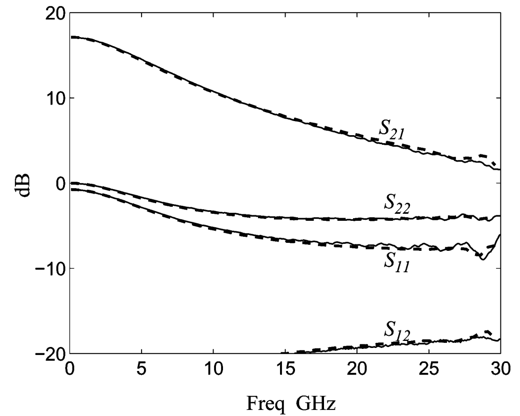


Fig. 17. Measured and simulated $S$-parameters of the HBT biased at $V_c = 2$ V, $I_c = 6.6$ mA, $V_b = 0.95$ V, and $I_b = 65.7$ $\mu$A. The solid curves are the measured results; the overlapping dashed curves are their simulated counterparts. The error $\epsilon^2$ is 0.38%.

as shown in Figs. 15 and 16. Here, the solid curves are the measured results; the overlapping dashed curves are their simulated counterparts. If we define the error $\epsilon^2$ as

$$\epsilon^2 = \frac{1}{4N}\sum\left[\left|\frac{S_{11}^{\text{mea}} - S_{11}^{\text{sim}}}{S_{11}^{\text{mea}}}\right|^2 + \left|\frac{S_{21}^{\text{mea}} - S_{21}^{\text{sim}}}{S_{21}^{\text{mea}}}\right|^2 + \left|\frac{S_{12}^{\text{mea}} - S_{12}^{\text{sim}}}{S_{12}^{\text{mea}}}\right|^2 + \left|\frac{S_{22}^{\text{mea}} - S_{22}^{\text{sim}}}{S_{22}^{\text{mea}}}\right|^2\right] \quad (23)$$

where the summation is over the $N = 300$ frequency points from 0.1 to 30 GHz. The calculated error $\epsilon^2$ is 0.13%. The bias condition and parameter values used in the simulation are tabulated in Table II.

Applying the same collector and base voltages, another transistor of the same size on the same wafer is measured, with

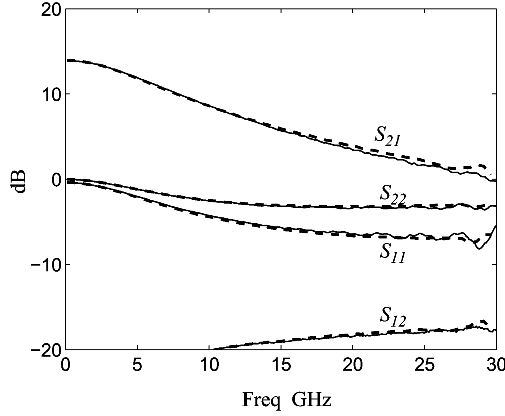


Fig. 18. Measured and simulated $S$-parameters of the HBT biased at $V_c = 2$ V, $I_c = 2.8$ mA, $V_b = 0.90$ V, and $I_b = 19.4\ \mu$A. The solid curves are the measured results; the overlapping dashed curves are their simulated counterparts. The error $\epsilon^2$ is 0.27%.

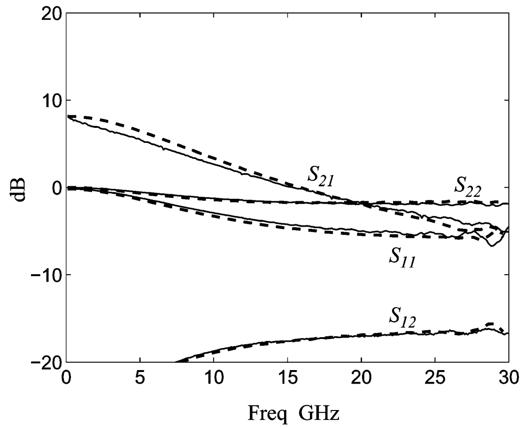


Fig. 19. Measured and simulated $S$-parameters of the HBT biased at $V_c = 2$ V, $I_c = 0.73$ mA, $V_b = 0.85$ V, and $I_b = 4.6\ \mu$A. The solid curves are the measured results; the overlapping dashed curves are their simulated counterparts. The error $\epsilon^2$ is 0.86%.

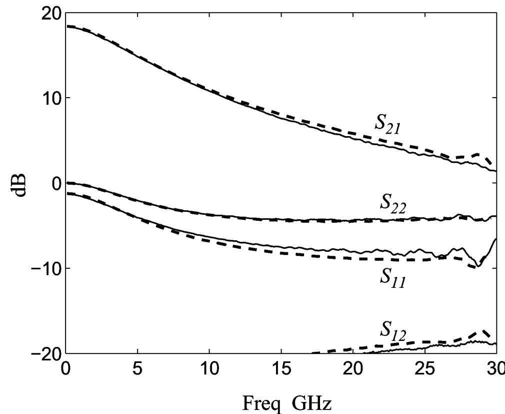


Fig. 20. Measured and simulated $S$-parameters of the HBT biased at $V_c = 2$ V, $I_c = 11.8$ mA, $V_b = 1.0$ V, and $I_b = 124\ \mu$A. The solid curves are the measured results; the overlapping dashed curves are their simulated counterparts. The error $\epsilon^2$ is 0.55%.

consistent results shown in Fig. 17. If $V_b$ is changed from 0.95 to 0.9 V and then 0.85 V, $I_c$ will decrease from 6.6 to 2.8 mA and then 0.73 mA, with the corresponding current density being 1.08, 0.46, and 0.12 mA/$\mu$m$^2$, respectively. The simulated results in these cases agree with their respective measured counterparts, as shown in Figs. 18 and 19. On the other hand, if $V_b$ is changed from 0.95 to 1.0 V, $I_c$ will increase from 6.6 to 11.8 mA (current density 1.93 mA/$\mu$m$^2$) with slightly improved gain response at low frequency; the simulated results still follow the measured ones, as shown in Fig. 20. Both $f_T$ and $f_{\max}$ under these different base voltages are tabulated in Table III.

TABLE III
TRANSISTOR BIASED AT DIFFERENT BASE VOLTAGES

| $V_b$ | 0.85Volt | 0.9Volt | 0.95Volt | 1.0Volt |
|---|---|---|---|---|
| $I_c$ | 0.73mA | 2.8mA | 6.6mA | 11.8mA |
| $C_{bc}$ | 2.27fF | 3.24fF | 3.59fF | 4.51fF |
| intrinsic $f_T$ | 21GHz | 42GHz | 53GHz | 50GHz |
| overall $f_T$ | 15GHz | 33GHz | 42GHz | 41GHz |
| overall $f_{max}$ | 34GHz | 53GHz | 62GHz | 59GHz |

## III. CONCLUSION

In this paper, new procedures for deriving the SiGe HBT's small-signal Pi modeling have been developed. For the external base–collector capacitor $C_{\rm ext}$ and the base spreading resistor $R_{bb}$, reliable analytical solutions have been proposed and compared with other methods. The lossy substrate effect has also been appropriately modeled. Agreements between the measured and simulated results in each derivation step thus vindicates the accuracy and efficiency of our new modeling approach. In addition to the intended normal-biased condition, this proposed approach shows satisfying results for different biasing conditions. Therefore, circuits designed using the HBT's small-signal Pi model can be accurately analyzed. In the future, we plan to extend this modeling work to address each parameter's nonlinear effect, thus facilitating the design of mixers.

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