Three-Dimensional Fully Symmetric Inductors, Transformer, and Balun in CMOS Technology

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***Abstract*—This paper presents novel three-dimensional (3-D) symmetric passive components, including inductors, transformers, and balun. Layout areas of these components are drastically reduced by 32% to 70%, while the symmetry of the input and the output ports is still maintained. The inductance mismatch in the 3-D transformer is less than 0.1%, and the coupling coefficient can be up to 0.77. The 3-D balun manifests less than 0.6-dB gain mismatch for 10-GHz range, and the phase error is less than 7° from 1- to 10-GHz frequency range according to measurement results. Furthermore, the self-resonant frequency ($f_{\rm SR}$) of the proposed architecture is improved by 32% to 61% in contrast to their planar counterparts. On the other hand, the quality factor is degraded by less than 2 for the sake of using lower metal layers. The distributed capacitance model is utilized to validate their superiorities in $f_{\rm SR}$. All the devices are fabricated in a generic 0.18-μm CMOS process.**

***Index Terms*—Balun, coupling coefficient, self-resonant frequency, transformer, 3-dimensional inductor.**

I. Introduction

With the blooming progress in VLSI technologies, system/radio on a chip (SOC/ROC) has become a prominent trend for circuit design in the nanometer-scaled CMOS era. Monolithic passive components, including inductors, transformers, and baluns, have been widely used in RF ICs design, such as low noise amplifier [1], mixer [2], and oscillators [3], etc. These components play a key role in the circuit integration, and in general have significant impacts on the overall system performance. In these applications, major issues of the passive components are quality factor, self-resonant frequency, chip area, and coupling coefficient (for transformer and balun). On the other hand, for broad band amplifier design under a low supply voltage, shunt/series peaking techniques utilizing inductor or transformer are often adopted for bandwidth enhancement. In these cases, the self-resonant frequency ($f_{\rm SR}$) of the inductor is more demanding than its quality factor. As the operating frequency exceeds $f_{\rm SR}$, the peaking inductor would become a capacitive load and dominate the achievable operating speed of the circuit. Furthermore, the chip area of the passive components is also a critical concern, especially in some applications where lots of passive components are required, such as a limiting amplifier design [4].

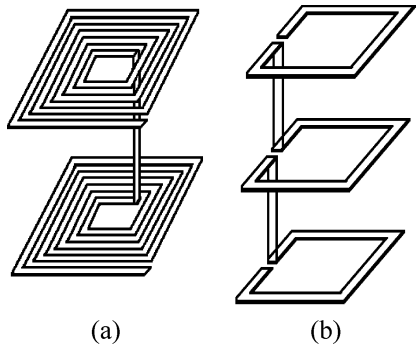

Fig. 1. (a) Stacked inductors. (b) Miniature 3-D inductors.

Recently, several passive component architectures with improved performance have been proposed, including stacked inductors [Fig. 1(a)], miniature 3-D inductors [5] [Fig. 1(b)] [6], symmetric planar inductors, transformers, and baluns [7], [8].

Also, other techniques to improve the quality factor and self-resonant frequency of the passive components have been addressed [9]–[13]. Conventionally, these passive components are laid out in a planar spiral shape, which occupies significant chip area, especially for balun and transformer design. Although [5] and [6] propose stacked architectures to reduce the chip area, but those miniaturized inductors are basically asymmetric, as are illustrated in Fig. 1.

This paper proposes novel 3-D miniaturized passive components while maintaining the symmetry of both the input and the output ports [21]. In the RF or broad band integrated circuits (ICs) designs, fully differential architectures are preferable for they have higher common mode noise immunity. Our proposed passive components can be utilized to replace two asymmetric counterparts in these designs, so as to save chip area and cost. Also, they manifest good inductance matching, higher self-resonant frequency, and higher coupling coefficient by the fully symmetric interleaved architecture. This implies that the layout trace can be shortened to achieve the same inductance, thus smaller series resistance can be benefited. In addition, by the differential excitation of the fully symmetric 3-D architecture, the inductor Q can be improved by reducing the substrate loss [10]. And the most important of all, the chip area can be drastically reduced in contrast to their planar counterpart.

This paper is organized as follows. Section II presents the architecture of our proposed 3-D symmetric inductor and its lumped circuit model. Recently, inductor models on substrate loss and quality factor have drawn tremendous research efforts [14]–[20]. In this paper, a simple distributed capacitance model

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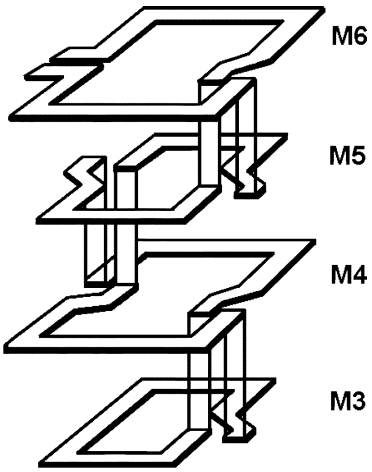

Fig. 2. Symmetric 3-D inductor structure.

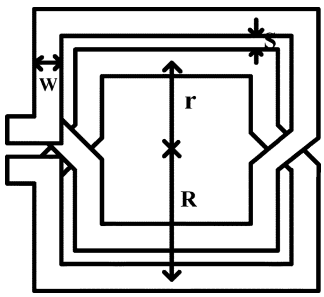

Fig. 3. Top view of a symmetric inductor.

(DCM) of the 3-D inductor is utilized to investigate its self-resonant frequency ($f_{\rm SR}$) [22]. Their superiorities in $f_{\rm SR}$ over conventional planar architecture are validated by both the DCM and experimental results. Section III describes the applications of the 3-D inductor in a 3-D transformer design. To improve its coupling coefficient, a multi-layer, multi-turn transformer is proposed. Its self-resonant frequency is also investigated by a DCM model. The design of 3-D baluns and their characterizations are reported in Section IV. Finally, our conclusions are presented in Section V.

II. 3-D Inductor

Fig. 2 illustrates the proposed 3-D symmetric inductor architecture [21]. As a 4 turns example, the metal wire winds downward with a right-half turn on the upper layer interleaved with a left-half turn on the adjacent lower metal layer and vice versa. When the wire reaches the bottom layer, it winds upward along the counter path. In this way, the input and output port will be fully symmetric. To eliminate the parasitic capacitance between the adjacent metal layers, the outer radius of the loops on the adjacent layers are offset by the metal width, so that loops on M6, and M4 have the same radius, while that of loops on M5 and M3 is smaller.

The 3-D inductor can be characterized by the following design parameters, including the number of layers n, metal width w, inner radius r, outer radius R, and the metal spacing between adjacent wires s. Fig. 3 shows the top view of the inductor corresponding to the design parameters.

The self-resonant frequency ($f_{\rm SR}$) of an inductor can be viewed as the frequency at which the peak magnetic (E_M) and electric energy (E_E) are equal, and can be determined by $f_{\rm SR} = (2\pi\sqrt{C_{\rm eq}L_{\rm eq}})^{-1}$, where $L_{\rm eq}$ and $C_{\rm eq}$ respectively represent the equivalent inductance and capacitance of the inductor. In the following, the $C_{\rm eq}$ of both our proposed 3-D inductor and a planar inductor are analyzed utilizing a DCM [22] to investigate their $f_{\rm SR}$ performance respectively.

For a given peak voltage of V_0 across the inductor and a stored electric energy of (E_E) in the structure, the equivalent capacitance $C_{\rm eq}$ can be calculated by [6], [22]

$$E_E = \frac{1}{2}C_{\rm eq}V_o^2. \tag{1}$$

To derive the electric energy stored in the parasitic capacitors of the inductor, the following assumptions are made to simplify the derivations [5], [6], [22].

1) Voltage distribution is proportional to the length of the metal track.
2) The voltage potential is equal in half turn of the metal wire in the inductor and is determined by averaging the voltages of the previous half turn and the next one.

For an n turns inductor, assume the lengths of each half turn are denoted as $l_1, l_2, \ldots, l_{2n}$, the metal width is W, metal thickness is T, and the total length of the metal wire is $l_T = \sum_{k=1}^{2n} l_k$

Define $d_k = 1/l_T \cdot \sum_{i=1}^{k} l_i$, the voltage profile of the inductor under a single ended stimulus can be described as

$$V_k = V_0 \times (1 - d_k). \tag{2}$$

Based on the above assumptions, the voltage of the kth half turn of the inductor can be approximated as

$$V(k) = \frac{1}{2}\left[V_0 \times (1 - d_{k-1}) + V_0 \times (1 - d_k)\right]. \tag{3}$$

Fig. 4 displays the cross-sectional view of a planar inductor and its voltage profile. For a planar inductor, the major parasitic capacitance stems from the metal-to-substrate overlapped capacitance and the metal-to-metal side-wall capacitance. Let $C_{{\rm mts},j}$ denote the unit capacitance of metal j to substrate, which is a constant depending on the process [23], the electrical energy stored in the capacitor between the metal layer and the substrate can then be expressed as $E_{E1,{\rm mts}}$, where

$$E_{E1,{\rm mts}} = \frac{1}{2}\sum_{k=1}^{2n} C_{{\rm mts},j} \cdot l_k \cdot W \cdot V(k)^2. \tag{4}$$

In addition, let $C_{{\rm msm},j}$ denote the unit side-wall capacitance between the kth and the $k+2$th half turn on metal j, the electric energy stored in the side-wall parasitic capacitors between the metal layers can be expressed as $E_{E1,{\rm mtm}}$, where

$$E_{E1,{\rm mtm}} = \frac{1}{2}\sum_{k=1}^{2n-2} C_{{\rm msm},j} \cdot l_k \cdot T \cdot \left[V(k) - V(k+2)\right]^2. \tag{5}$$

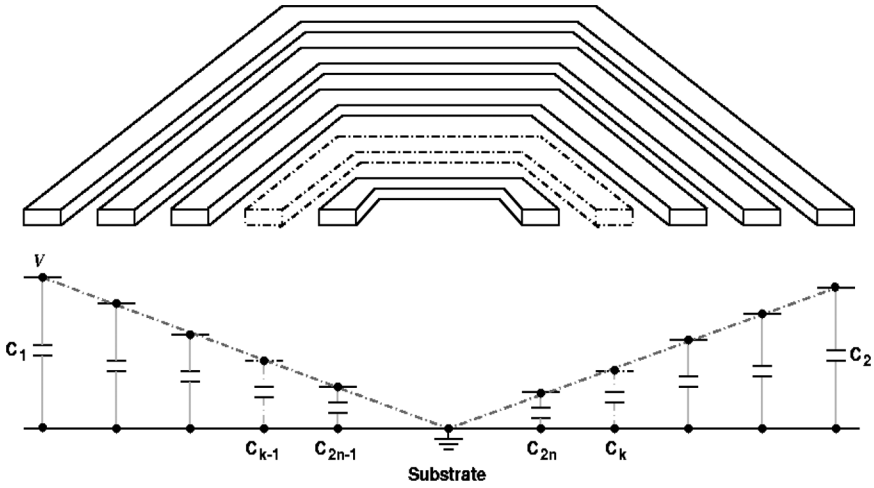

Fig. 4. Cross-sectional view and voltage profile of a planar inductor.

Combining (4) and (5), the total electric energy $(E_{E1,\mathrm{tot}})$ stored in the structure can be derived as [22]

$$E_{E1,\mathrm{tot}} = E_{E1,\mathrm{mts}} + E_{E1,\mathrm{mtm}} = \frac{1}{2} C_{\mathrm{eq1}} V_0^2. \tag{6}$$

Thus, the effective parasitic capacitance of a planar inductor can be derived utilizing the DCM and expressed as C_{eq1}, where

$$C_{\mathrm{eq1}} \approx \frac{1}{4} \sum_{k=1}^{2n} C_{\mathrm{mts},j} \cdot l_k \cdot W \cdot (2 - d_{k-1} - d_k)^2 + \frac{1}{4} \sum_{k=1}^{2n-2} C_{\mathrm{msm},j} \cdot l_k \cdot T \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2. \tag{7}$$

On the other hand, the cross-sectional view of the proposed 3-D inductor is shown in Fig. 5. For an n-turn, single turn per layer 3-D inductor, its major parasitic capacitance stems from the interlayer metal-to-metal and metal-to-substrate overlapped capacitance. Also, it can be seen that the metal-to-substrate capacitors exist in the bottom two metal layers only. Furthermore, since there is only one turn on a metal layer, the side-wall (fringing) capacitance is almost negligible.

Based on the same assumptions mentioned above, the electrical energy stored in the capacitor between the metal layer and the substrate can be expressed as $E_{E2,\mathrm{mts}}$, where

$$E_{E2,\mathrm{mts}} = \frac{1}{2} \sum_{k=n-1}^{n+2} C_{\mathrm{mts},j} \cdot l_k \cdot W \cdot V(k)^2. \tag{8}$$

Besides, let $C_{\mathrm{mtm},j}$ denote the unit metal-to-metal overlapped capacitance between the kth and the $k+2$th half turn on metal j, the electrical energy stored in the metal-to-metal parasitic capacitors can be represented as

$$E_{E2,\mathrm{mtm}} = \frac{1}{2} \left[\sum_{k=1}^{n-2} C_{\mathrm{mtm},j} \cdot l_k \cdot W \cdot [V(k) - V(k+2)]^2 + \sum_{k=n+1}^{2n-2} C_{\mathrm{mtm},j} \cdot l_k \cdot W \cdot [V(k) - V(k+2)]^2 \right] \tag{9}$$

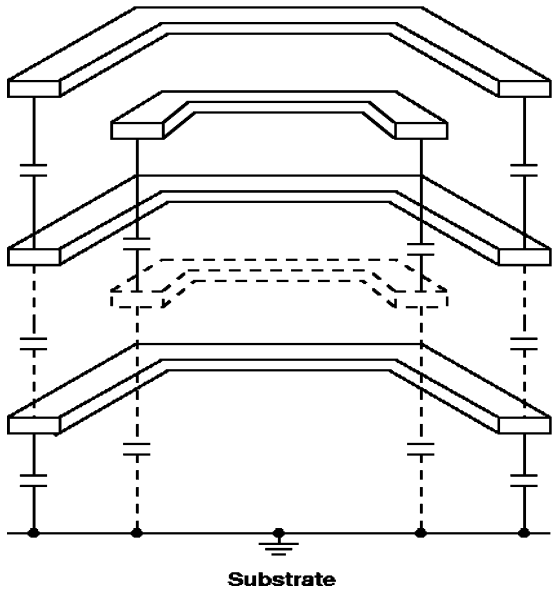

Fig. 5. Cross-sectional view of a 3-D transformer.

By taking both (8) and (9) into accounts, the total electric energy $(E_{E2,\mathrm{tot}})$ stored in the structure utilizing DCM can be derived as

$$E_{E2,\mathrm{tot}} = \frac{1}{2} C_{\mathrm{eq2}} V_0^2 = E_{E2,\mathrm{mts}} + E_{E2,\mathrm{mtm}}. \tag{10}$$

Thus, under a single-ended stimulus, the effective parasitic capacitance of the 3-D inductor can be expressed as C_{eq2}, where

$$C_{\mathrm{eq2}} \approx \frac{1}{4} \sum_{k=n-1}^{n+2} C_{\mathrm{mts},j} \cdot l_k \cdot W \cdot (2 - d_k - d_{k-1})^2 + \frac{1}{4} \sum_{k=1}^{n-2} C_{\mathrm{mtm},j} \cdot l_k \cdot W \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2 + \frac{1}{4} \sum_{k=n+1}^{2n-2} C_{\mathrm{mtm},j} \cdot l_k \cdot W \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2. \tag{11}$$

TABLE I
PERFORMANCE COMPARISONS OF PLANAR SYMMETRIC, 3-D ASYMMETRIC AND 3-D SYMMETRIC INDUCTOR

r = 45 μm	n	3	4	5	6
Planar symmetric inductor	L(nH)	1.56	2.6	4.65	6.25
	f_{SR}(GHz)	19.3	14.5	11.7	8.4
	Q(max)	7.4	6.9	6.2	5.3
3-D asymmetric inductor [6]	L(nH)	1.6	2.74	4.5	6.3
	f_{SR}(GHz)	25.2	18.4	14.7	11.2
	Q(max)	6.1	5.25	4.8	4.15
Proposed 3-D symmetric inductor	L(nH)	1.64	2.7	4.44	6.1
	f_{SR}(GHz)	31	21.5	15.4	12.5
	Q(max)	5.7	4.7	4.35	4.05
$\frac{A_{3D}}{A_{planar}}$	3-D Symmetric / Asymmetric Inductor	70%	52%	40%	32%

Since the equivalent inductance $L_{\rm eq}$ of an inductor can be derived as

$$L_{\rm eq} = \sum_{i=1}^{n} L_i + M \tag{12}$$

where L_i represents the inductance on each loop, and M represents the summation of mutual inductances, the self-resonant frequency can be derived as

$$f_{\rm SR} = \frac{1}{2\pi\sqrt{L_{\rm eq}C_{\rm eq}}}. \tag{13}$$

Thus an inductor structure with a smaller $C_{\rm eq}$ would manifest a higher $f_{\rm SR}$. Compare (7) with (11), although our proposed 3-D inductors suffer from metal-to-metal overlapped capacitance, the impacts of the parasitic capacitance can be alleviated by increasing the distance between the metal plates (offset the diameters of the adjacent loops), and minimizing the electrical potential between the top and bottom plates (by the twisted and interleaved architecture). On the other hand, in contrast to a planar counterpart, no metal-to-metal side-wall capacitance exists in the proposed one turn per layer architecture. The side-wall parasitic capacitance would become significant in the deep submicron technology [22]. Thus, the effective parasitic capacitance $(C_{\rm eq})$ of the 3-D inductor can be reduced, resulting in a better self-resonant frequency $(f_{\rm SR})$.

Table I summarizes the performance comparisons between planar symmetric inductors, conventional 3-D asymmetric inductors in [6], and our proposed 3-D symmetric inductors by EM simulation. With the same inner loop diameter (r), metal width (w), metal spacing (s), and about the same inductance, the 3-D inductors (for both the symmetric and asymmetric ones) manifest a higher self-resonant frequency in all cases by self shielding, and the most important of all, the chip area can be reduced by 32% to 70%. Besides, the quality factors for the symmetric and asymmetric 3-D inductors are about the same.

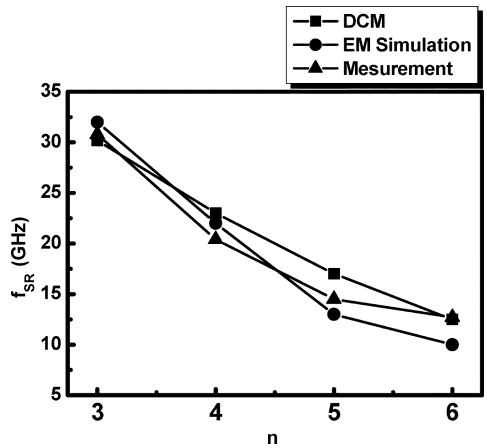

Fig. 6. $f_{\rm SR}$ performance comparison of 3-D inductor (by DCM model, EM simulation, and measurement).

In contrast to a planar inductor which is mainly composed of the top (thickest) metal, the series resistance of the 3-D inductors increases due to via connections and employing the lower (thinner) metal layers. Thus, the quality factor is degraded (by less than 2).

Fig. 6 illustrates the experimental results on the self-resonant frequency $(f_{\rm SR})$ v.s. number of turns (n) for the 3-D inductors. All the components are fabricated in a 0.18-μm standard CMOS technology, and have an outer radius (R) of 45 μm. The $f_{\rm SR}$ estimated by (11) are well agreed with simulations (by EM-tools) and measurement results for various numbers of turns (n). According to the simulation result, a 3-turns 3-D symmetric inductor has a self-resonant frequency as high as 30 GHz. It reveals that by both offsetting the diameters of adjacent loops and the interleaving voltage profile, the effective parasitic capacitance of the 3-D inductors can be significantly reduced, thus a high $f_{\rm SR}$ can be benefited.

Fig. 7 shows the distributed circuit model of a 4-turn 3-D inductor. Here, $(R_1 - R_4)$ and $(R_5 - R_8)$ respectively represent the distributed resistance of L_1 and L_2. $M_{\rm mn}$ represents the distributed mutual inductance between the mth and the nth half

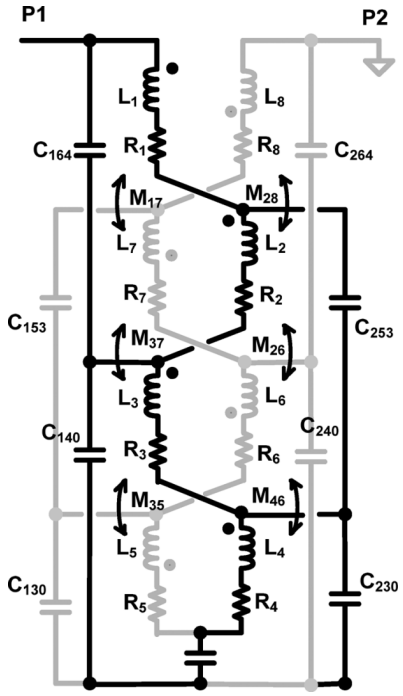

Fig. 7. Distributed circuit model of 3-D inductor.

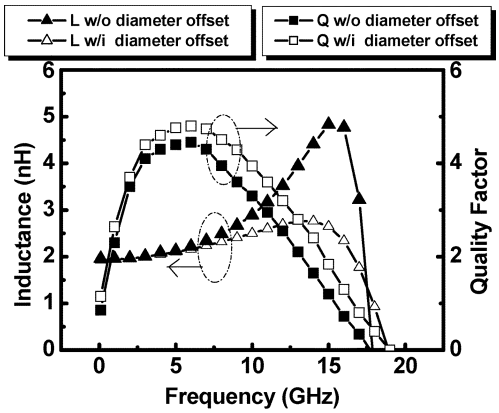

Fig. 8. Simulated inductance and quality factor of single-turn-4-layers architecture with and without diameter offset (inner radius $r = 38.5\ \mu$m, metal width $w = 10\ \mu$m, spacing $s = 1.5\ \mu$m).

turn of the 3-D inductor ($m = 1, 2, 3, 4$; $n = 5, 6, 7, 8$). C_{1jk} and C_{2jk} denote the distributed overlapping capacitance between metal layer ($j = 3, 4, 5, 6$; $k = 3, 4$) and substrate ($k = 0$).

Fig. 8 shows the simulated inductance and quality factor of the 3-D inductors with and without diameters offset of the adjacent loops. It can be seen that both the quality factor and the self-resonant frequency of the proposed architecture (with diameter offset) can be improved.

The 3-D inductors occupy a smaller chip area and manifest an improved self-resonant frequency at the expense of a poorer quality factor. In contrast to a planar inductor which is mainly composed of the top (thickest) metal, the series resistance of the 3-D inductors increases due to via connections and employing the lower (thinner) metal layers. The metal thickness is about 2μm for the top layer metal and is only 0.53 μm for the bottom layer metal in this technology. To improve the quality factor,

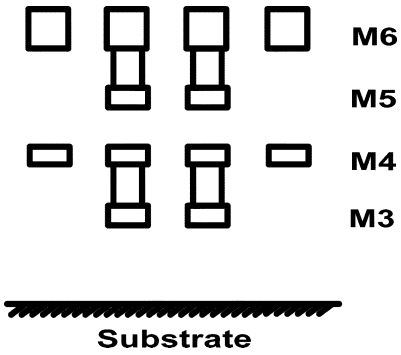

Fig. 9. Cross-sectional view of a symmetric 3-D inductor with IMLS.

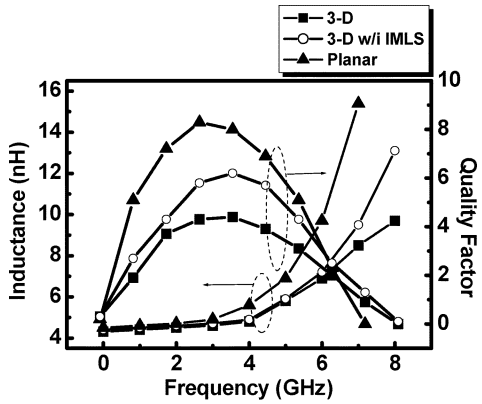

Fig. 10. Q comparison of planar, 3-D, and 3-D with IMLS inductors.

improved multi-level shunt (IMLS) techniques can be adopted [10]. Fig. 9 shows the cross-sectional view of the 3-D inductor with IMLS. As the radii of the loops on the adjacent metal layers are different, the effective trace thickness can be increased by the shunting metal layer. Besides, to avoid severely degrading its self-resonant frequency, the IMLS is only utilized in the inner loops to compromise between the parasitic capacitance and the series resistance.

Fig. 10 shows the quality factor comparisons of a planar symmetric and a 3-D symmetric inductor by simulation. Here the inner loops of the IMLS inductor is composed of two metal layers shunting together, as is shown in Fig. 9, while the planar inductor utilizes only the top layer metal. All the inductors have the same inductance of 4.5 nH, 4 turns, $w = 10\ \mu$m, $s = 1.5\ \mu$m and inner radius r of 65 μm. The planar and 3-D inductors respectively occupy a chip area of $209 \times 209\ \mu$m^2 and $163 \times 163\ \mu$m^2. According to simulation results, it can be seen that the peak quality factor of the planar inductor is the best (higher than that of the IMLS 3-D inductor by 2), while the quality factor of the 3-D inductor can be increased by 2 utilizing IMLS.

The superiorities of the proposed 3-D inductors in area consumption are further investigated for equivalent inductor (L) and quality factor (Q) with respect to their planar variants. Here the planar inductors are laid-out by either reducing the metal width w (planar I) or reducing the inner loop radius r (planar II). According to EM-simulation results, the performance comparisons are summarized in Table II. In both cases, the total length of the metal wire is about the same to have the same inductance. Thus,

TABLE II
PERFORMANCE COMPARISONS OF PLANAR AND 3-D INDUCTORS WITH EQUAL L AND Q

Architecture		Total Length	L	Q (max)	Metal Width	Metal Spacing	Inner Radius	f_{SR}	Area (μm x μm)
3-D	1-turn-3-layers	1200 μm	1.74 nH	6.2	10μm	1.5 μm	40 μm	20 GHz	66% 100x100
Planar I	3.7 turns	1194 μm	1.72 nH	6.28	5μm	1.5 μm	40 μm	13.5 GHz	94 % (119x119)
Planar II	3.5 turns	1196.5 μm	1.73 nH	6.55	10μm	1.5 μm	23 μm	17.1 GHz	100 % (123x123)

the number of turns is increased in the planar inductors for a reduced metal width or a reduced inner radius (3.7 turns for planar I and 3.5 turns for planar II). It turns out that the chip area saving in both cases becomes insignificant, while the $f_{\rm SR}$ of the planar inductors is still worse than that of the 3-D inductor. The main reason for the $f_{\rm SR}$ degradation is due to the fact that the increment of the side-wall capacitance (as the number of turns is increased) overwhelms the reduction of the metal-to-substrate capacitance in this technology.

III. 3-DIMENSINAL TRANSFORMER

A. 1 Turn per Layer 3-D Transformer

A 1:1, 3-D fully symmetric transformer can be easily built up by center-tapping the middle point of a 3-D symmetric inductor to a common mode voltage or ground, as is shown in Fig. 11(a). Fig. 11(b) depicts the symbol view, where an inverting type transformer bridges port 1 and port 2. The magnetic coupling mainly stems from conductor loops on the adjacent layers.

The voltage profile of a 3-D inductor under single-ended stimulus is different from that of differential excitation. For an n turns, single turn per layer transformer, the voltage profile of the transformer under differential stimulus is modified to

$$V_k = V_0 \times (1/2 - d_k) \tag{14}$$

and the voltage of the kth half turn of the inductor can be approximated as

$$V(k) = \frac{1}{2}\left[V_0 \times \left(\frac{1}{2} - d_{k-1}\right) + V_0 \times \left(\frac{1}{2} - d_k\right)\right]. \tag{15}$$

Thus, the effective parasitic capacitance of the 3-D transformer under differential excitation can be expressed as $C_{\rm eq3}$, where

$$\begin{aligned} C_{\rm eq3} \approx & \frac{1}{4}\sum_{k=n-1}^{n+2} C_{{\rm mts},j} \cdot l_k \cdot W \cdot (1 - d_k - d_{k-1})^2 \\ & + \frac{1}{4}\sum_{k=1}^{n-2} C_{{\rm mtm},j} \cdot l_k \cdot W \\ & \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2 \\ & + \frac{1}{4}\sum_{k=n+1}^{2n-2} C_{{\rm mtm},j} \cdot l_k \cdot W \\ & \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2 \end{aligned} \tag{16}$$

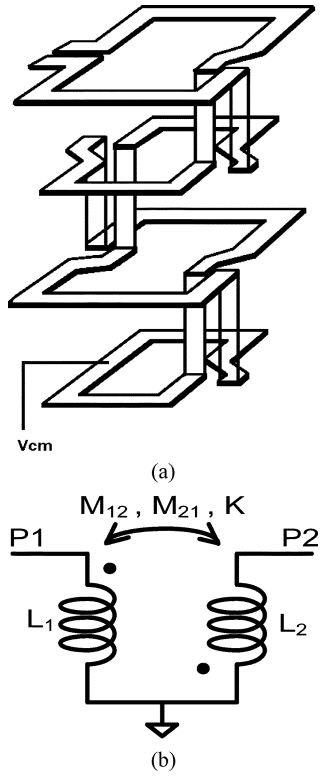

Fig. 11. (a) 1:1 3-D transformer. (b) Symbol view.

Compare (16) with (11), since the effective capacitance between the metal to the substrate is reduced, a 3-D inductor under differential stimulus manifests a higher self-resonant frequency. Fig. 12 illustrates the simulated quality factor of the single-turn-4-layers 3-D inductors (Inner radius $r = 38.5\ \mu$m, metal width $w = 10\ \mu$m, spacing $s = 1.5\ \mu$m) under single-ended and differential stimuli. It reveals that both the quality factor and $f_{\rm SR}$ can be improved by differentially driving the transformer.

The self-inductance (L_1, L_2), mutual inductance $(M_{12}M_{21})$, and coupling coefficient (K) of the 1:1 3-D transformer is characterized as

$$L_1 = \frac{\mathrm{Imag}\,(Z(1,1))}{2\pi f} \quad L_2 = \frac{\mathrm{Imag}\,(Z(2,2))}{2\pi f}$$
$$M_{21} = \frac{\mathrm{Imag}\,(Z(2,1))}{2\pi f} \quad M_{12} = \frac{\mathrm{Imag}\,(Z(1,2))}{2\pi f}$$
$$K = \frac{M_{21}}{\sqrt{L_1 L_2}} = \frac{M_{12}}{\sqrt{L_1 L_2}} (M_{12} = M_{21})$$

where $\mathrm{Imag}(Z(m,n))$ is the imaginary part of the Z parameters measured by network analyzer.

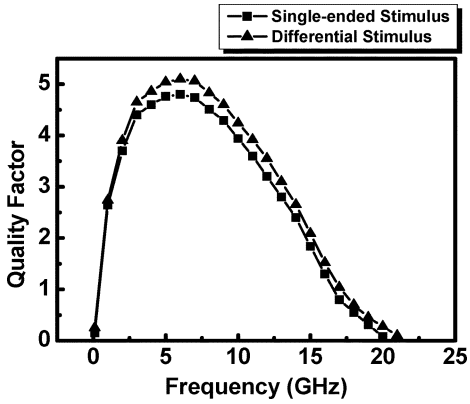

Fig. 12. Simulated quality factor of a single-turn-4-layers inductor under single-ended and differential stimuli (inner radius $r = 38.5$ μm, metal width $w = 10$ μm, spacing $s = 1.5$ μm).

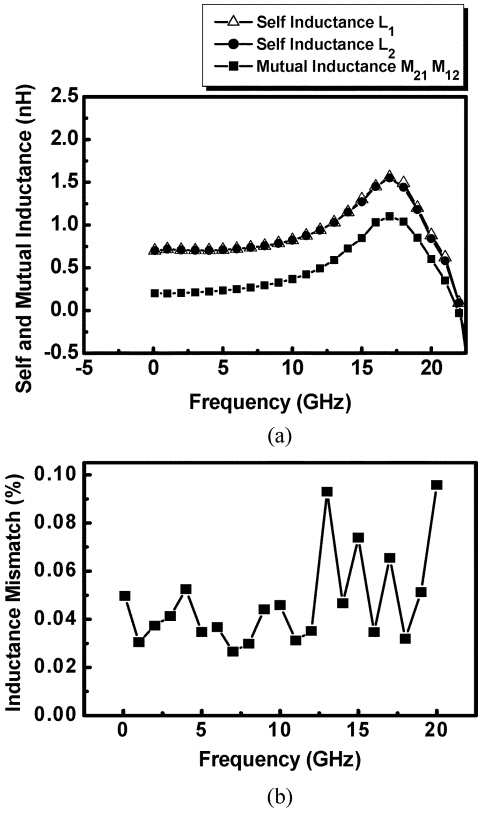

Fig. 13. (a) Measured self and mutual inductance. (b) Inductance mismatch.

Fig. 13 shows the measured performance of a test kit with an inner diameter $r = 38.5$ μm, $w = 10$ μm, $s = 1.5$ μm, 4 turns, and single turn per layer architecture. The inductance in each branch is about 0.75 nH. The mutual coupling coefficient of the transformer ranges from 0.3 to 0.7, which increases along with the increments of operating frequency. The inductance mismatches between the two branches are less than 0.1% within 20-GHz range, which demonstrates that the architecture is perfect in symmetry.

The effectiveness of the DCM in evaluating the $f_{\rm SR}$ of 3-dimensional transformers has been verified by experimental results. Fig. 14 illustrates the $f_{\rm SR}$ performance estimated by the DCM, simulated by an EM tool, and by measurement for 1 turn per layer transformers. In all cases the DCM model described

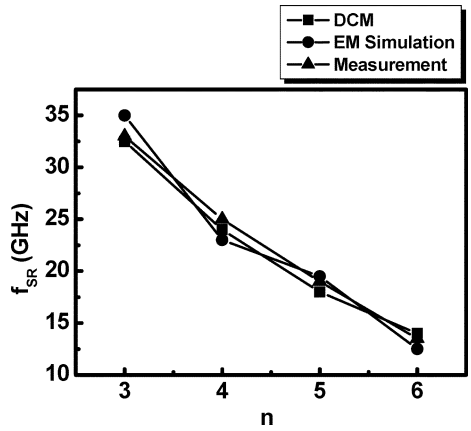

Fig. 14. $f_{\rm SR}$ performance comparison of 3-D transformer (by DCM model, EM simulation, and measurement).

in (16) provide a convenient and fairly accurate way in evaluating $f_{\rm SR}$ performance. Also, the $f_{\rm SR}$ of a differentially driven transformer shown in Fig. 14 is better than that of a single-ended driven inductor which is shown in Fig. 6.

B. 2 Turn per Layer 3-D Transformer

To further improve the coupling coefficient of the 3-D transformer, a two turn per layer architecture is proposed [24], as is shown in Fig. 15(a). Compared to its one turn per layer counterpart, the mutual coupling coefficient is enhanced by increasing both the magnetic coupling on the same metal layer and the adjacent metal layer.

The distributed circuit model of the 2 turns two layer transformer is shown in Fig. 15(b), where R_i, and L_i $(\mathrm{i} = 1 \sim 8)$ respectively represent the distributed resistance and inductance, $M_{\rm mn}$ represents the distributed mutual inductance between the mth and the nth half turn of the 3-D transformer ($\mathrm{m} = 1, 2, 3, 4$; $\mathrm{n} = 5, 6, 7, 8$). C_{1jk}, and C_{2jk} denote the metal-to-metal overlapped capacitance ($\mathrm{j} = 6$, $\mathrm{k} = 5$), and C_{1xx}, and C_{2yy} denote the side-wall fringing capacitance $(x, y = 5, 6)$.

For a $2n$ turns, 2 turns per layer transformer, define

$$d_k = \frac{\sum_{i=1}^{k} l_i}{\sum_{i=1}^{4n} l_i}. \tag{17}$$

Based on the DCM mentioned above, the total electric energy $(E_{E4,\rm tot})$ stored in the structure utilizing DCM can be derived as

$$\begin{aligned} E_{E4,\rm tot} &= E_{E4,\rm mts} + E_{E4,msm} + E_{E4,\rm mtm} \\ &= \frac{1}{2}\sum_{k=n}^{n+1} C_{\rm mts}(j)\cdot l_k \cdot W \cdot \left\{[V(k)]^2 + [V(3k)]^2\right\} \\ &\quad + \frac{1}{2}\sum_{k=1}^{2n} C_{\rm msm}(j)\cdot l_k \cdot T \cdot [V(k) - V(k+2n)]^2 \\ &\quad + \frac{1}{2}\sum_{i=0, i\neq n-1}^{2n-2}\sum_{k=1}^{2} C_{\rm mtm}(j)\cdot l_k \cdot W \\ &\quad \cdot [V(k+i) - V(k+4n-2-i)]^2 . \end{aligned} \tag{18}$$

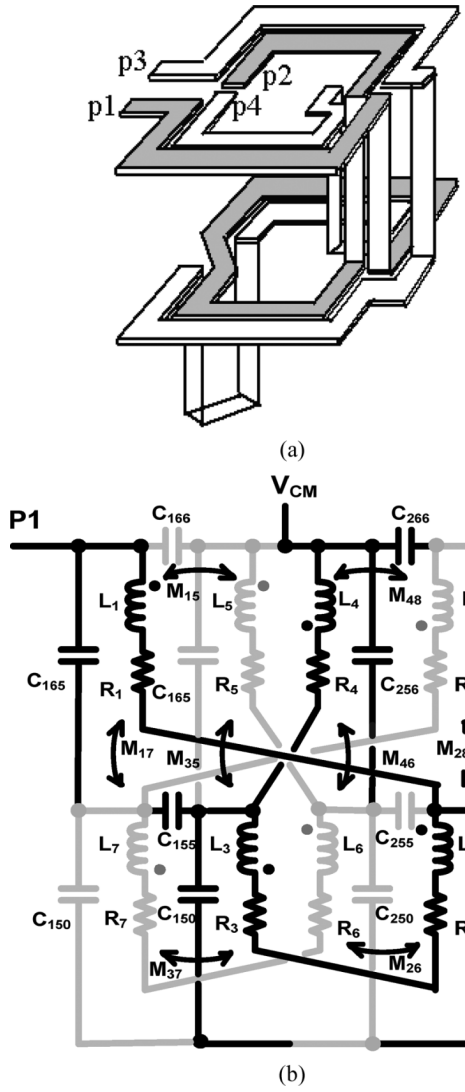

Fig. 15. (a) Symmetric 3-D transformer. (b) Circuit model of a 2 turns per layer transformer.

Thus the effective parasitic capacitance of a $2n$-turns-n -layers transformer under differential excitation can be derived as C_{eq4}, where

$$\begin{aligned} C_{\mathrm{eq4}} \approx & \frac{1}{4}\sum_{k=n}^{n+1} C_{\mathrm{mts}}(j)\cdot l_k \cdot W \\ & \cdot \left\{[1-d_{k-1}-d_k]^2+[1-d_{3k-1}-d_{3k}]^2\right\} \\ & +\frac{1}{4}\sum_{k=1}^{2n} C_{\mathrm{msm}}(j)\cdot l_k \cdot T \\ & \cdot [d_{k+2n}+d_{k+2n-1}-d_k-d_{k-1}]^2 \\ & +\frac{1}{4}\sum_{i=0,i\neq n-1}^{2n-2}\sum_{k=1}^{2} C_{\mathrm{mtm}}(j)\cdot l_k \cdot W \\ & \cdot [d_{k+4n-2-i}+d_{k+4n-3-i}-d_{k+i}-d_{k+i-1}]^2. \quad (19) \end{aligned}$$

Compare (19) with (16), the parasitic capacitances between the two ports are increased in contrast to that of a single turn per layer architecture. This implies that the insertion loss of a multi-turn per layer 3-D transformer can be reduced with the aid of electrical coupling in addition to magnetic coupling. On the other hand, the self-resonant frequency would be suffered. This view point is verified by measurement results.

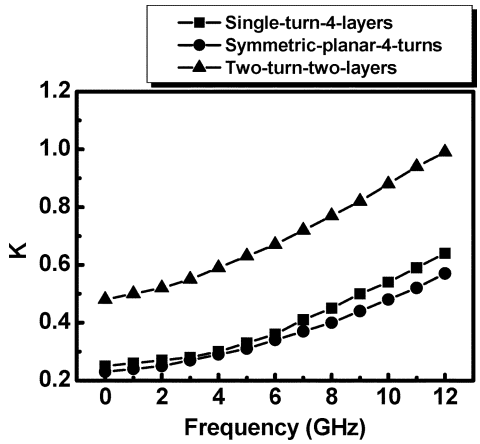

Fig. 16. Measured coupling coefficient k.

Fig. 16 illustrates the coupling coefficients of a single-turn per layer (4 turns), a two turns two layers, and a planar 4 turns transformer. With the same inductance in each branch (1 nH), the measured coupling coefficient of the two turn two layer transformer is up to 0.77 at 8 GHz, while the coupling coefficients for the single turn 4 layers (3-D) and single layer four turns (planar) architectures are about the same ($0.4 \sim 0.45$). Moreover, the chip areas for the 3-D structures are only 52% smaller compared to their planar counterpart. On the other hand, the self-resonant frequencies of a single turn per layer (4 layers), a two turns per layer (2 layers), and a 4 turns planar transformer are 24, 12.1, and 16.5 GHz, respectively. The performance benchmark is summarized in Table III. By improving the magnetic coupling and introducing electric coupling in the 3-D multi-turn per layer transformer, it is beneficial when the transformer is utilized as an ac-coupled device.

Fig. 17 shows the measured insertion loss of the transformer between the input and output ports. By a 4 turn, 2 turns per layer architecture, the insertion loss can be improved to be less than -3 dB. The f_{SR} performances of various inductors and transformers are summarized in Table IV. Also, the DCM models derived in (7), (11), (16), and (19) are applied in evaluating their f_{SR} respectively. Compared to the experimental results, the prediction errors are within 3% to 10%.

IV. 3-D Balun

A 3-D balun (balance to unbalance converter) can be built up by interleaving one symmetric inductor with one symmetric transformer. Fig. 18 depicts the corresponding layout topology and the symbol view. For an $R = 100$ μm, $w = 10$ μm, $s = 1.5$ μm, 3 turns/6 layers balun, the measured insertion loss (S_{21} and S_{31}), gain mismatches, and phase mismatches are illustrated in Fig. 19(a)–(c), respectively. In this prototype, a single turn per layer topology is used, thus the mutual coupling mainly stems from layer to layer magnetic coupling. The insertion loss within the $6 \sim 10$-GHz frequency band is less than 5 dB, which can be further improved by increasing the number of loops per layer. The 3-D balun manifests less than 0.6-dB gain mismatch and 7° phase error for 10-GHz frequency range.

TABLE III
PERFORMANCE BENCHMARK

W=10um	L1 / L2 / M21 (nH)	Q1 / Q2 (max)	f_{SR}	K	Area
Single-turn-4-layers transformer (r=38.5 um)	0.76/0.75/0.34@8GHz	4.7/4.6 @11GHz	24 GHz	0.45 @8GHz	52%
2-turn-2-layers transformer (r=27 um)	0.62/0.61/0.48@8GHz	4.3/4.2 @8.5GHz	12.1 GHz	0.77 @8GHz	52%
Symmetric planar 4-turns transformer (r=38.5 um)	0.8/0.79/0.32@8GHz	6.2/6.3 @10GHz	16.5 GHz	0.4 @8GHz	100%

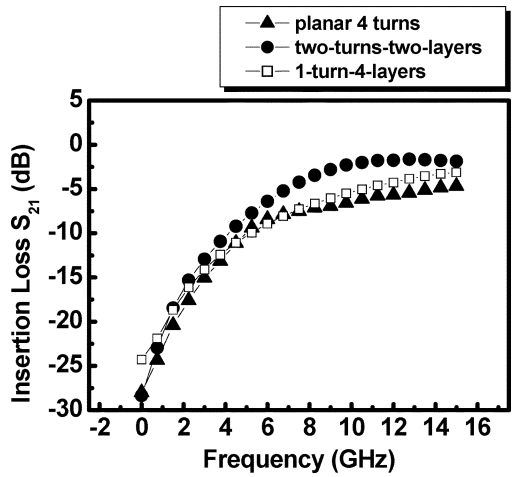

Fig. 17. Coupling loss of the transformer in two port network.

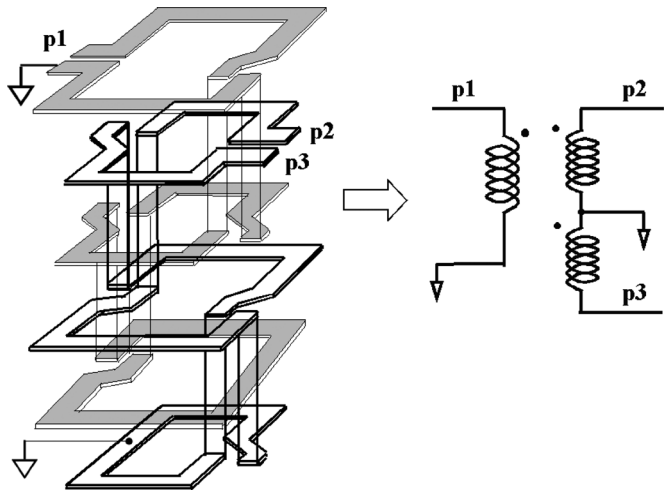

Fig. 18. Proposed symmetric 3-D balun. (a) Layout topology. (b) Symbol view.

Table V shows the performance comparison between the proposed 3-D balun and its planar counterpart by EM tool simulations. For an $r = 27$ μm, $w = 10$ μm, $s = 1.5$ μm, and 6 turns architecture (3 turns for both the primary and secondary port), the proposed 3-D balun manifests a lower insertion loss, a better gain and phase matching performance, a much higher self-resonant frequency, and the chip area is only 28% smaller, while the quality factor degradation is less than 1.5 in a 10-GHz frequency range.

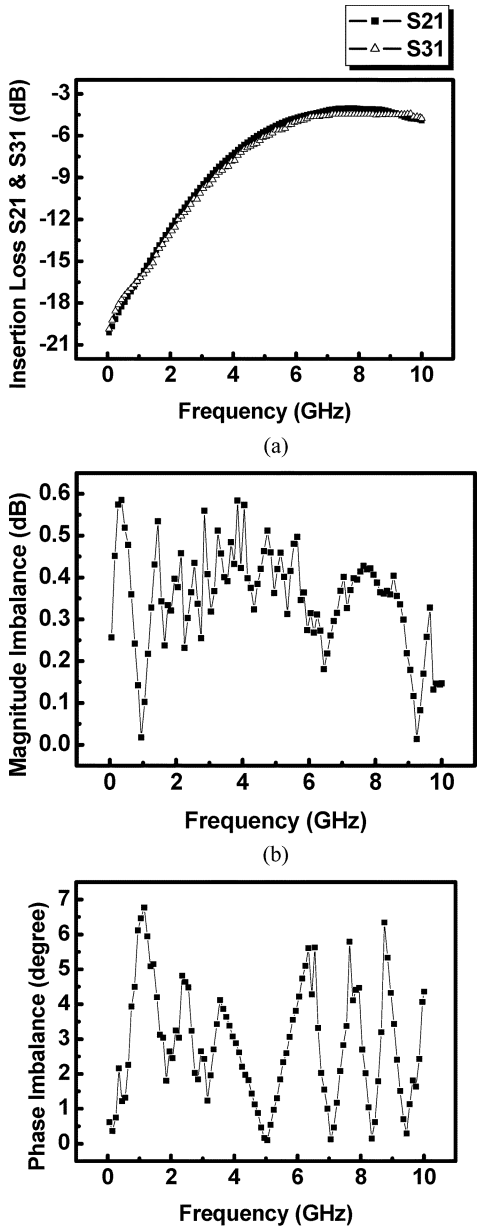

Fig. 19. 3D balun measurement results. (a) S_{21} and S_{31} gain response (insertion loss) (dB). (b) Gain mismatch (dB). (c) Phase mismatch (degree).

V. CONCLUSION

This paper presents novel miniaturized 3-D symmetric passive components, including inductors, transformers, and baluns

TABLE IV
f_{SR} COMPARISONS (DCM V.S. MEASUREMENT RESULTS)

Architecture	L_{eq} (nH)	C_{eq}(fF) by DCM	f_{SR} by DCM	f_{SR} Measured	Quality factor	Chip area	Prediction Error
Symmetric-planar- 4-turns inductor (r = 38.5 μ m)	2	51.4 (C_{eq1})	15.7 GHz	16.5 GHz	6.9	100% 139 x 139	5%
Single-turn- 4-layers inductor (r = 38.5 μ m)	2	23.96 (C_{eq2})	23 GHz	21 GHz	4.6	52 % 100 x 100	9.5%
Single-turn- 4-layers transformer (r = 38.5 μ m)	1.9	21.69 (C_{eq3})	24.8 GHz	24 GHz	4.7	52 % 100 x 100	3.3 %
Two-turns two-layers inductor (r=27 μ m)	2.2	67.2 (C_{eq4})	13.1 GHz	12.1 GHz	4.3	52 % 100 x 100	8.2 %

TABLE V
3-D V.S. PLANAR BALUN PERFORMANCE COMPARISON

Architecture	Insertion Loss (dB)	Gain Mismatch (dB)	Phase Mismatch (dB)	f_{SR} (GHz)	Q (max)	Area
3-D Balun	< 5 dB @6~10GHz	<0.6dB @1~10GHz	<7° @1~10GHz	15.6	5.4	100 x 100 28%
Planar Balun	<6.2dB @6~8GHz	<0.8dB @5~8GHz	<7° @5~8GHz	10.4	6.8	189 x 189 100%

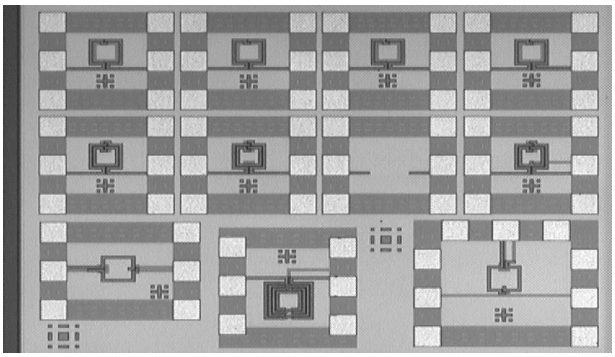

Fig. 20. Device micrograph.

[21]. All the devices are fabricated in a 0.18-μm 1P6M generic CMOS process. Fig. 20 shows the die photo. The de-embedded open kit is also built in for calibration [9]. Compared to conventional symmetrical planar counterparts, the proposed 3-D architectures manifest better self-resonant frequency and coupling coefficient while their chip areas are greatly reduced. The self-resonant frequency (f_{SR}) of the proposed 1 turn per layer architecture is improved by 32% to 61%, while the chip area is reduced by 32% to 70%. Quality factor improvements utilizing IMLS in the 3-D architectures are also proposed and discussed. The coupling coefficient (K) of the transformer can be further improved by enhancing magnetic coupling and introducing electric coupling in a multi-turn multi-layer architecture, but the self-resonant frequency will be suffered. The measured K is up to 0.77 at 8 GHz in a two turns two layer architecture. The 1:1 transformer shows less than 0.1% inductance mismatch in a 18-GHz range, and K is up to 0.7 at 8 GHz. In addition, 3-D baluns can be easily derived by interleaving a 3-D inductor with a 3-D transformer. Both the baluns and transformer show wide band gain and phase matching. And finally, DCMs of the 3-D passive components are utilized in calculating their effective parasitic capacitance and analyzing the self-resonant frequency. They provide a convenient way and design insights in the performance evaluation.

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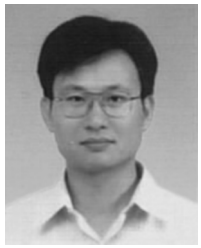

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