High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization

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Abstract—In this letter, high-performance bottom-gate (BG) low-temperature poly-silicon thin-film transistors (TFTs) with excimer laser crystallization have been demonstrated using self-aligned (SA) backside photolithography exposure. The grains with lateral grain size of about 0.75 μm could be artificially grown in the channel region via the super-lateral-growth phenomenon fabricated by excimer laser irradiation. Consequently, SA-BG TFTs with the channel length of 1 μm exhibited field-effect mobility reaching 193 cm^2/V $\cdot$ s without hydrogenation, while the mobility of the conventional non-SA-BG TFT and conventional SA top-gate one were about 17.8 and 103 cm^2/V $\cdot$ s, respectively. Moreover, SA-BG TFTs showed higher device uniformity and wider process window owing to the homogenous lateral grains crystallized from the channel steps near the BG edges.

Index Terms—Bottom gate (BG), excimer laser crystallization (ELC), lateral grain growth, self-aligned (SA), thin-film transistor (TFT).

I. INTRODUCTION

LOW-TEMPERATURE poly-silicon (LTPS) thin-film transistors (TFTs) have been extensively investigated for use in active-matrix liquid-crystal displays (AMLCDs) and active-matrix organic light-emitting displays [1], [2]. The mobility of poly-Si TFTs fabricated by excimer laser crystallization (ELC) is generally two orders higher than amorphous-Si (a-Si) TFTs; therefore, the peripheral driving circuits and pixel elements can be integrated on the same glass substrate. In the early stage of the LTPS TFTs development, bottom-gate (BG) TFT structure was attractive because the ELC was thought as an additional process step to the a-Si TFTs. However, BG TFTs suffered from worse electrical performance than top-gate (TG) TFTs because of the smaller grain size and poor grain quality resulting from the BG metal acting as a heat sink during ELC [3], [4]. Moreover, BG TFTs exhibited significant performance

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variation as the devices scaled-down owing to the misalignment effect. Although some self-aligned (SA) BG TFTs have been demonstrated, the device processes were too complicated to be utilized in the large-area fabrication [5], [6]. As a result, only a few studies have been conducted for BG TFTs with short channel length, and TG TFTs have been widely adopted in AMLCDs due to the self-alignment capability in the last decade. Although high field-effect mobility for TG-TFTs has been attained by ELC, it is difficult to make the laser-energy density hit the super-lateral-growth (SLG) regime everywhere due to the narrow laser process window [7]–[9]. Consequently, poor device uniformity and narrow process window were encountered in TG-TFTs. Furthermore, in the applications of system-on-panel, TFTs must exhibit good uniformity of device performance. Thus, many laser-crystallization methods were proposed to solve the above problems [10]–[17]. However, most of them need complex fabrication process or are problematic for circuit layout due to the anisotropy of the grain-boundary spacing.

In this letter, an SA-BG TFT with appropriate channel length has been fabricated by the simple ELC and backside exposure. The process steps in these technologies are not only highly compatible with the conventional commercial a-Si TFT process but also with minimum parasitic capacitance for high circuit performance. Owing to the lateral grain growth and SA structure, SA-BG TFTs exhibit higher performance and better uniformity.

II. DEVICE FABRICATION

Fig. 1 illustrates the key processes for the fabrication of SA-BG LTPS TFTs and non-SA-BG ones. At first, a 1000-Å-thick phosphorus-doped a-Si layer was deposited by LPCVD at 550 °C on quartz wafer. After defining the BG region, a 1000-Å-thick tetraethyl orthosilicate gate oxide layer was deposited by PECVD at 385 °C and a 1000-Å-thick a-Si layer was subsequently deposited by LPCVD at 550 °C. The samples were performed by KrF ELC ($\lambda = 248$ nm) at room temperature in a vacuum chamber of 10^{-3} torr. The number of laser shots per area was 20 (i.e., 95% overlapping), and the laser-energy density was varied. A SA photolithography, using the BG as an opaque mask, was applied by backside exposure through the quartz substrate [18], [19], while for the non-SA
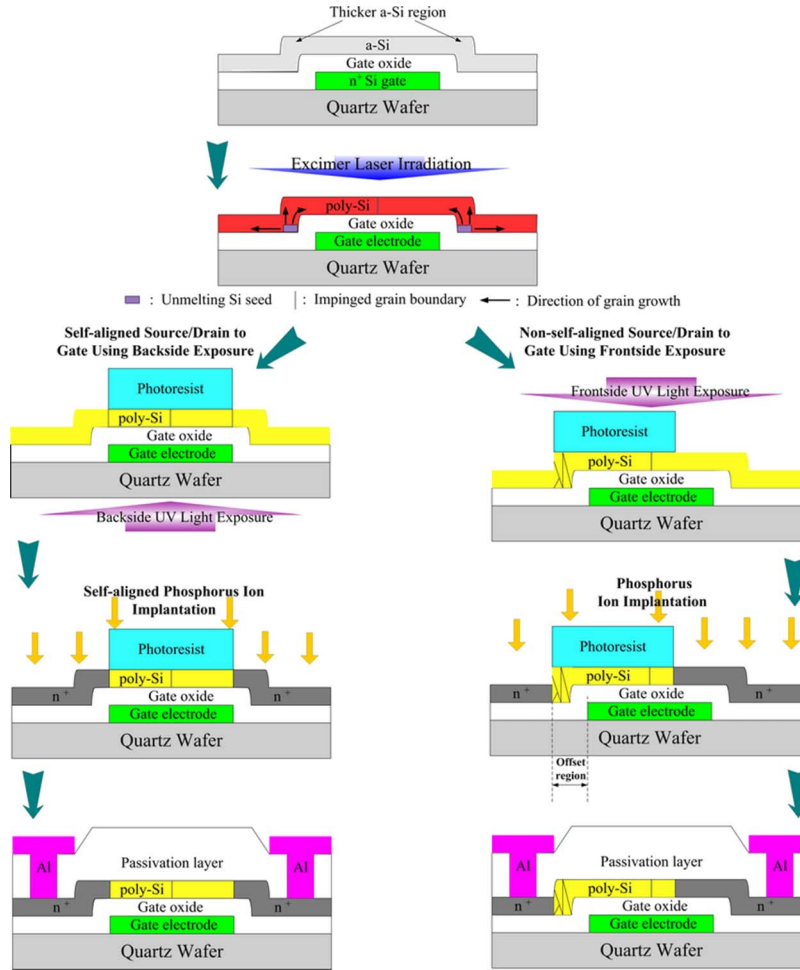
Fig. 1.   Key-process procedures for fabricating small-dimension SA BG LTPS TFTs with lateral grain growth and the non-SA BG ones.

TFT, a front-side UV light exposure is used in defining the source/drain regions which result in the offset region. The offset length in non-SA TFT is about 0.45 μm due to the process of masker aligner, and the offset length can be further reduced by using the I-line stepper system. It is worth mentioning that the fabrication processes of new SA TFTs and conventional non-SA ones are almost the same, except the lithography process of defining the source/drain regions. Then, a phosphorous ion implantation with a dose of 5×10^{15} cm^{-2} was carried out to form source-and-drain regions followed by the definition of active region by reactive-ion-etching. Next, the typical passivation layer deposition, dopants activation, contact holes opening, and metallization completed the fabrication of SA-BG TFTs. No hydrogenation plasma treatment was performed during the device-fabrication process. For comparison, the conventional non-SA-BG TFTs were also fabricated. In addition, for clarifying the effect of poly-Si grain structures on electrical characteristics, conventional SA-TG TFTs were also fabricated using the SLG laser-annealing condition.

III. RESULTS AND DISCUSSION

Fig. 2 displays the SEM photograph of ELC poly-Si films with BG structure after Secco etching and the length of BG is 1.5 μm. It can be observed that the grains with 0.75 μm
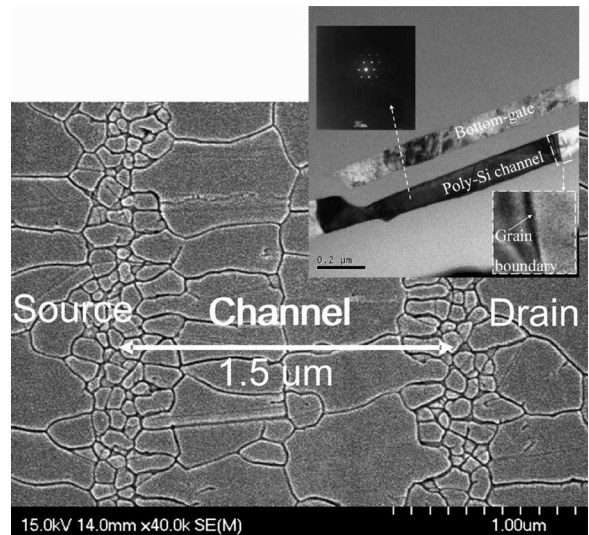

Fig. 2.   SEM micrograph of ELC poly-Si film with BG structure after Secco etching. The inset of Fig. 2 is the cross-sectional TEM image and the diffraction pattern of laser-crystallized poly-Si thin films of BG devices.

in lateral dimension were formed in the channel region, while small and fine grains were located near the edges of the BG. For the short channel length with the proper thicknesses of gate
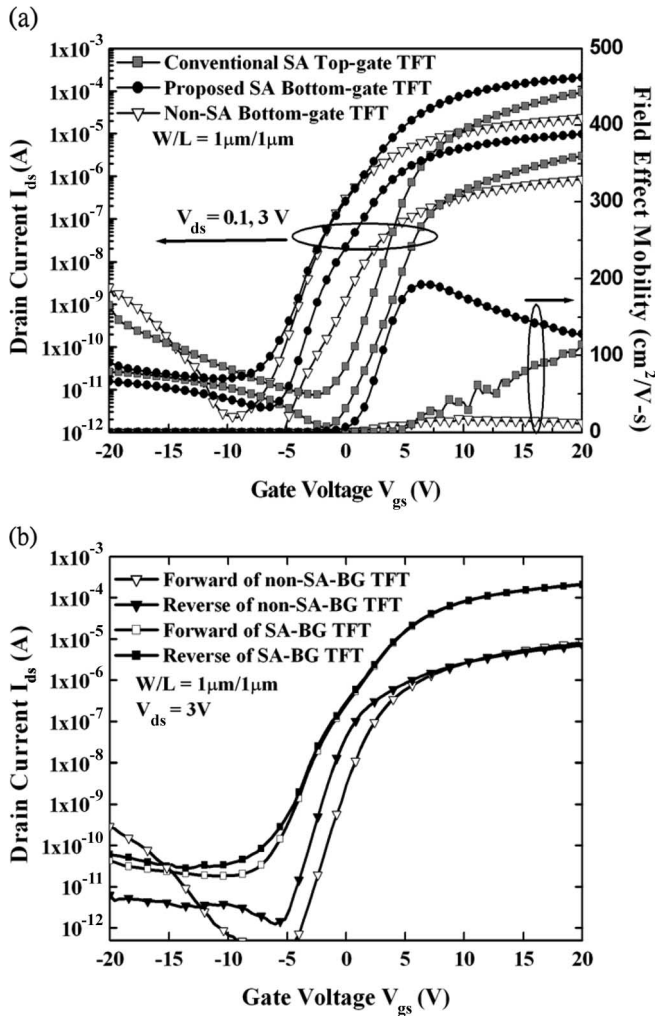
Fig. 3. (a) $I–V$ curves of SA-BG TFT with lateral silicon grain, non-SA-BG TFT, and conventional TG TFT. (b) Experimental measured bidirectional transfer characteristics of SA-BG TFT and non-SA-BG TFT under the polarities of the source and drain are interchanged.

TABLE I
MEASURED ELECTRICAL CHARACTERISTICS OF SA-BG TFTS WITH LATERAL GRAIN GROWTH AND CONVENTIONAL ONES. THE THRESHOLD VOLTAGE WAS DEFINED AS THE GATE VOLTAGE REQUIRED TO ACHIEVE A NORMALIZED DRAIN CURRENT OF $I_{ds} = (W/L) \times 10^{-8}$ A AT $V_{ds} = 0.1$ V. THE FIELD-EFFECT MOBILITY AND SUBTHRESHOLD SWING WERE EXTRACTED AT $V_{ds} = 0.1$ V, AND THE I_{ON}/I_{OFF} CURRENT RATIO WAS DEFINED AT $V_{ds} = 3$ V

TFT Structures (W = L = 1 μm)	Threshold Voltage (V)	Field-Effect-Mobility (cm^2/Vs)	Standard Deviation of Field-Effect-Mobility	Subthreshold Swing (V/dec)	On/Off Current Ratio
Proposed SA Bottom-Gate	-0.77	193	11.2	1.19	1.14 x10^7
Conventional non-SA Bottom-Gate	1.70	17.8	13.7	1.25	1.07 x10^7
Conventional SA Top-Gate	3.33	103	40.1	1.26	1.75 x10^7

one at the corner, were easier to be controlled for the wider range from 430 to 510 mJ/cm^2.

Typical transfer characteristics of SA-BG TFTs, conventional non-SA-BG TFTs, and SA-TG ones for $W = L = 1$ μm are shown in Fig. 3(a). Table I lists the average values of several important electrical characteristics of these three different TFTs. Owing to the uniformly large transverse grains grown in the channel region and SA source/drain to the BG, this proposed SA-BG TFTs exhibited better electrical characteristics with field-effect-mobility of 193 cm^2/V · s. Although the poly-Si grain structure in the channel region is similar in the SA-BG and non-SA-BG TFTs after ELC. However, after the lithography process of defining the source/drain regions, the lateral grain structure is still symmetric above the gate electrode in the SA TFTs, while the grain structure becomes asymmetric in the channel region, and there is an offset region in the conventional non-SA TFTs due to the misaligment process effect. In consequence, for the non-SA TFTs, because small and fine grains are near the edges of BG and the series resistance of the offset region is large, the non-SA-BG TFTs display lower field-effect mobility, and lower on-current [21]. Fig. 3(b) shows the transfer characteristics of SA-BG TFTs and non-SA-BG ones under both the forward- and reverse-measurement modes. The symmetric electrical characteristics confirmed that the proposed TFT is a SA gate structure. Moreover, to study the uniformity of these three different TFTs performance, 20 TFTs for the optimal laser-irradiation condition are measured. SA-TG TFTs display the worst uniformity which the mobilities range from 45 to 285 cm^2/V · s owing to the nonuniform grain distribution in the SLG regime. As for the BG devices, the mobilities of the SA-BG TFTs range from 170 to 210 cm^2/V · s, but for the non-SA BG-TFTs, the mobilities range from 8.5 to 60 cm^2/V · s. It is found that the variation range of mobility is similar about 50 cm^2/V · s. But for the calculation of nonuniformity, our definition of nonuniformity is (maximum mobility − minimum mobility)/(average mobility). As a result, the nonuniformity of non-SA-BG device is worse from the lower average mobility. The standard deviation of field-effect

electrode, gate oxide, and channel layers using this crystallization, only single-grain boundary perpendicular to the channel direction is also observed by TEM image, shown in the inset of Fig. 2. It has been reported that lateral thermal gradient could arise from the heat generated at moving solid–melt interfaces [9], [20]. In this experiment, as a proper excimer laser irradiation was performed on the a-Si thin film with BG structure, the laser-energy densities could cause complete melting of 1000-Å-thick silicon thin film in the channel region but partial melting of the thicker a-Si film near the edges of the BG. Therefore, the lateral grain growth started from the unmelted silicon solid seeds near the BG corner and extended toward the completely melted region until the solid–melt interface from opposite direction impinged. If the channel region, i.e., BG plateau, were arranged in a proper distance, there were two columns of longitudinal grains colliding in the middle of the channel region without any spontaneous nucleation. Thus, the grain boundaries in the channel region could be controlled and reduced. Moreover, the process window could be broaden because the laser-energy densities, between completely melting silicon thin film in the channel but partially melting the thicker

mobility for these three different TFTs is listed in Table I. It could be concluded that SA-BG TFTs exhibit better characteristics and improved uniformity based on the lateral grain growth and SA structure.

IV. CONCLUSION

High-performance SA-BG LTPS TFTs have been fabricated by ELC with backside exposure. Consequently, besides the high field-effect mobility, symmetric electrical characteristics and good device uniformity are achieved owing to the artificially controlled lateral grains with SA structure. The SA-BG TFTs are, therefore, promising for future system-on-panel applications.

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