# On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs

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Abstract—This letter reports a new mechanism for the enhanced impact-ionization rate  $(I_{sub}/I_d)$  present in shortchannel uniaxial strained p-MOSFETs. Through the pinch-off voltage  $(V_{dsat})$ , we have assessed the impact of strain on the maximum channel electric field. Due to the strain-enhanced mobility,  $V_{dsat}$  becomes lower, resulting in the observed  $V_g$ -dependent enhancement in  $I_{sub}/I_d$ . This mechanism needs to be considered when one-to-one comparisons of the hot-carrier effect between strained and unstrained devices are made.

Index Terms—Hot-carrier effect, impact ionization, strainedsilicon, substrate current.

### I. INTRODUCTION

S STRAINED-silicon is widely used in state-of-the-art CMOS technologies [1]–[4] to enable the mobility scaling [5], the hot-carrier effect is another important scaling issue that has to be considered for strained MOSFETs.

## II. RESULTS AND DISCUSSION

The hot-carrier effect is usually monitored by the substrate current  $(I_{sub})$  [6].  $I_{sub}$  results from the impact ionization caused by energetic carriers in the channel. Several authors [7]–[9] have reported the strain-induced enhancement of impact-ionization rate  $(I_{sub}/I_d)$ . Irisawa *et al.* [7] examined long-channel strained MOSFETs and attributed the enhanced  $I_{sub}/I_d$  to the reduced bandgap energy. Whether there is any other physical mechanism responsible for the strain-enhanced impact ionization merits further examination.

 $I_{\rm sub}$  has long been closely related to the maximum channel electric field  $(E_m)$  near the drain [6]. With the strain-induced enhancement of carrier mobility,  $E_m$  may vary and may play a crucial role in one-to-one comparisons of the hot-carrier effect between strained and unstrained devices. In this letter, we investigate the substrate current in short-channel uniaxial strained p-MOSFETs and report a new mechanism responsible for the strain-enhanced impact ionization.

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Co-processed strained and unstrained p-MOSFETs are investigated in this study. The strained devices were fabricated by state-of-the-art process-induced uniaxial strained-silicon technology featuring SiGe source/drain and compressive contact etch stop layer (CESL) [10]. For the transistors with gate length  $L_{\text{gate}} = 65$  nm, the saturation drain current ( $I_d$ ) of the strained device is improved more than 85% as compared with its control counterpart.

Fig. 1(a) shows the gate-bias dependence of the measured  $I_{\rm sub}$  for the strained and control devices. Typical bell-shape characteristics can be seen. Fig. 1(b) shows that the impactionization rate of the strained device is larger than that of the unstrained one. The strain-induced enhancement in  $I_{\rm sub}/I_d$  increases with gate bias.

According to the lucky electron model [11]

$$\frac{I_{\rm sub}}{I_d} \propto e^{-\frac{\varphi_i}{q\lambda E_m}} \tag{1}$$

where  $\varphi_i$  is the energy required for impact ionization, and  $\lambda$  is the mean-free path. Although the strain-induced reduction in bandgap energy (hence,  $\varphi_i$ ) may raise the impact-ionization rate for the strained device [7], it cannot explain the gatebias dependence of the enhancement in  $I_{sub}/I_d$  as observed in Fig. 1(b).

The  $V_g$  dependence of  $I_{sub}/I_d$  stems from  $E_m$ , the maximum channel electric field.  $E_m$  can be modeled [6] as

$$E_m = \frac{V_d - V_{\rm dsat}}{l} \tag{2}$$

where  $V_{\rm dsat}$  is the potential at the pinch-off (i.e., saturation) point in the channel, and l is the characteristic length in the pinch-off region. Although  $E_m$  cannot be directly measured, the impact of strain on  $E_m$  can be assessed through  $V_{\rm dsat}$ . From the output resistance ( $R_{\rm out}$ ) versus  $V_d$  plot (Fig. 2),  $V_{\rm dsat}$  can be extracted by linear extrapolation because  $R_{\rm out}$  is proportional to  $V_d - V_{\rm dsat}$  in the channel-length modulation region [12], [13]. It can be seen from Fig. 2 that the strained device has a smaller  $V_{\rm dsat}$  than its control counterpart for a given gate voltage overdrive ( $V_{\rm gst}$ ).

Fig. 3 shows the  $V_{\rm gst}$  dependence of the extracted  $V_{\rm dsat}$ . The strain-induced reduction (i.e., the discrepancy between the control and strained devices) in  $V_{\rm dsat}$  increases with gate bias. It explains why in Fig. 1(b) the strain-induced enhancement in  $I_{\rm sub}/I_d$  increases with gate bias.

The strain-reduced  $V_{dsat}$  results from the enhanced mobility in the strained device. The enhancement in mobility

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1E-6 PFET =65nm gate 1E-7 1E-8  $I_{sub}(A)$ 1E-9 1.8V 1E-10 |V<sub>d</sub>|=1.6V solid : Control |V<sub>d</sub>|=1.4V dash: Strained 1E-11 0.8 0.0 0.2 0.4 0.6 1.0 1.2 1.4  $|V_{gst}|$  (V) (a) 1E-3 PFET L<sub>gate</sub>=65nm 1E-4 |V<sub>d</sub>|=1.8V 1E-5 b dus 1E-6 1E-7 |V<sub>d</sub>|=1.6∨ solid : Control dash: Strained |V<sub>d</sub>|=1.4V 1E-8 0.6 0.8 1.0 1.2 0.0 0.2 0.4 1.4  $|V_{gst}|$  (V) (b)

Fig. 1. (a)  $I_{\rm sub}$  versus gate voltage overdrive  $(V_{\rm gst})$  for the strained and control devices with various drain biases. (b)  $I_{\rm sub}/I_d$  versus  $V_{\rm gst}$  showing the strain-enhanced impact ionization.

corresponds to an increase in slope of the carrier velocity versus lateral field characteristic [14] and a reduction in the critical field ( $E_{sat}$ ) for velocity saturation [15], [16]. Since  $V_{dsat}$  is essentially determined by  $E_{sat}$  in the high  $V_{gst}$  regime [6], [16], the impact of strain on  $V_{dsat}$ , as shown in Fig. 3, becomes significant with increasing gate bias.

The strain-reduced  $V_{\rm dsat}$  enhances the impact-ionization rate and needs to be considered in monitoring the hot-carrier effect of the strained device. Fig. 4 shows that, with the extracted  $V_{\rm dsat}$  from Fig. 3, the same  $I_{\rm sub}$  data (Fig. 1) reduce to a single straight line for the control and strained devices, respectively, when  $\ln(I_{\rm sub}/I_d)$  is plotted against  $1/(V_d - V_{\rm dsat})$  as predicted by (1) and (2). In Fig. 4, the slope of the strained device is about 9.5% smaller than that of the unstrained device. Since the slope is proportional to  $\varphi_i l/\lambda$ , we can estimate from Fig. 4 that the upper bound of the bandgap change due to strain is 9.5%. The reduced slope for the strained device has also been reported by Irisawa *et al.* [7], who attributed it mainly to the reduced



Fig. 2.  $R_{\rm out}$  versus  $V_d$  plot can be used to determine  $V_{\rm dsat}$ . The strained device has a smaller  $V_{\rm dsat}$  than its control counterpart for a given  $V_{\rm gst}$ .



Fig. 3. Impact of strain on  $V_{dsat}$  increases with  $V_{gst}$ .

bandgap energy. Our expected value of the bandgap change is between 5% to 10%.

## **III.** CONCLUSION

In conclusion, we report a new mechanism for the enhanced impact ionization present in short-channel uniaxial strained p-MOSFETs. Due to the strain-enhanced mobility,  $V_{dsat}$  becomes lower, resulting in the observed  $V_g$ -dependent enhancement in  $I_{sub}/I_d$ . This mechanism is important and needs to be considered when one-to-one comparisons of the hot-carrier effect between strained and unstrained devices are made.



Fig. 4. Strained-reduced  $V_{\rm dsat}$  needs to be considered in the construction of the  $\ln(I_{\rm sub}/I_d)$  versus  $1/(V_d-V_{\rm dsat})$  plot for monitoring the hot-carrier effect of the strained device.

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