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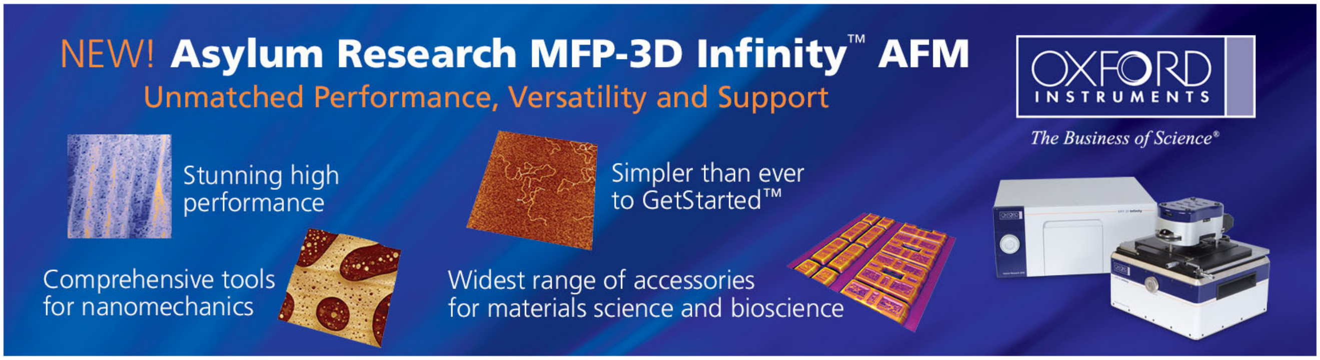

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Observation of the negative differential capacitance in Schottky diodes with InAs quantum dots near room temperature

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The negative differential capacitance (NDC) of Schottky diodes with the layers of InAs quantum dots (QDs) has been clearly observed near room temperature. A simple model involving two zero-dimensional quantum states is proposed to explain the NDC behavior. The simulation results show that the NDC is caused by the fast charging-discharging process in the second states of QDs. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2752737]

In these years the investigation of structures with self-assembled quantum dots (QDs) draws increasing attention because of their potential application on nanoelectronics. Because of the ability to accumulate charges in the QDs, heterojunctions with QDs show interesting features in capacitance-voltage (*C*-*V*) dependences.[1–6] Most of these reports presented the experimental results of the *C*-*V* dependences and the parameters of QDs, such as concentration, energy levels, and capture cross sections, were determined accordingly. The method for calculating the capacitance dependence was proposed to compare with the experimental results.[7–9] Particularly, in the work of Chiquito *et al.*,[9] a negative differential capacitance (NDC) characteristic was observed at low temperatures and a model was provided to explain the results. However, in the consideration of practical application, such as quantum dot memory devices, the operation temperature has to be much higher. In this letter, the effects of InAs QDs on the *C*-*V* characteristics of the Schottky diodes are investigated. Multilayers InAs QDs and dots-in well (DWELL) in GaAs matrix were built into the space-charged region (SCR) of the Schottky diode. Both samples show clear NDC in their capacitance-voltage characteristics near room temperature. A simple model involving two states in QDs to explain the NDC characteristics is also proposed.

Two samples were grown on n^+-GaAs (100) substrates by molecular beam epitaxy using a Varian GEN II system equipped with an arsenic cracker cell. Detailed structures are shown in Fig. 1. As shown in Fig. 1(a), sample A (LM3654) contains five layers InAs QDs embedded in GaAs matrix. The spacer between QDs layers is an 80 nm lightly doped ($n = 6.4 \times 10^{15}$ cm^{-3}) GaAs. Sample B (LM3677) consists of three layers of InAs/In$_{0.15}$Ga$_{0.85}$As DWELL spacing by 50 nm n^--GaAs, as shown in Fig. 1(b). The growth conditions of InAs QDs in two samples are detailed in the following: For sample A, the growth temperature, InAs growth rate and arsenic (As$_4$) beam-equivalent pressure were about 485 °C, 0.05 ML/s, and 3×10^{-5} torr, respectively. According to a previous study on the sample grown at the same condition, the area density of the QDs was about 1×10^{11} cm^{-2}. On the other hand, for sample B, the corresponding growth conditions were 520 °C, 0.033 ML/s, and As$_2 = 1.5 \times 10^{-5}$ torr and the area density of the QDs was about 1×10^{10} cm^{-2}. The ground state transition energies were 1.23 and 1.11 eV with full width at half maximum of 74 and 50 meV for samples A and B, respectively, given by the low temperature (~20 K) photoluminescence measurement. The samples were then processed into 400×400 μm^2 Schottky diodes as follows: The Ti/Au (20/100 nm) Schottky contacts were made with a standard photolithography, e-gun evaporation, and lift-off. Ohmic contacts were formed by indium soldering on the back side of wafer.

Capacitance measurements were carried out by means of the capacitance bridge at a frequency of 1 MHz at different temperatures and bias voltages. The measurement results having unusual *C*-*V* dependences are shown in Fig. 2. Specifically, in the range of a small forward biases (between 0.3 and 1.0 V), the NDC characteristics were observed clearly in the both samples. As we can see in the Fig. 2(a), for sample

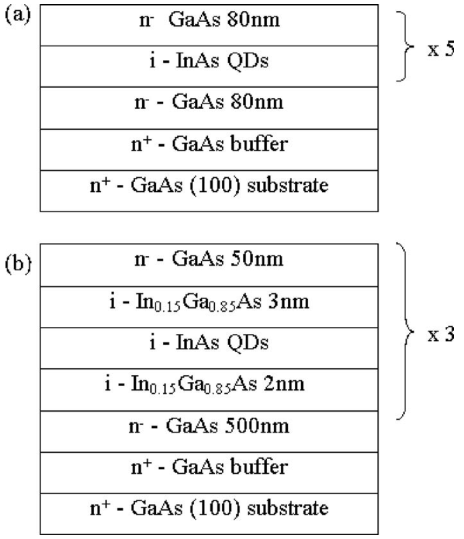

FIG. 1. Grown sample structures: (a) sample A with InAs QDs in the GaAs matrix and (b) sample B with InAs QDs in InGaAs QWs.

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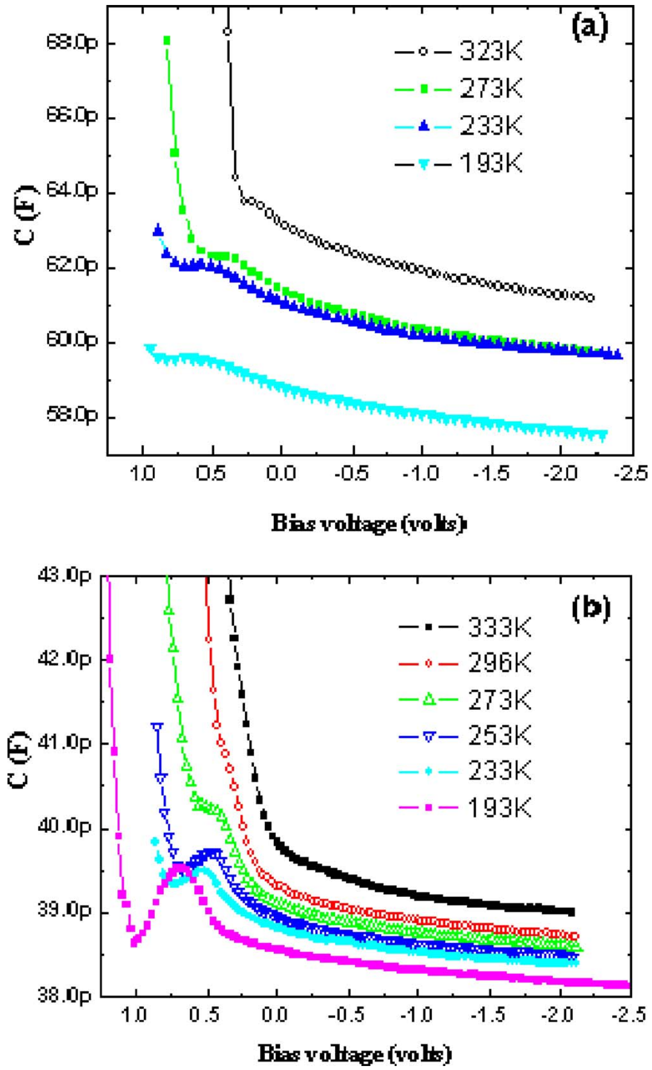

FIG. 2. (Color online) Measured capacitance-voltage curves for (a) sample A and (b) sample B.

A (the InAs QDs in GaAs matrix), the NDC characteristics happened below about 233 K but did not get more significant at 193 K. However, for sample B (the InAs QDs in InGaAs QWs), the NDC characteristics became clear below 253 K and the peaks went sharper as the temperatures lowered, as shown in Fig. 2(b). As sample A had higher density and more layers of QDs than sample B did, we suspect that the correlation between NDC and number of dots is not straight forward. It is also worth noting that the concentration of *n*-typed doping in bulk GaAs was only 6.4×10^{15} cm^{-3}. So, the negative charge accumulated in QDs can play a role in the potential distribution under certain applied voltages. Hence, we have to calculate the band profile taking the QDs states into account.

Here we proposed a simple model for the *C*-*V* dependences of the Schottky diode with only one layer of QDs embedded at a distance of L_{dot} from the metal contact, as shown schematically in Fig. 3. The width of the QDs layer is disregarded for simplicity, such that spatial distribution of QDs can be modeled by means of a delta function. Poisson's equation with the boundary conditions is

$$\frac{d^2\varphi}{dx^2} = -\frac{eN_d}{\varepsilon\varepsilon_0} + \frac{en_{\text{dot}}}{\varepsilon\varepsilon_0}\delta(x - L_{\text{dot}}), \qquad (1)$$

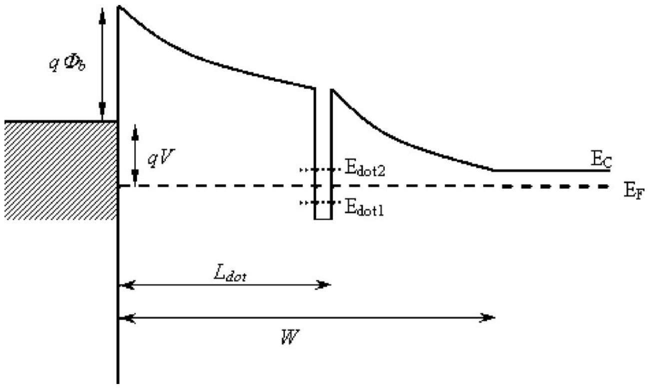

FIG. 3. Band profile of a Schottky diode containing a single layer of QDs for our simulation.

$$\varphi(w) = 0, \qquad (2)$$

$$\left.\frac{d\varphi}{dx}\right|_{x=w} = 0. \qquad (3)$$

The charge density, in the right-hand side of Poisson's equation, consists of two components: N_d is the constant charge density of ionized impurity and n_{dot} is the charge density accumulating in QDs. The solution of Eq. (1) can be obtained with boundary conditions (2) and (3),

$$\varphi(x) = -\frac{eN_d}{2\varepsilon\varepsilon_0}(x-w)^2 + \begin{cases} 0, & x > L_{\text{dot}} \\ \dfrac{en_{\text{dot}}}{\varepsilon\varepsilon_0}(L_{\text{dot}} - x), & x < L_{\text{dot}}. \end{cases} \qquad (4)$$

With a large enough reverse bias, the presence of QDs layer does not make any effect on the potential profile, because the energy levels of QDs are far above the quasi-Fermi level and QDs states are unoccupied. That is, the n_{dot} in formula (4) is nearly zero and thereby the $\varphi(x)$ would tend to be classical.[8,9] When the applied reverse voltage decreases, the Fermi level E_f approaches to the first energy level E_{dot1} and it leads to filling ground energy states with electrons. As a result, n_{dot1} increases as follows:

$$n_{\text{dot1}}(V_{\text{dot}}) = N_{\text{dot}}\frac{\eta_1}{1+\exp((E_F - E_{\text{dot 1}} - eV_{\text{dot}})/kT)}, \qquad (5)$$

where N_{dot} is the effective density of QDs and η_1 is the maximum number of electrons captured to the ground state (E_{dot1}) of each QD. Furthermore, by using the condition $\varphi(0) = -\Phi_B + V$ (where the Φ_B is the Schottky barrier height), we can obtain the equation

$$-\Phi_B + V = -\frac{eN_d}{2\varepsilon\varepsilon_0}w^2 + \frac{en_{\text{dot 1}}}{\varepsilon\varepsilon_0}L_{\text{dot}}. \qquad (6)$$

Thus, voltage V as a parameter defining SCR width is done in Eq. (6). To obtain the to-be-solved equation, we place Eq. (5) into Eq. (6) and find

$$w^2 - \frac{2\varepsilon\varepsilon_0}{eN_d}(\Phi_B - V) - \frac{2N_{\text{dot}}}{N_d} \times \frac{\eta_1}{1+\exp((E_F - E_{\text{dot}} - (e^2N_d/2\varepsilon\varepsilon_0)(L_{\text{dot}} - w)^2)/kT)} \times L_{\text{dot}} = 0. \qquad (7)$$

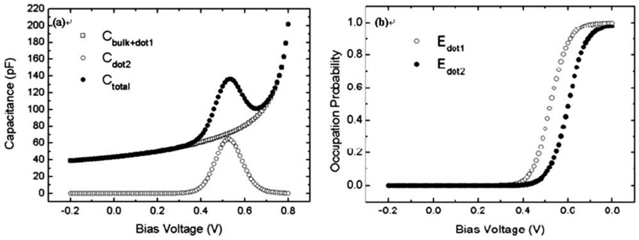

FIG. 4. (a) Calculated C-V dependence and (b) occupation probabilities of E_{dot1} and E_{dot2}.

The solution of Eq. (7) can be obtained by simply using numerical method. Afterward, we can calculate the bulk capacitance with the depletion width w,

$$C_{\mathrm{bulk+dot\ 1}} = \frac{\varepsilon\varepsilon_0}{w}. \tag{8}$$

Actually, when measuring capacitance-voltage characteristic, we applied a constant voltage V and an alternative testing signal $V(\omega)$ at measuring frequency ω to the diode. As a result of applying of the static voltage, the QDs ground state (E_{dot1}) accumulated negative charges due to electron filling. Most of these charges could not follow alternative testing signal V_ω due to the long capture/escape times (τ_1) for the first QDs energy level (in the range of 10^{-3}–10^{-6} s,[1,2,10] which is much slower than the testing signal frequency 1 MHz. However, it could be a different case when the applied static voltage V increased and the quasi-Fermi level around QDs approached to the second energy level (E_{dot2}) in QDs. Because the capture/escape time for the second states (E_{dot2}) in QDs could be much shorter, some of the electrons in the second states can catch up with the charging-discharging process of the testing signal V_ω. So, to take this effect into account we have to include an additional capacitance C_{dot2}:[8,9]

$$C_{\mathrm{dot\ 2}} = e\frac{dn_{\mathrm{dot\ 2}}}{dV}. \tag{9}$$

Here, we have assumed for simplicity that all the electrons in the second states can follow the frequency of the testing signal V_ω. The n_{dot2} can be obtained with the formula similar to that of n_{dot1}

$$n_{\mathrm{dot\ 2}}(V_{\mathrm{dot}}) = N_{\mathrm{dot}}\frac{\eta_2}{1+\exp((E_F - E_{\mathrm{dot\ 2}} - eV_{\mathrm{dot}})/kT)}. \tag{10}$$

Accordingly, the total capacitance is

$$C = C_{\mathrm{bulk+dot\ 1}} + C_{\mathrm{dot\ 2}}. \tag{11}$$

A typical numerical simulation is plotted in Fig. 4, where the used parameters are $T=233$ K, $N_{\mathrm{dot}}=1\times 10^{10}$ cm^{-2}, $L_{\mathrm{dot}}=1\times 10^{-5}$ cm, $E_1=-0.2$ eV, $E_2=-0.16$ eV, $\Phi_B=0.81$ V, $\eta_1=2$, and $\eta_2=4$. As we can see in Fig. 4(a), the total capacitance consists of two parts; the bulk capacitance ($C_{\mathrm{bulk+dot1}}$) and the E_{dot2} charging-discharging capacitance (C_{dot2}). Clearly, the NDC characteristic is contributed from C_{dot2}, which is caused by the fast charging-discharging process in the second states of QDs. With the calculated occupation probability versus bias voltage shown in Fig. 4(b), the reason for happened NDC becomes obvious. The C_{dot2} is the differentiation of n_{dot2} to the bias voltage [Eq. (9)], so the NDC peaks happen when the E_{dot2} is half-filled. More importantly, due to the discrete density of states in QDs, the occupation probability saturates as it comes close to 1, which makes C_{dot2} lower down to zero. This tells us that the NDC characteristics are basically a zero-dimensional effect.

Comparing the Figs. 2(b) and 4(a), our calculations are qualitatively consistent with the experimental results of sample B with lower density QDs. In the case of sample A, however, because of its high density of QDs, the accumulation of electrons in E_{dot1} influences the band profile significantly and decreases the voltage change of QDs (V_{dot}), which seriously broadens the NDC peaks, as our calculation shows (not plotted here). That is why we saw much weaker NDC peaks in our measurement [Fig. 2(a)]. Other effects having not been taken into account, such as the inhomogeneous of QDs ensemble and multiple layers of QDs, could also weaken the NDC characteristics. Besides, we have also calculated the temperature-dependent *C*-*V* with the same model. The simulation results show that the NDC peaks broaden as the temperature increases, due to the temperature dependence in the Fermi-Dirac distribution function. However, the peaks keep at the same bias voltage at different temperatures, which is not consistent with the experimental data. In Fig. 2, one can see that the peaks shifted to higher bias voltage as the temperature lowered. We believe that the shifting mainly comes from that the Schottky barrier height enlarges as the temperature increases (which is not included in our simulation), but other temperature-dependent parameters, such as band gap narrowing and quantum dots level shifting, may also play a role in this and so further investigations are necessary.

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