9.5 GHz GaInP/GaAs HBT divide-by-two frequency divider using super-dynamic D-type flip–flop technique

H.-J. Wei, C. Meng, Y.W. Chang and G.-W. Huang

A frequency divider with super-dynamic D-type flip–flop is demonstrated in 2 μm GaInP/GaAs HBT ($f_T = 40$ GHz) technology. By biasing the HBT devices around the peak transit-time frequency (f_T), the operating frequency of a D-FF with ECNFP (emitter-coupled negative feedback pairs) can be improved. At a supply voltage of 5 V, a divide-by-two function of 9.5 GHz is achieved.

Introduction: As demands increase on higher data-rate communication systems, the speed of a D-type flip–flop plays an important role in most digital circuits. Use of circuit topology to compensate for the inherent limitations of the device was reported in [1–3]. The super-dynamic D-type flip–flop with an ECNFP has the fastest speed. An ECNFP added to the regenerative pair has a trade-off between the limited voltage headroom and the DC current when operating near the peak of f_T. Originally, the super-dynamic structure was only demonstrated in the FET process. In this Letter, the design issues of a super-dynamic frequency divider using GaInP/GaAs HBT technology are discussed and successfully implemented. GaInP/GaAs HBT technology has several advantages, such as low base resistance, suppressed $1/f$ noise, accurate thin-film resistors with 50 Ω sheet resistance and semi-insulating GaAs substrate. In particular, the low base resistance is beneficial to the super-dynamic frequency divider when operating at limited voltage headroom and small internal voltage swing without noise immunity degradation.

Circuit design: The super-dynamic frequency divider consists of a single-ended input buffer, an output driver and a core master-slave D-type flip–flop. For the divide-by-two function, the slave output is cross-connected to the master input. Every D-latch is composed of a differential pair and a cross-coupled regenerative pair. Emitter couple logic (ECL) topology is employed to achieve the properties of high speed and low input sensitivity. Based on the concept of the HLO-FF (high-speed latching operation flip–flop) structure [1], ECNFPs are inserted in the regenerative pairs by the cascode manner to limit logic voltage swing to $R_L(I_{read} - I_{latch})/2$ and increase the maximum operating frequency. The logic information is stored only during the clock switching time, and then decays during the equilibrium state [2, 3]. An improved maximum speed also accompanies the minimum frequency limitation because D-FF operating behaviour becomes increasingly dynamic. A schematic of the super-dynamic D-type flip–flop is shown in Fig. 1.

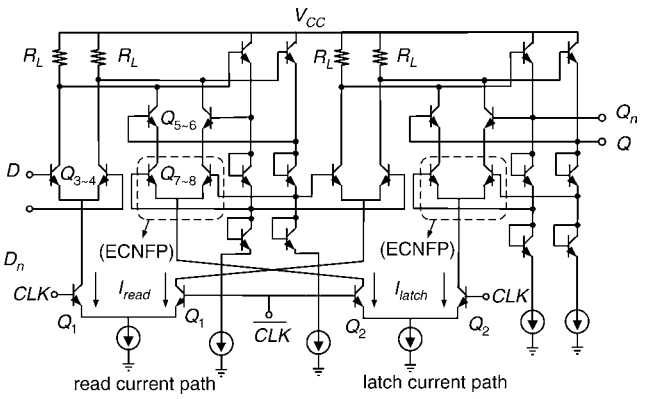

Fig. 1 *Schematic of super-dynamic D-type flip–flop*
$I_{read} = 2.5 \times I_{latch}$

Because the inserted ECNFPs have more transistors stacked in the latch path, the device size and DC current influence the output swing and the maximum speed of the HBT. As shown in Fig. 2, the speed of the HBT can be increased by increasing the current density until the Kirk-effect occurs. On the other hand, the parasitic emitter resistor decreases the small-signal gain, and then a larger voltage swing is required for driving the ECL [4]. The internal voltage swing is unfavourable to high-speed operation. Thus, the size of HBT operating at the higher frequency cannot be too small under the higher current density, especially in choosing the size of the transistors for the clock input. The other device sizes in the differential pairs and regenerative pairs with ECNFP can be reduced to reduce the parasitic capacitance of the loading.

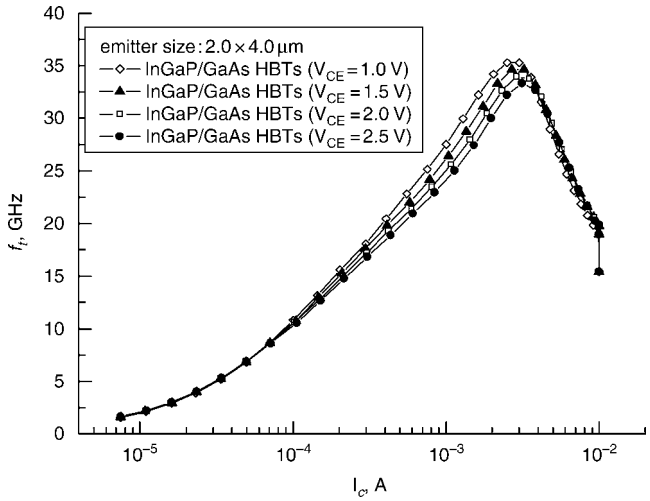

Fig. 2 *Measured transit time frequency (f_T) against collector current for various V_{CE}*
Emitter size: 2.0 × 4.0 μm

Experimental results: The size of the GaInP/GaAs HBT super-dynamic frequency divider including probing pads is 1.0 × 1.0 mm, and a die photo is shown in Fig. 3. HBT devices of 2 × 4 μm are only used for the clock transistors (Q_1) in the read current path. The rest of the HBT devices in the differential pairs (Q_3–Q_4), the regenerative pairs with ECNFP (Q_5–Q_8) and the clock transistors (Q_2) of the latch current path are 2 × 2 μm. At a supply voltage of 5 V, the transistors Q_1 and Q_2 of the clock pair with 0.20 and 0.17 mA/μm^2 operate around the peak transit-time frequency (f_T). Because the transistors (Q_5–Q_8) operate at lower frequency, their current density with the half of the transistor (Q_2) will not degrade the speed of the D-FF. Fig. 4 shows the input sensitivity power against the operating frequency. The super-dynamic frequency divider is able to work from 5.5 to 9.5 GHz. The lowest sensitivity level is only −45 dBm at a self-oscillating frequency of 8.05 GHz. The output spectrum with the maximum input frequency of 9.5 GHz is also shown in Fig. 4.

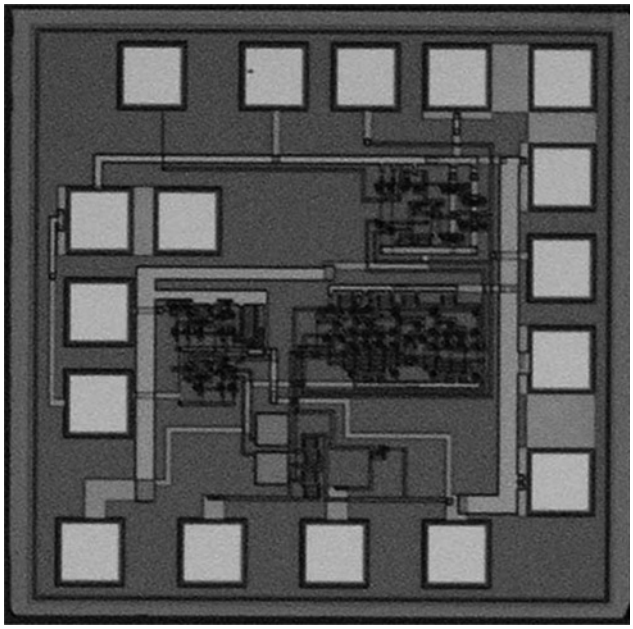

Fig. 3 *Die photo of GaInP/GaAs HBT super-dynamic frequency divider*
1.0 × 1.0 mm

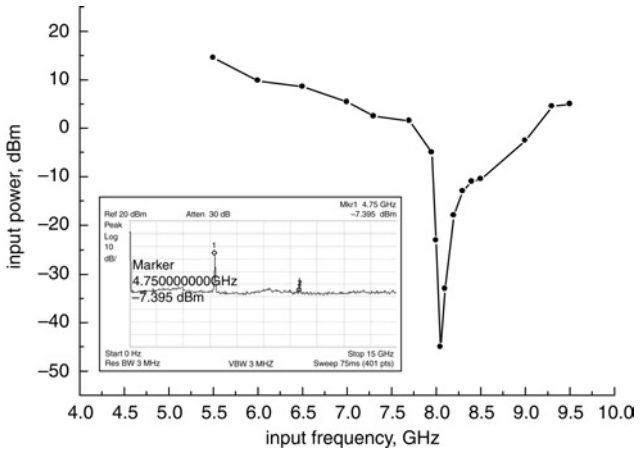

Fig. 4 *Measured input sensitivity of super-dynamic frequency divider (including output spectrum with input signal of 9.5 GHz)*

Conclusions: The design issues and performance of super-dynamic frequency dividers have been discussed and demonstrated using 2 μm GaInP/GaAs HBT technology. By biasing the HBT devices around the peak of f_T, the operating frequency range is 5.5–9.5 GHz at a supply voltage of 5 V. The experimental results show that the super-dynamic frequency divider using HBT is a good candidate for high-speed applications.

Acknowledgments: This work is supported by the National Science Council of Taiwan, Republic of China, under contract numbers NSC 95-2752-E-009-001-PAE, NSC 95-2221-E-009-043-MY3, by the Ministry of Economic Affairs of Taiwan under contract number 95-EC-17-A-05-S1-020, by the MoE ATU Program under contract number 95W803, and by the National Chip Implementation Center (CIC).

13 March 2007
Electronics Letters online no: 20070727
doi: 10.1049/el:20070727

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