Transient Charging and Discharging Behaviors of Border Traps in the Dual-Layer HfO_2/SiO_2 High-κ Gate Stack Observed by Using Low-Frequency Charge Pumping Method

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***Abstract*—Transient charging and discharging of border traps in the dual-layer HfO_2/SiO_2 high-κ gate stack have been extensively studied by the low-frequency charge pumping method with various input pulse waveforms. It has been demonstrated that the exchange of charge carriers mainly occurs through the direct tunneling between the Si conduction band states and border traps in the HfO_2 high-κ dielectric within the transient charging and discharging stages in one pulse cycle. Moreover, the transient charging and discharging behaviors could be observed in the time scale of 10^{-8}–10^{-4} s and well described by the charge trapping/detrapping model with dispersive capture/emission time constants used in static positive bias stress. Finally, the frequency and voltage dependencies of the border trap area density could also be transformed into the spatial and energetic distribution of border traps as a smoothed 3-D mesh profiling.**

***Index Terms*—Border trap, hafnium oxide, high-κ dielectric, low-frequency charge pumping method, transient charging effect, transient discharging effect.**

I. INTRODUCTION

AS THE MOORE'S law continues to drive the aggressive scaling of gate dielectric thickness, it is becoming increasingly clear that we are approaching the materials' limit of conventional SiO_2-based ultrathin oxides [1]. In order to avoid the intolerable tunneling leakage and power consumption in the ultrathin oxides, high dielectric permittivity (high-κ) dielectric has been proposed to offer thicker dielectric physical thickness while maintaining the same equivalent oxide thickness (EOT) in electrical properties. Among those investigated high-κ dielectrics, Hf-based high-κ dielectrics (including HfO_2, HfSiO, and HfSiON) have been recognized as the most promising candidates to be used in the advanced sub-45-nm technology nodes so as to extend the scaling limit. Moreover, the process optimization, dielectric composition, gate stack structure, and reliability issues of Hf-based high-κ dielectrics have been studied with a great intensity and variety [2]–[5]. However, it has been reported that there is plenty of preexisting bulk traps in the HfO_2 high-κ dielectrics, thus leading to the critical reliability issue of threshold voltage instability induced by charge trapping and detrapping.

First, the hysteresis of capacitance–voltage curves and the V_t shift determined by static I_d–V_g characteristics have been widely used to study the slow high-κ traps from which the trapped charge carriers could not detrap immediately [6], [7]. Then, the pulse I_d–V_g technique and charge pumping method have been proposed and employed to investigate the fast high-κ traps which could instantly capture and emit the charge carriers by tunneling through the thin interfacial oxide [8]–[10]. The tunneling model through the thin interfacial oxide is similar to that of tunneling into near-interface oxide traps in the heavily irradiated SiO_2 that has already been studied and proposed [11]–[16]. These near-interface oxide traps are defined as the oxide traps located near the interface that can instantly exchange charge carriers with the underlying Si substrate through direct tunneling [17], [18] and are suggested to be named as "border traps" to be distinguished from the conventional interface states and oxide traps [19]. Similarly, the detected fast high-κ traps by the charge pumping method measured at low frequencies could also be defined as the preexisting high-κ traps located near the high-κ/SiO_2 interface that can instantly exchange charge carriers with the underlying Si substrate through direct tunneling, and be called the border traps in the high-κ dielectrics to be distinguished from other fast high-κ traps (which have not been detected, depending on the measurement frequency [19]). This low-frequency charge pumping method has been demonstrated as an effective tool to determine the bulk trap density and trap generation rate in the high-κ dielectric [20], and the initial high-κ bulk trap density is highly associated with the reliability and yield issues from the viewpoint of dielectric breakdown [21]. The correlation between the stress-induced leakage current and high-κ bulk trap density has been shown in good agreement to evaluate the time-to-breakdown t_{BD} in time-dependent dielectric breakdown tests [22], [23]. Furthermore, the charge pumping method with varying frequency has also been used to profile the spatial

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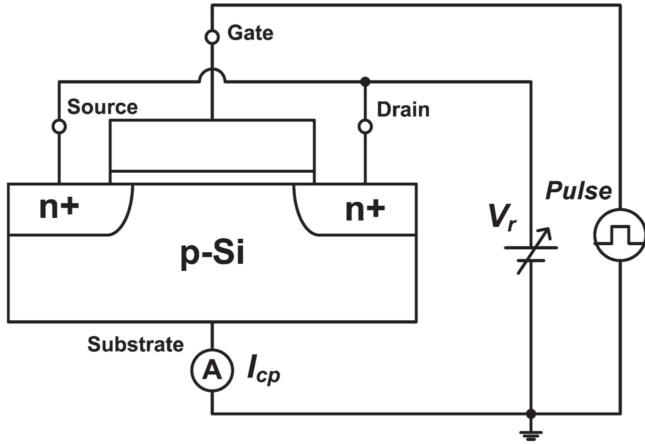

Fig. 1. System setup of the charge pumping method. The gate of an NMOS device is connected to a pulse generator, and a reverse bias voltage V_r is applied to the source and drain, while the charge pumping current I_{cp} is measured at the grounded substrate.

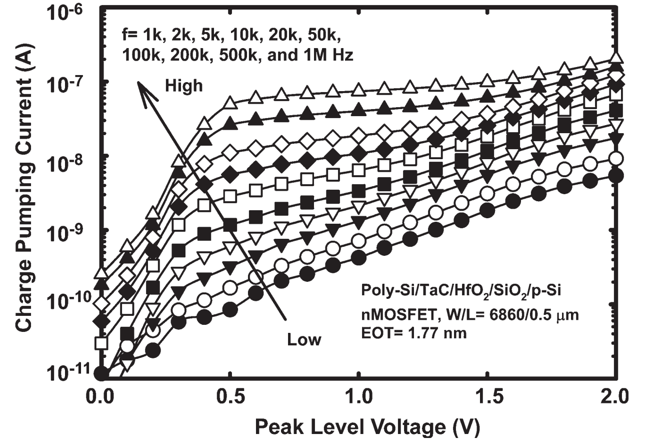

Fig. 2. Charge pumping current I_{cp} of the poly-Si/TaC/HfO_2/SiO_2/p-Si high-κ gate stack with EOT $= 1.77$ nm as a function of peak level voltage V_{peak} at various frequencies.

distribution of trapping centers and to determine the trap generation location in the high-κ/oxide gate stack [24], [25].

In this paper, the transient charging and discharging behaviors of the border traps in the HfO_2/SiO_2 high-κ gate stack have been extensively studied by the low-frequency charge pumping method with various input pulse waveforms. Furthermore, an elastic direct tunneling model through trapezoidal potential barriers has been proposed to profile the spatial and energetic distribution of the border traps in the HfO_2/SiO_2 high-κ gate stack as a smoothed 3-D mesh surface profiling.

II. Experiment and Analysis Method

NMOS devices with poly-Si/TaC/HfO_2/SiO_2/p-Si high-κ gate stack were fabricated using the conventional CMOS process technology. The thin interfacial oxide SiO_2 ($\sim$1.0 nm) was thermally grown on 300-mm p-type silicon wafers, followed by the deposition of HfO_2 ($\sim$3.2 nm) high-κ gate dielectric using atomic layer deposition technique. Then, an n-type metal gate electrode TaC ($\Phi_m \sim 4.3$ eV on HfO_2 [26]) was deposited using physical vapor deposition method, and the poly-Si gate served as the capping layer to ensure the process compatibility. Finally, the high-κ gate stack was patterned using lithography and dry etching technologies, and the EOT of the above HfO_2/SiO_2 high-κ gate stack was extracted as 1.77 nm by using the C–V simulation program which has taken the quantum effect into consideration [27].

An extension of the well-known charge pumping method to low frequencies has been employed to distinguish the border traps in the HfO_2/SiO_2 high-κ gate stack from the conventional interface states at the SiO_2/Si interface. Fig. 1 shows the measurement system setup of the charge pumping method. The gate of an NMOS device is connected to a pulse generator, and a reverse bias voltage ($V_r = 50$ mV) is applied to the source and drain, while the charge pumping current I_{cp} is measured at the grounded substrate. By applying a series of input pulse waveforms with various frequencies to the gate, the charge pumping current due to the contributions from both the interface states and border traps could be measured at the substrate. Then, each of the individual contributions could be separated by analyzing the recombined trapped charge density per cycle as a function of the frequency of input pulse waveform. If there is no contribution from the border traps, the recombined trapped charge density per cycle would be constant over a wide frequency range. However, in the presence of border traps, the recombined trapped charge density per cycle would increase with the decreasing frequency due to the longer time for charge carriers to exchange between the interface states and border traps located spatially near the interface. In this paper, the low-frequency charge pumping method with various input pulse waveform parameters has been employed to study the transient charging and discharging behaviors of border traps, the related tunneling physical model, and the spatial and energetic distribution of border traps in the dual-layer HfO_2/SiO_2 high-κ gate stack.

III. Results and Discussion

A. Low-Frequency Charge Pumping Results

Fig. 2 shows the charge pumping current I_{cp} of the high-κ NMOS device as a function of peak level voltage V_{peak} at various frequencies. As can be seen, different I_{cp} curves could be observed at high and low frequencies. At low frequencies, the I_{cp} continued to increase exponentially with the increasing peak level voltage, and this particular phenomenon could not be seen in typical SiO_2 and SiON ultrathin oxides. Fig. 3 shows the trapped charge density N_t of the dual-layer HfO_2/SiO_2 high-κ gate stack as a function of peak level voltage V_{peak} at frequencies ranging from 1 k to 1 MHz, and the inset illustrates the definition of input pulse waveform parameters such as the peak and base level voltages, pulse period, pulse width, and rise/fall time. The typical pulse waveform parameters are illustrated as follows if not specified: Duty cycle is 50%, rise time and fall time are both 100 ns, and peak and base level voltages are +2.0 and −1.0 V, respectively. The N_t detected at a specific frequency is calculated as

$$N_t = I_{\mathrm{cp}}/qfA_G \quad (1)$$

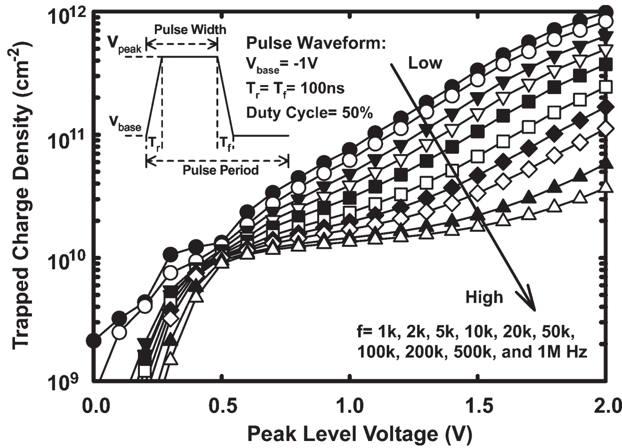

Fig. 3. Trapped charge density N_t of the dual-layer HfO_2/SiO_2 high-κ gate stack as a function of peak level voltage $V_{\rm peak}$ at various frequencies. The inset illustrates the definition of input pulse waveform parameters.

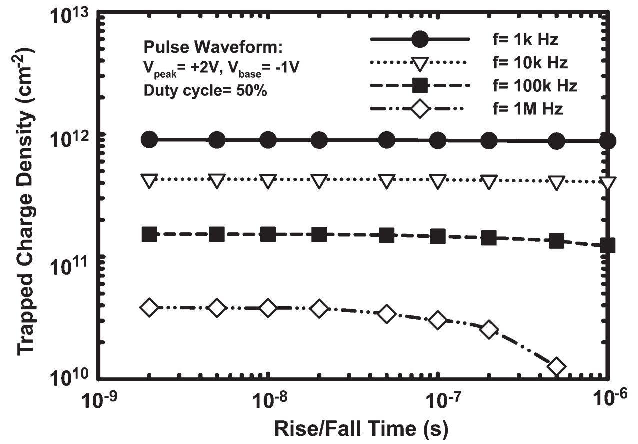

Fig. 4. Trapped charge density N_t as a function of the rise/fall time (T_r/T_f) of input pulse waveform at various frequencies (1 k, 10 k, 100 k, and 1 MHz). T_r/T_f is highly associated with the scanned energy range of interface states in the Si forbidden bandgap.

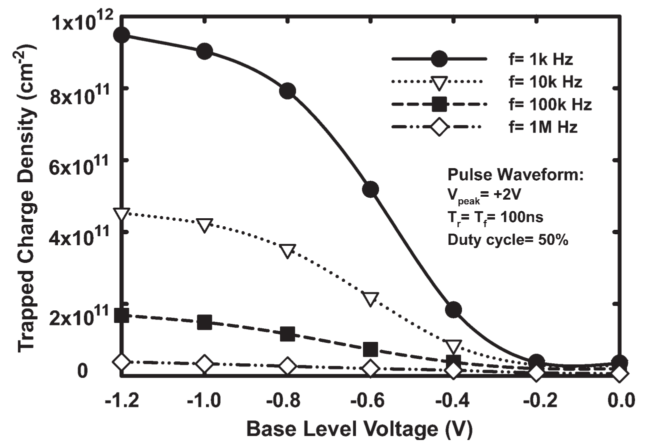

Fig. 5. Trapped charge density N_t as a function of the base level voltage $V_{\rm base}$ of input pulse waveform at various frequencies (1 k, 10 k, 100 k, and 1 MHz). The negative bias voltage of $V_{\rm base}$ plays a significant role to pull out the trapped charge carriers in the transient discharging stage.

where $I_{\rm cp}$ is the charge pumping current measured at the substrate, q is the fundamental electron charge, f is the frequency of input pulse waveform, and A_G is the gate area. As compared to the N_t measured at $f = 1$ MHz (which is believed to mainly stand for the interface state density $N_{\rm it}$), the additional N_t at lower frequencies are attributed to the contributions from the preexisting bulk traps in the HfO_2 high-κ dielectric since the amount of oxide traps should be negligible in the well-fabricated thermally grown interfacial oxide [8], [9]. Moreover, it was found that these border traps could not be detected anymore in the HfO_2/SiO_2 high-κ gate stack with the same HfO_2 high-κ dielectric ($\sim$3.2 nm) but thicker interfacial oxide ($\sim$1.6 nm), or in the HfSiON/SiO_2 high-κ gate stack with the optimized HfSiON high-κ dielectric ($\sim$3.5 nm) and the same interfacial oxide ($\sim$1.0 nm). It appears that the preexisting high-κ bulk traps located near the HfO_2/SiO_2 interface or called border traps could instantly exchange charge carriers with the underlying Si substrate if the interfacial oxide is thin enough for these charge carriers to tunnel through within the given pulse cycle. In addition, the N_t increased exponentially with the decreasing frequency and increasing peak level voltage, and these findings are consistent to those of tunneling into and from the near-interface oxide traps in heavily irradiated thermal oxides SiO_2 [15]–[18].

B. Transient Charging and Discharging Behaviors

Fig. 4 shows the trapped charge density N_t as a function of the rise/fall time (T_r/T_f) of input pulse waveform at various frequencies $(f = 1\ \text{k}, 10\ \text{k}, 100\ \text{k}, \text{and}\ 1\ \text{MHz})$. The N_t remained constant even with a great variety of T_r/T_f ranging from 2 ns to 1 μs except the one measured at $f = 1$ MHz. Since the T_r/T_f is highly associated with the scanned energy range of interface states in the Si forbidden bandgap [28] and the N_t at low frequencies are almost independent of T_r/T_f, the injected channel electrons from the Si conduction band states may directly tunnel into and out from the border traps in the HfO_2 high-κ dielectric within the durations of transient charging ($V_{\rm peak}$, ON state) and discharging ($V_{\rm base}$, OFF state) stages, respectively. This may also eliminate the possibility of two-step capture and emission process (in which an efficient thermal Shockley–Read–Hall capture into an interface trap is followed by a trap-to-trap tunneling transition and vice versa [29]). Fig. 5 shows the trapped charge density N_t as a function of the base level voltage $V_{\rm base}$ of input pulse waveform at various frequencies. When the negative $V_{\rm base}$ increased, the N_t at low frequencies grew gradually and eventually became saturated. Also note that the N_t at various frequencies are almost identical at $V_{\rm base} = 0 \sim -0.2$ V. It suggests that the negative bias voltage of $V_{\rm base}$ plays a significant role to pull out the trapped electrons from the border traps in the transient discharging stage. Fig. 6 shows the trapped charge density N_t as a function of the duty cycle of input pulse waveform at various frequencies. Similar to the capture and emission of the interface states, the transient charging and discharging of border traps should both occur within one pulse cycle to constitute the recombination charge pumping current. With very small ($\sim$0%) or very large ($\sim$100%) duty cycles, the charge carriers may not have enough time to tunnel into or out from the border traps in the HfO_2 high-κ dielectric, and only the interface states that can exchange charge carriers in a very short time could be observed

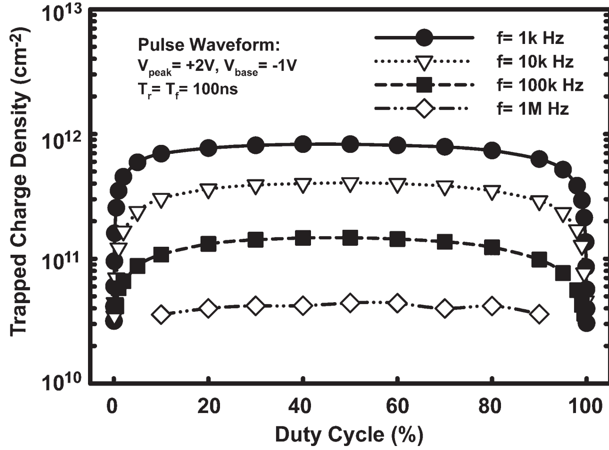

Fig. 6. Trapped charge density N_t as a function of the duty cycle of input pulse waveform at various frequencies (1 k, 10 k, 100 k, and 1 MHz). Symmetric transient charging and discharging behaviors could be observed at very small and very large duty cycles.

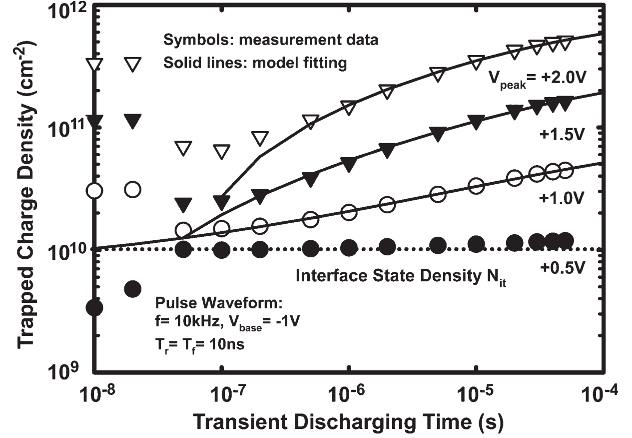

Fig. 8. Trapped charge density N_t as a function of transient discharging time at various peak level voltages V_{peak} by changing the off time of input pulse waveform at $f = 10$ kHz. Symbols are measurement data, dotted line is the interface state density, and solid lines are the model fitting results.

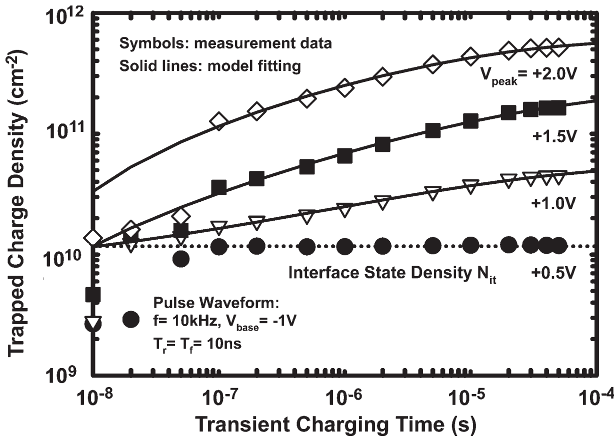

Fig. 7. Trapped charge density N_t as a function of transient charging time at various peak level voltages V_{peak} by changing the on time of input pulse waveform at $f = 10$ kHz. Symbols are measurement data, dotted line is the interface state density, and solid lines are the model fitting results.

as the one measured at $f = 1$ MHz. In addition, symmetric transient charging and discharging behaviors could also be clearly observed at very small and very large duty cycles, therefore suggesting equal forward and reverse tunneling time constants.

Fig. 7 shows the trapped charge density N_t as a function of transient charging time at various peak level voltages V_{peak} by changing the on time within one pulse cycle at $f = 10$ kHz. The N_t began to increase rapidly at the transient charging time $\sim 10^{-7}$ s in a power law relation and eventually became saturated except the one with $V_{\mathrm{peak}} = +0.5$ V where only the interface states were observed, thus implying that the transient charging effect may occur within 50–100 ns. Symbols are measurement data, dotted line is the interface state density, and solid lines are the model fitting results using the charge trapping model with dispersive capture time constants [30], [31]

$$N_t(t) = N_{\mathrm{bt}}(t) + N_{\mathrm{it}} = N_{\mathrm{bt},0}\left[1 - \exp\left(-(t/\tau)^{\beta}\right)\right] + N_{\mathrm{it}} \quad (2)$$

where t is the transient charging time, $N_{\mathrm{bt}}(t)$ is the detected border trap area density (cm^{-2}) as a function of transient charging time, N_{it} is the interface state density, $N_{\mathrm{bt},0}$ is the preexisting border trap area density in the HfO_2 high-κ dielectric, τ is the capture time constant, and β is the distribution factor of capture time constant ($\beta = 1$ for SiO_2). Although the $N_{\mathrm{bt},0}$ and τ vary, the β is $\sim$0.32 for various V_{peak}, and this also confirms that the border traps in the HfO_2/SiO_2 high-κ gate stack should be spatially located at the bulk layer of HfO_2 high-κ dielectric, not at the SiO_2 interfacial oxide. Fig. 8 shows the trapped charge density N_t as a function of transient discharging time at various peak level voltages V_{peak} by changing the off time within one pulse cycle at $f = 10$ kHz. Similar to the transient charging behavior, transient discharging behavior could also be well described by the same charge detrapping model with dispersive emission time constants. The $N_{\mathrm{bt},0}$ and τ of transient discharging behavior are near to those of transient charging behavior, and the β is also $\sim$0.32. Basically, the distribution factor β is a measure of the distribution width of capture/emission time constants, and these widely distributed capture/emission time constants could be attributed to the different tunneling distance from the Si substrate surface to those localized border traps in the high-κ bulk layer. This could be further explained by considering the exponential relationship between the tunneling time constant and tunneling distance in typical direct tunneling model. In addition, the previous studies about slow high-κ traps by using positive bias temperature instability stress and static I_d–V_g characteristics [31] also exhibited the same β ($\sim$0.32) value. Therefore, we could conclude that the slow and fast high-κ traps in the HfO_2 bulk layer may have similar spatial trap distribution and that the slow high-κ traps might be identical to the fast high-κ traps in properties but just located deeper inside. In other words, the slow and fast high-κ traps may only differ from the electrical response time, presumably due to their different spatial locations from the Si substrate surface.

C. Spatial and Energetic Distribution of Border Traps

Fig. 9 shows the detected border trap area density N_{bt} as a function of the frequency of input pulse waveform at various

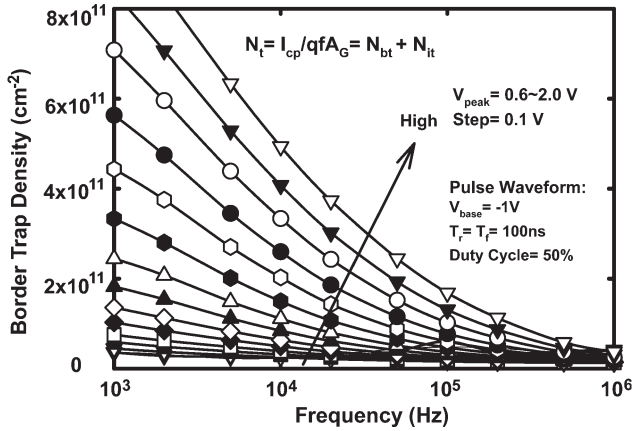

Fig. 9. Border trap area density $N_{\rm bt}$ of the dual-layer HfO_2/SiO_2 high-κ gate stack as a function of the frequency of input pulse waveform at various peak level voltages $V_{\rm peak}$. As can be seen, $N_{\rm bt}$ increased exponentially with the decreasing frequency and increasing peak level voltage.

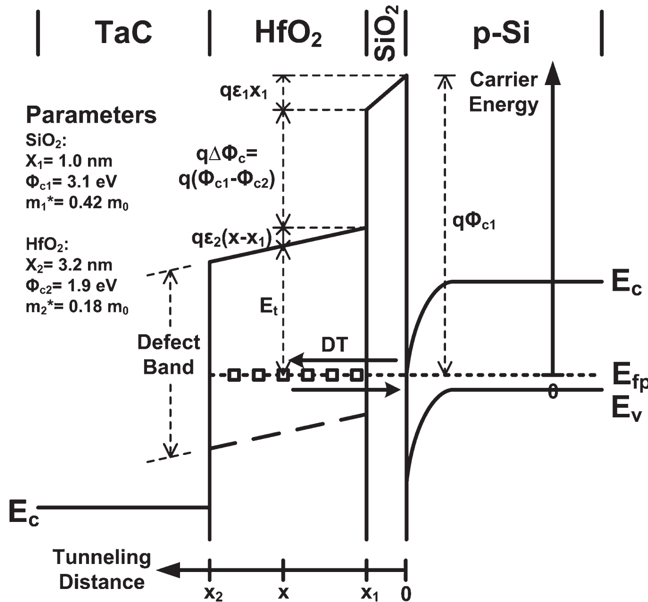

Fig. 10. Schematic band diagram of the dual-layer HfO_2/SiO_2 high-κ gate stack biased in the strong inversion region with the illustrations of tunneling distance and carrier energy coordinates. The model parameters are also given in the inset.

peak level voltages $V_{\rm peak}$ by transforming the frequency and voltage dependencies in Fig. 3. These frequency and voltage dependencies of $N_{\rm bt}$ could also be transformed into the relations of tunneling distance from the Si substrate surface and trap energy depth from the HfO_2 conduction band edge, respectively. Fig. 10 shows the schematic band diagram of the $TaC/HfO_2/SiO_2$/p-Si NMOS device biased in the strong inversion region with the illustrations of tunneling distance and carrier energy coordinates. If the transient charging and discharging of border traps mainly occur at the Si conduction band edge through direct tunneling and these border traps are widely distributed over a defect band in the HfO_2 high-κ dielectric [8], the $N_{\rm bt}$ could be regarded as the equivalent border trap area density $D_{\rm bt}$ at one specific energy level $(\mathrm{cm}^{-2}\cdot\mathrm{eV}^{-1})$, which is the integration of border trap volume density $\rho_{\rm bt}$ $(\mathrm{cm}^{-3}\cdot\mathrm{eV}^{-1})$ from the base oxide thickness x_1 to the maximum tunneling distance $x_{\max}$ in the HfO_2 high-κ dielectric since there should be negligible border traps in the thermally grown interfacial oxide SiO_2

$$N_{\rm bt} \sim D_{\rm bt} = \int_{x_1}^{x_{\max}} \rho_{\rm bt}(x, E_t)dx. \tag{3}$$

The trap energy depth E_t from the HfO_2 conduction band edge could be approximately obtained at various peak level voltages if the two-band structure (SiO_2 and HfO_2) with trapezoidal potential barriers has been considered

$$E_t(x,\varepsilon) = q\phi_{c2} - q\varepsilon_1 x_1 - q\varepsilon_2(x - x_1) \tag{4}$$

where ϕ_{c2} (1.9 eV) is the conduction band offset of HfO_2 [32], ε_1 and ε_2 are the electric fields in the SiO_2 and HfO_2 dielectrics, and x_1 is the base oxide thickness (1.0 nm). If the tunneling transition is an elastic direct tunneling process with symmetric forward and reverse tunneling time constants, the tunneling time constants between the available Si conduction band states and localized border traps should be equal to or less than $1/2f$ if the duty cycle is 50%

$$\frac{1}{2f} = \tau_0 \exp\left(2\int_0^{x_1} \frac{\sqrt{2m_1^*(q\phi_{c1} - q\varepsilon_1 x')}}{\hbar}dx' + 2\int_{x_1}^{x} \frac{\sqrt{2m_2^* E_t(x',\varepsilon)}}{\hbar}dx'\right) \tag{5}$$

where f is the frequency, τ_0 is the preexponential factor ($\sim 10^{-10}$ s) that is relatively insensitive to the tunneling distance and trap energy depth [33], $\hbar$ is the reduced Planck constant, ϕ_{c1} (3.1 eV) is the conduction band offset of SiO_2, and m_1^* (0.42 m_0) and m_2^* (0.18 m_0) are the effective mass of electrons in the SiO_2 and HfO_2 dielectrics [12], [32]. Then, the maximum tunneling distance $x_{\max}$ that can be reached during the given pulse cycle could be extracted from (5) with the above physical model parameters. As concerning about the spatial location of border traps, there is a controversy over the effective probing depth into the high-κ/oxide gate stack. Some researchers claim that the low-frequency charge pumping method is capable of probing into the high-κ dielectric [8], [9], [20]–[23], but others claim that this method could only probe within the interfacial oxide [24], [25]. This debate has been discussed in detail from the viewpoint of the preexponential factor τ_0, and reasonable comments have been made on the tunneling mechanism and effective probing depth [34]. Finally, the spatial and energetic distribution of the border trap volume density $\rho_{\rm bt}$ could be obtained as follows:

$$\rho_{\rm bt}(x, E_t) = \frac{-2\sqrt{2m_2^* E_t(x,\varepsilon)}}{\hbar}\frac{dN_{\rm bt}}{d\ln(f)}. \tag{6}$$

Fig. 11 shows the spatial and energetic distribution of the border trap volume density $\rho_{\rm bt}$ ($\sim 10^{17}$–10^{19} $\mathrm{cm}^{-3}\cdot\mathrm{eV}^{-1}$) in the dual-layer HfO_2/SiO_2 high-κ gate stack. Symbols are model-extracted data points, and 3-D mesh is the smoothed surface

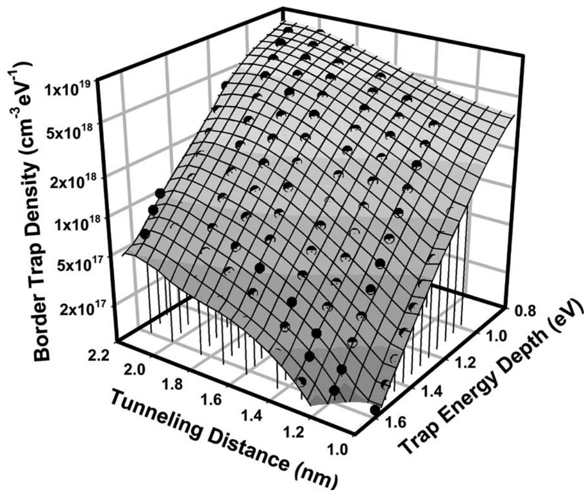

Fig. 11. Spatial and energetic distribution of border trap volume density $\rho_{\rm bt}$ in the dual-layer HfO_2/SiO_2 high-κ gate stack. Symbols are model-extracted data points, and 3-D mesh is the smoothed surface profiling of these points.

profiling of these points. The border trap volume density here should be regarded as the effective trapped charge density in the border traps since the dynamics of charge trapping and detrapping might be significant to the filling factor of these border traps. As the tunneling distance reached the HfO_2 high-κ dielectric $(x > 1.0$ nm), the $\rho_{\rm bt}$ began to increase gradually and eventually became saturated. Moreover, the $\rho_{\rm bt}$ increased exponentially with the decreasing trap energy depth E_t, and the variation of the $\rho_{\rm bt}$ seems to be less sensitive to the tunneling distance. These results suggest that most of the preexisting high-κ border traps are located in the HfO_2 bulk layer and that considerable parts of these border traps are positioned at the shallow energy levels.

IV. Conclusion

Low-frequency charge pumping method has been demonstrated as a powerful tool to measure the preexisting high-κ traps located near the HfO_2/SiO_2 interface or called border traps, which can instantly exchange charge carriers with the underlying Si substrate through direct tunneling. By varying the frequency, rise/fall time, peak and base level voltages, and duty cycle of input pulse waveforms, we will have a deep insight into the transient charging and discharging characteristics in high-κ/oxide gate stacks. These findings include the following points: 1) Transient charging and discharging stages occur during the on and off times within one pulse cycle (not at the transition times), respectively; 2) transient charging and discharging of border traps must both occur to constitute the charge pumping current; 3) symmetric transient charging and discharging behaviors imply the elastic direct tunneling between the localized border traps and available conduction band states; and 4) the same β value ($\sim$0.32) suggests similar spatial distribution of slow and fast high-κ traps. In addition, the transient charging and discharging behaviors of border traps could be analyzed as a function of time in the time scale of 10^{-8}–10^{-4} s, and this method is much faster than the known pulse I_d–V_g technique ($\sim$1–10 μs). Finally, based on an elastic direct tunneling model with trapezoidal potential barriers, the spatial and energetic distribution of the effective trapped charge density in the border traps could be profiled as a smoothed 3-D mesh.

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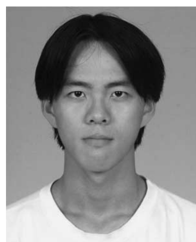

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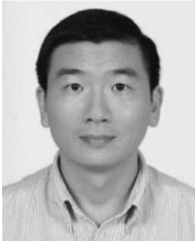

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