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Dynamic NBTI characteristics of PMOSFETs with PE-SiN capping

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Abstract

Negative-bias-temperature instability (NBTI) characteristics of strained p-channel metal–oxide–semiconductor field-effect transistors (PMOSFETs) under dynamic and AC stressing were investigated in this work. The compressive strain in the channel was deliberately induced by a plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN) capping layer in this study. It was found that the capping would degrade the NBTI characteristics, although the degradation is relieved when the stress frequency increases. The aggravated NBTI behaviors are ascribed to the higher amount of hydrogen incorporation during SiN deposition.

1. Introduction

Recently, mobility enhancement by channel strain engineering has emerged as an effective approach to improve the performance of scaled devices [1–5]. A method to introduce compressive strain to the channel of PMOSFETs is by use of a SiN capping layer deposited by plasma-enhanced CVD (PECVD) [1,2]. Though strained channel could enhance the mobility and thus the drive current of the device, potentially it could also compromise the device's reliability characteristics. From our previous study [6], hydrogen species unintentionally incorporated in the thin stress booster film may also adversely affect the device reliability characteristics. The device reliability issue is therefore a potential issue when the local strain is introduced and should therefore be carefully addressed.

Negative-bias-temperature instability (NBTI) is well known as one of the lifetime-limiting reliability concerns in CMOS devices when the gate oxide thickness is scaled to 3.5 nm and below [7]. Conventionally, characterization of NBTI is primarily based on static experimental data. However, for real-life operations of digital circuits, the applied bias to the gate of PMOSFETs in a CMOS inverter is being switched between "high" and "low" voltages incessantly. The dynamic NBTI (DNBTI) effect thus could greatly prolong the lifetime of PMOSFETs operating in a practical digital circuit [8]. A physical model has been previously proposed for DNBTI involving the interaction of the released hydrogen re-passivating Si dangling bonds during the passivation time [9]. However, reports on DNBTI of devices with SiN capping are lacking. In this work we investigate the issue by performing dynamic and AC stress measurements on PMOSFETs with a compressively strained channel.

2. Experimental

The test devices characterized in this study were fabricated on 6-in. n-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Gate oxide of 3 nm was grown in a vertical furnace in O_2 at 800 °C. After gate oxide growth, a 150 nm poly-SiGe layer was deposited by LPCVD, followed by standard plasma gate-etch process to form the patterned gate. Afterwards, the standard procedures of forming TEOS spacer and S/D junctions, a SiN layer of 100 nm and a TEOS passivation layers were deposited in turn by a PECVD system. Fig. 1 shows the cross-sectional view of the PMOSFETs with and without PE-SiN capping

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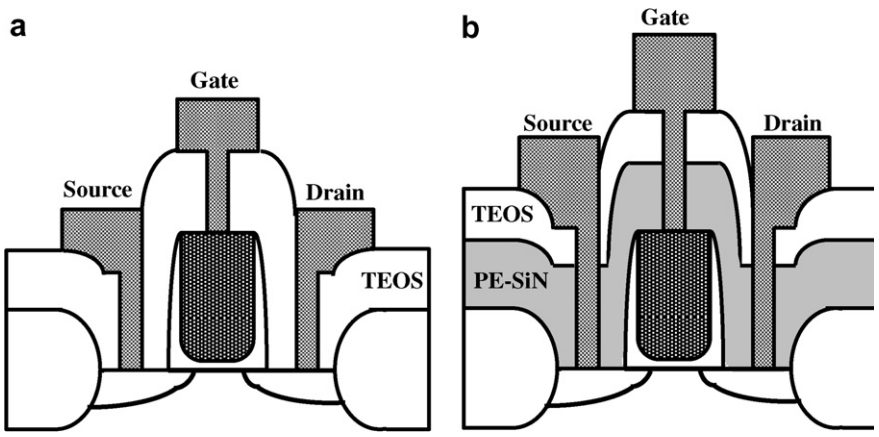

Fig. 1. Cross-sectional view of the PMOSFETs (a) without and (b) with PE-SiN capping layer.

layer. The stress induced by the PE-SiN layer was examined by probing the blanket films deposited on Si monitor wafers and the stress was measured to be around −95 MPa for 100 nm-thick SiN. Contact holes and metallization processes were subsequently performed. Finally, the processing was completed with a forming gas anneal at 400 °C. Electrical characterizations were measured using an HP4156 system. The stress measurements were performed using a temperature-regulated hot chuck at 125 °C. Setups of measurements are showed in Fig. 2. For dynamic stress measurements (Fig. 2(a)), alternating "stress" and "passivation" modes both with a period of 2000 s were performed on the devices. The source, drain and substrate electrodes were all connected to ground during the measurement, while the gate bias was applied with −4 V and 0 V (or 1 V) in stress and passivation periods, respectively. We have also performed the measurements with applied frequencies ranging from 1 kHz to 1 MHz and the amplitude of AC signal was $|V_{th}| + 4$ V (i.e., from $V_G - V_{th} = -4$ V to $V_G = 0$ V). Interface traps were evaluated using charge pumping method with a fixed amplitude of 1.5 V at 1 MHz. It was found that the measured I_{CP} current showed essentially linear dependence on the frequency. Based on the results we conclude that interface states are mainly responsible for the CP current.

It was widely suspected that hydrogen species presenting at the oxide/Si interface are one of the culprits in aggravating NBTI [10,11]. For example, breaking of H-terminated bonds leads to the generation of interface states. Excessive hydrogen may come from the deposited thin films, such as SiN. In this aspect, it is well known that the PE-SiN film contains a substantial amount of hydrogen [12]. The anomalously high hydrogen species incorporated in the film is a result of using SiH_4 and NH_3 as precursors during deposition. Deposition temperature is also important As has been pointed out in [12], due to the increase in dissociation rate of hydrogen from the precursor species when the temperature increases, SiN layer deposited by the PECVD operated at 200–400 °C has higher hydrogen contents than that by low-pressure (LP) CVD operated at 700–900 °C. In Fig. 3 we compare the characterization results of Fourier transform infrared (FTIR) spectrometer performed on SiN films prepared by PECVD and LPCVD. As can be seen in the figure, extra signal of S–H bonds are indeed detected in the PE-SiN and the result is consistent with [12].

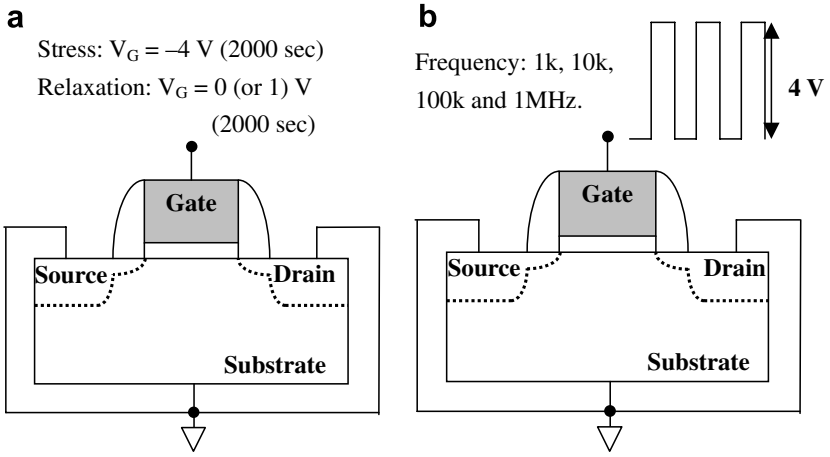

Fig. 2. Measurement setup for (a) dynamic NBTI and (b) AC NBTI stress.

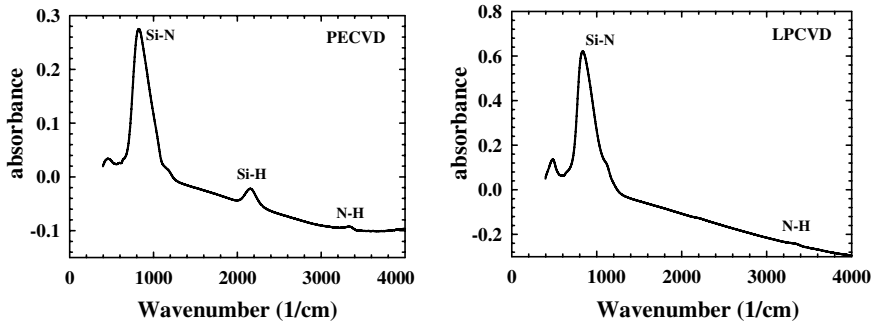

Fig. 3. Bonding signals of LP- and PE-SiN layers detected by Fourier transform infrared sepectrometer (FTIR). PE-SiN layer depicts an extra signal of Si–H bond.

3. Dynamic NBTI characteristics

It was shown in our previous work that the deposited PE-SiN film tends to increase the drive current and the improvement becomes more significant as the devices become shorter. This is a reasonable trend since the uniaxial strain level increases with decreasing channel length. Specifically, 29% improvement in drive current could be reached at a channel length of 0.45 μm [6].

Fig. 4(a) and (b) depicts DNBTI results in devices with and without SiN capping, respectively. The control (e.g., without SiN capping) samples show reasonable trends as those reported in previous works [13]. Under the same stress conditions, the devices with SiN capping layer exhibit larger ΔV_{th} and ΔN_{it}. It is also noted that ΔN_{it} shows obvious saturation behavior in the case of the strained devices, as shown in Fig. 4(b), and even in the second and third stress periods the peak values remain almost unchanged. Such behavior is not presented in the control samples (shown in Fig. 4(a)).

Despite the saturation of ΔN_{it}, ΔV_{th} continues to reach higher peaks during subsequent stressing periods, as shown in Fig. 4(b) indicating the existence of an unaccounted contributor to the NBTI degradation and recovery processes. In addition, we can also see that the amount of V_{th} recovery is higher for passivation voltage (V_P) of 1 V. This observation holds true for devices with or without SiN capping. This observation strongly suggests that the neutralization of trapped holes in the oxide [13], in addition to the re-passivation of interface states, occurs in the recovery period for the devices. Although ΔN_{it} of the strained devices is independent of V_P, as shown in Fig. 4(b), the recovery in ΔN_{it} still represents the most significant contributor to the V_{th} recovery, even at V_P of 1 V. The results suggest that neutral hydrogen species plays a major role in the re-passivation of interface states and the recovery processes [14].

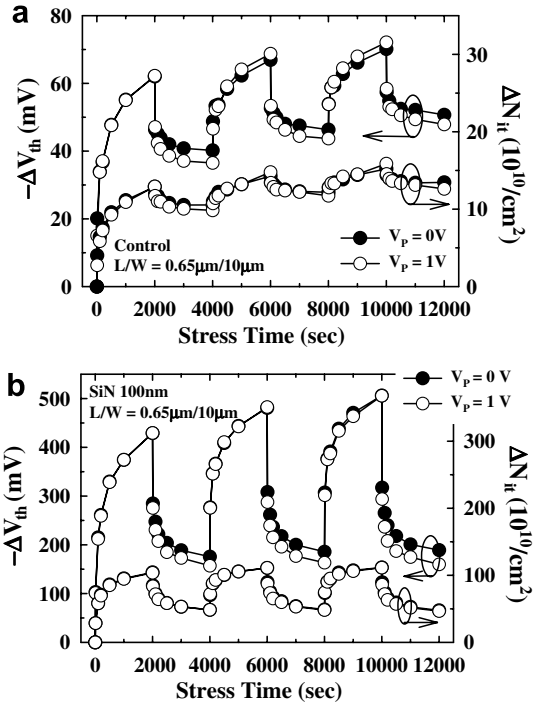

Fig. 4. DNBTI characteristics of devices (a) without and (b) with SiN capping layers. Stress and passivation voltages are $V_G - V_{th} = -4$ V and $V_G = 0$ V (or 1 V) at 125 °C, respectively.

4. Effect of stress frequency

Next we investigated the effect of AC stress frequency on these devices. Fig. 5 shows ΔV_{th} in devices, both with and

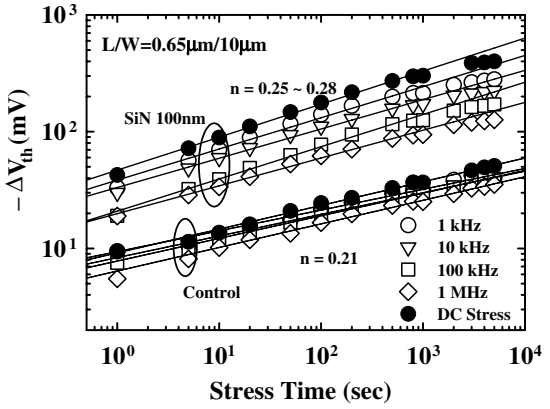

Fig. 5. Threshold voltage shift for devices with and without SiN capping, measured at four different AC stress frequencies at 125 °C.

without SiN capping, stressed at four different frequencies, all with 50% duty cycle. The splits subjected to the static DC stress are also shown as the reference. From Fig. 5, it is clearly seen that the interface state creation shows only weak frequency dependence for the control devices. In reference to the analysis made in previous reports [13,15], the observation is reasonable. In contrast, both ΔV_{th} and ΔN_{it} of the strained devices depict strong frequency dependence. This is further evidenced in Fig. 6, in which the shifts in ΔV_{th} and ΔN_{it} after 500 s stress are plotted as a function of stress frequency. It can be seen that both ΔV_{th} and ΔN_{it} are strongly dependent on the stress frequency for the strained devices. Specifically, ΔV_{th} decreases from 214 mV to 94.2 mV when the stress frequency increases from 1 kHz to 1 MHz. These observations are explained as follow: the excess hydrogen species coming from the SiN capping layer would diffuse to the oxide/Si interface during device fabrication. Breaking of the excess hydrogen-related bonds during stressing would contribute to the generation of interface states and leads to a higher exponent value (designated as "n" in Fig. 5). Nevertheless, the bond breaking process needs sufficient stress time to trigger, resulting in the significant frequency dependence.

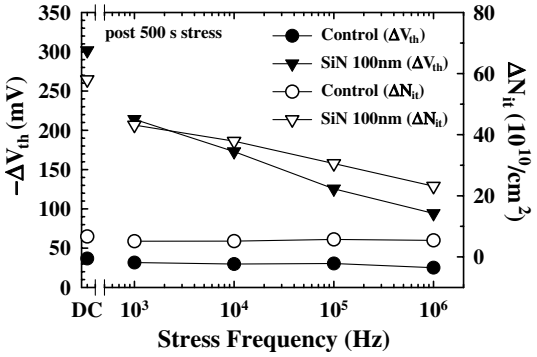

Fig. 6. ΔV_{th} and ΔN_{it} versus stress frequency. In the device with SiN capping, ΔV_{th} and ΔN_{it} are strongly dependent on frequency. As frequency increases, ΔV_{th} and ΔN_{it} significantly decrease.

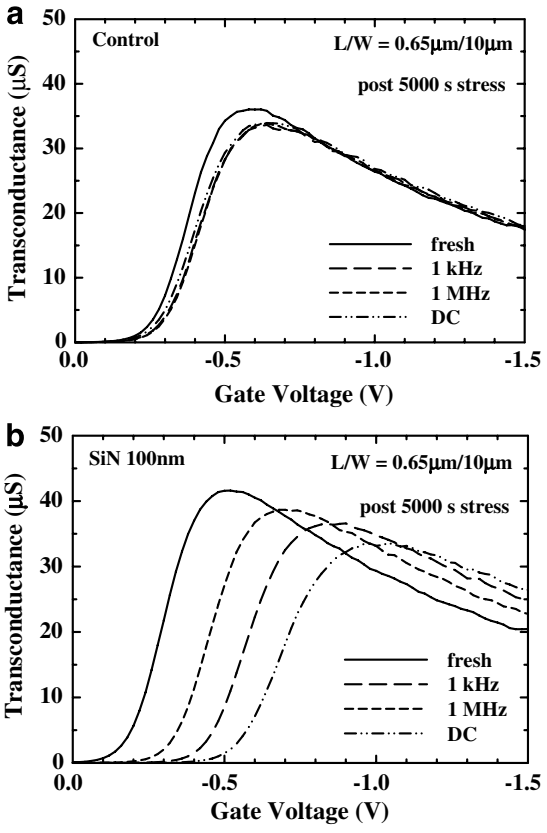

Fig. 7. Transconductance in devices with and without SiN-capping, as-fabricated and after 5000 s DC and AC stress (1 kHz and 1 MHz), both measured at $V_G - V_{th} = -4$ V and 125 °C NBT stress. (a) Control devices and (b) SiN capping devices.

Fig. 7 compares the transconductance (GM) of fresh devices with those subjected to 5000 s of DC or AC stress. It is obvious that the differences among the DC and AC stress samples are marginal in the control devices. On the other hand, despite the significant enhancement in GM in fresh devices with SiN capping, the degradation under DC stress is grossly aggravated. In other words, the benefit of using channel strain is negated under DC NBT stress. Nevertheless, such restriction is greatly relieved under AC stress, especially when the frequency is high.

5. Effect of channel length

Fig. 8 shows ΔV_{th} of the stressed samples versus channel length after 500 s DC stress or AC stress (1 MHz). In the figure, it is clearly seen that the use of PE-SiN capping may result in aggravated NBTI, although the device degradation could be largely reduced at high stress frequency. Moreover, it is seen that the ΔV_{th} increases with decreasing channel length in the SiN-capping devices. This again implies that diffusion of the excessive hydrogen from the PE-SiN is mainly responsible for the aggravated NBTI characteristics.

The charge pumping current of the fresh device with SiN capping is slightly smaller than that of the control sample, as shown in Fig. 9. This is ascribed to the fact that hydrogen can effectively passivate the dangling bonds at the

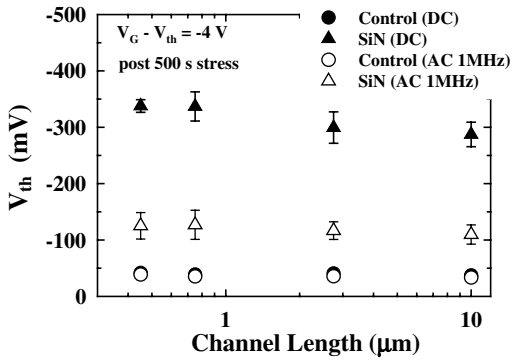

Fig. 8. ΔV_{th} versus channel length after 500 s NBTI stress. For a given channel length, devices with PE-SiN capping show larger ΔV_{th}.

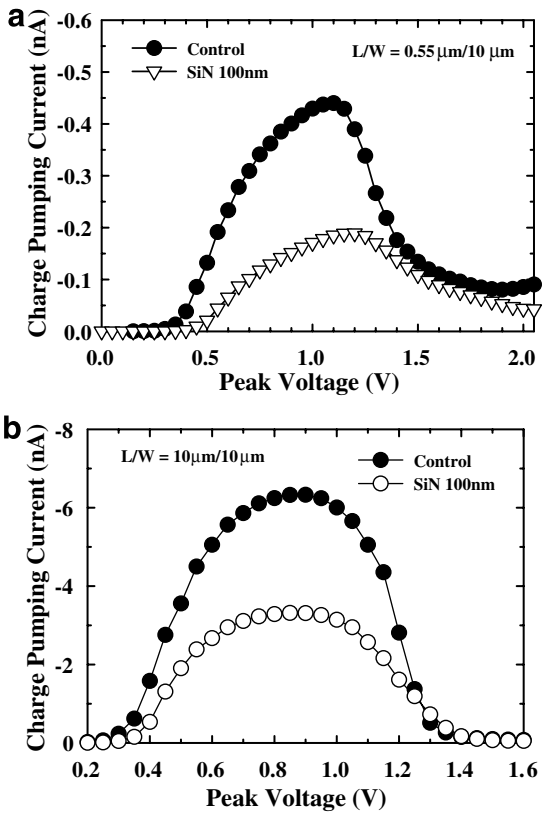

Fig. 9. Charge pumping current of fresh devices with and without PE-SiN capping. (a) $L = 0.55$ μm and (b) $L = 10$ μm.

SiO_2/Si interface, and leads to a lower interface state density for the as-fabricated devices with SiN-capping, irrespective of the channel length scaling. Nevertheless, the extra hydrogen species also act as the reaction precursors for the aggravated NBTI observed in devices with SiN-capping. This is consistent with the higher exponent value for devices with PE-SiN capping in the above discussion. Moreover, higher SiN strain energy stored in the channel may also play a role in the aggravated degradation process, which may weak Si–N, Si–O and Si–Si bonds near the SiO_2/Si interface, though more efforts are required to fully understand details about the process.

The above results clearly indicate that the NBTI is aggravated for devices with SiN-capping. Although the capping of a SiN layer can enhance drive current in the fresh device, aggravated NBT stress degrades the after-stress device performance and almost negates the benefit gained by SiN capping layer. Based on the above-mentioned fact that the deposited PE-SiN layer contains a large amount of hydrogen species, so the Si–H bonding is easier to break in the strained devices, and the voluminous hydrogen species aggravate NBTI. Hydrogen is believed to be the main passivating species for Si dangling bonds and plays a major role during NBTI stress, where Si–H bonds are depassivated, forming interface traps. It is therefore important to optimize the amount of hydrogen species while retaining its compressive stress during the deposition of SiN layer. This could be accomplished by carefully adjusting the process conditions (e.g., $SiH_4/N_2/NH_3$ gas flow rate, pressure, RF power) in PECVD systems [2], or resorting to high-density plasma CVD (HDPCVD) systems [12]. The latter approach has been shown to dramatically reduce the hydrogen content incorporated in the deposited films. This is essential to preserve the drive current enhancement while keeping the NBTI reliability characteristics at bay.

6. Conclusions

In this study, PMOSFETs with uniaxial strain in the channel induced by a compressive SiN-capping layer were fabricated and evaluated its NBTI characteristics. As a result, we can see that the SiN capping may aggravate the NBTI characteristics. The large amount of hydrogen species contained in the PE-SiN layer is the main culprit responsible for the worsened reliability. Hydrogen species is believed to play a major role during NBTI stress. Care should therefore be exercised to optimize the amount of hydrogen species to ensure that the NBTI effect is kept at bay, while simultaneously maintaining the performance enhancement characteristic of the compressive strain channel. In addition, recovery of the generated interface states in the strained device is not sensitive to the passivation voltage during stressing, indicating that neutral hydrogen species are mainly responsible for the phenomena. A strong dependence on the AC stress frequency is observed for the SiN-capped devices. Our observation reveals an important message that the aggravated NBTI in the strained devices could be largely alleviated by high frequency operation.

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References

[1] Ootsuka F, Wakahara S, Ichinose K, Honzawa A, Wada S, Sato H, et al. A highly dense, high-performance 130 nm node CMOS technology for large scale system-on-a-chip applications. In: Digest of the 2000 international electron devices meeting, 2000. p. 575–8.
[2] Ito S, Namba H, Yamaguchi K, Hirata T, Ando K, Koyama S, et al. Mechanical stress effect of etch-stop nitride and its impact on deep submicron transistor design. In: Digest of the 2000 international electron devices meeting, 2000. p. 247–50.
[3] Ghani T, Armstrong M, Auth C, Bost M, Charvat P, Glass G, et al. A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors. In: Digest of the 2003 international electron devices meeting, 2003. p. 978–81.
[4] Chidambaram PR, Smith BA, Hall LH, Bu H, Chakravarthi S, Kim Y, et al. 35 drive current improvement from recessed-SiGe drain extensions on 37 nm gate length PMOS. In: Digest of the 2004 symposium on VLSI technology, 2004. p. 48–9.
[5] Mistry K, Armstrong M, Auth C, Cea S, Coan T, Ghani T, et al. Delaying forever: uniaxial strained silicon transistors in a 90 nm

CMOS technology. In: Digest of the 2004 symposium on VLSI technology, 2004. p. 50–1.
[6] Lu CY, Lin HC, Chang YF, Huang TY. Devices characteristics and aggravated negative bias temperature instability in PMOSFETs with uniaxial compressive strain. Jpn J Appl Phys 2006;45:3064–9.
[7] Thewes R, Brederlow R, Schlünder C, Wieczorek P, Hesener A, Ankele B, et al. Device reliability in analog CMOS applications. In: Digest of the 1999 international electron devices meeting, 1999. p. 81–4.
[8] Chen G., Chuah KY, Li MF, Chan DSH, Ang CH, Zheng JZ, et al. Dynamic NBTI of PMOS transistors and its impact on device lifetime. In: 2003 International reliability physics symposium proceedings, 2003. p. 196–202.
[9] Mitani Y. Influence of nitrogen in ultra-thin SiON on negative bias temperature instability under AC stress. In: Digest of the 2004 international electron devices meeting, 2004. p. 117–20.
[10] Stathis JH, Zafar S. The negative bias temperature instability in MOS devices: A review. Microelectron Reliab 2006;46:270–86.
[11] Ogawa S, Shimaya M, Shiono N. Interface trape generation at ultrathin SiO_2 (4–6 nm) interfaces during negative-bias temperature aging. J Appl Phys 1995;77:1137–48.
[12] Yota J, Hander J, Saleh AA. A comparative study on inductively-coupled plasma high-density plasma, plasma-enhanced, and low pressure chemical vapor deposition silicon nitride films. J Vac Sci Technol, A 2000;18:372–6.
[13] Huard V, Denais M. Hole trapping effect on methodology for DC and AC negative bias temperature instability measurements in PMOS transistors. In: 2004 International reliability physics symposium proceedings, 2004. p. 40–5.
[14] Chakravarthi S, Krishnan AT, Reddy V, Machala CF, Krishnan S. A comprehensive framework for predictive modeling of negative bias temperature instability. In: 2004 International reliability physics symposium proceedings, 2004. p. 273–82.
[15] Alam MA. A critical examination of the mechanics of dynamic NBTI for PMOSFETs. In: Digest of the 2003 international electron devices meeting, 2003. p. 345–8.