RF Power Performance of Asymmetric-LDD MOS Transistor for RF-CMOS SOC Design

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***Abstract*—This letter presents a new asymmetric-lightly-doped-drain (LDD) metal oxide semiconductor (MOS) transistor that is fully embedded in a CMOS logic without any process modification. The radio frequency (RF) power performance of both conventional and asymmetric MOS transistor is measured and compared. The output power can be improved by 38% at peak power-added efficiency (PAE). The PAE is also improved by 16% at 10-dBm output power and 2.4 GHz. These significant improvements of RF power performance by this new MOS transistor make the RF-CMOS system-on-chip design a step further.**

***Index Terms*—Lightly-doped-drain (LDD), metal oxide semiconductor field effect transistor (MOSFET), metal oxide semiconductor (MOS) transistor, radio frequency (RF) power transistor.**

I. Introduction

THE rapid technology evolution of Si metal oxide semiconductor field effect transistor (MOSFET) is beneficial for integrated circuit (IC) design with higher device speed and cost reduction. Besides the advantages on digital performance, the scaling of CMOS technology also has largely improved the radio frequency (RF) performance of MOS devices. The most significant improvement along with CMOS technology scaling is the larger RF gain, higher cut-off frequency (f_t), and maximum oscillation frequency (f_{max}) [1]–[10]. This has made CMOS device technology the prime choice for RF system-on-chip (SoC) application such as WCDMA, W-LAN, and ultra-wide band (UWB) wireless communication. However, the low drain breakdown voltage of CMOS transistors restricts the use of CMOS for power amplifiers. This limitation for high voltage operation significantly reduces the maximum output power and efficiency for CMOS devices. Therefore, the RF SoC design, which includes the RF power amplifier, is a long time historical challenge for using the baseline CMOS logic process. In the past, LDMOS transistors were introduced to overcome the low drain break-down voltage issue at the expense of complex process and lower operation speed [11]–[13]. However, this is opposite to the technology trend for wireless communication, where continuously increasing operation frequency is needed.

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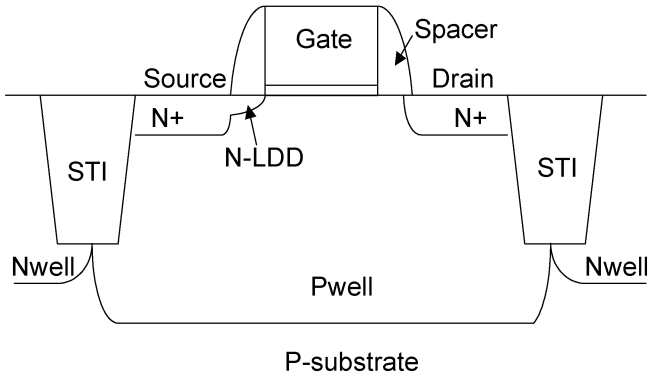

Fig. 1. Device structure of asymmetric-LDD MOS transistor. The major difference to conventional MOS transistor is no n^+-LDD region at drain side. The formed depletion region under reverse drain bias can sustain large voltage for RF power application.

To overcome the low breakdown voltage issue and improve the RF power performance, in this letter we report an asymmetric-lightly-doped-drain (LDD) MOS transistor for high frequency RF power application. This new asymmetric-LDD MOS transistor is fully embedded in the conventional foundry logic process without any additional process step or extra cost.

II. Experimental Procedure

The structure of the new asymmetric-LDD MOS transistor is shown schematically in Fig. 1. To increase the transistor breakdown voltage for RF power application, the LDD region at the drain size was removed, which is the major difference to a conventional MOS transistor. This was accomplished by blocking the ion implantations to LDD region and Halo process at the drain side for the new transistor. The devices we studied in this work are multiple fingers MOS transistors with 10 gate fingers, 0.23-μm gate length and 5 μm width. For comparison, the same interconnect and RF layout were used [6]–[10]. The devices were fabricated by a standard logic process provided by IC foundry. The RF power characterization was carried out by on-wafer measurements at 2.4 GHz using an ATN load-pull system, where the input and output impedance matching conditions were selected to optimize the output power.

III. Results and Discussion

A. Drain Breakdown Voltage

Fig. 2 shows the comparison of dc drain breakdown voltage for conventional and asymmetric-LDD MOS transistors. For the conventional MOS transistor, a $\mathrm{BV_{dss}}$ of 3.6 V was measured at I_{ds} of 0.1 $\mu\mathrm{A}/\mu\mathrm{m}$ and V_{gs} of 0 V. However, the maximum

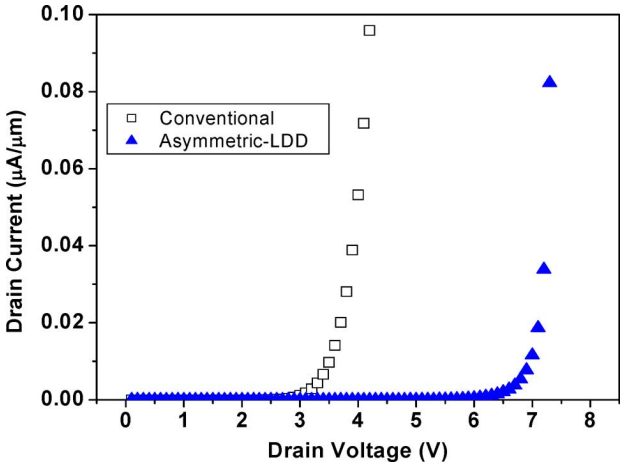

Fig. 2. Comparison of drain breakdown voltage ($\mathrm{BV_{dss}}$) at $V_{\mathrm{gs}} = 0$ V. The devices have a physical gate length of 0.23 μm. Significantly larger $\mathrm{BV_{dss}}$ is obtained using the new design.

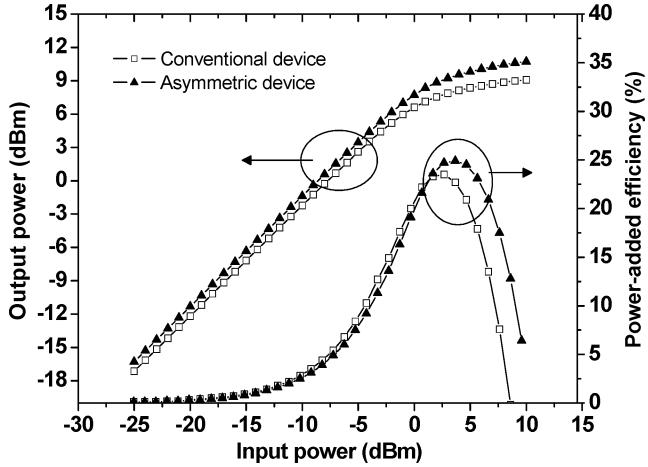

Fig. 3. Measured RF output power and PAE versus the input power for conventional and asymmetric-LDD MOS transistors at 2.4 GHz. The matching point is adjusted for the maximum power output point in the load pull system. Higher output power and broader PAE are measured for this new asymmetric-LDD MOS transistor.

drain bias is only 1.8 V if considering the reliability of 10 years continuous operation [6]. In sharp contrast, the $\mathrm{BV_{dss}}$ of the asymmetric-LDD transistor is increased to 7.0 V as measured under the same criteria. This large improvement of $\mathrm{BV_{dss}}$ is due to the designed wide depletion region beneath the spacer region and between the drain and substrate. In contrast, the existing n^+-LDD in a conventional CMOS transistor just provides an electrically short path between inversion channel and drain. Such wide depletion region in the new design can support significantly larger reverse-biased drain voltage than conventional case. This new device design with large drain depletion region is similar to bipolar transistor from the device physics point-of-view. Since the electrons can pass through the drain depletion region with fast saturation velocity under large reverse biased voltage, little degradation of operation speed can be expected. Therefore, this new asymmetric-LDD MOS transistor can effectively resolve the fundamental challenge of low breakdown voltage issue in the small energy bandgap Si MOS transistor. In the meanwhile this device still preserves the high frequency operation of sub-μm MOS transistors with cutoff frequency (f_t) of 34 GHz close to the 35 GHz of conventional MOS. This device also gives a higher maximum oscillation frequency (f_{max}) of 86 GHz than the 76 GHz of conventional MOS. It is generally known the increasing breakdown voltage may lower down the drive current. However, the new asymmetric MOSFET can be operated at a higher voltage that gives close drive current (10.44 mA at $V_{\mathrm{ds}} = 2.5$ V) to conventional device (9.76 mA at $V_{\mathrm{ds}} = 1.8$ V). One major reliability issue for conventional deep sub-μm MOSFET is the hot carrier injection (HCI) degradation [14], caused by impact ionization and electrons injection into the gate oxide by high drain field. From detailed transistor simulation T-Supreme Medici Analysis (TMA) [15], the asymmetric-LDD device design pushes the peak electric field away from the gate edge and reduces the electron injection into the gate oxide. Thus, good HCI reliability may be expected for this new device.

B. RF Power Performance

We have further measured the RF power performance in the asymmetric-LDD MOS transistor. The output power and PAE versus the input power of both the conventional and asymmetric-LDD MOS transistors are shown on Fig. 3. The dc bias point of the conventional MOS transistor is at V_{gs} of 1.2 V and V_{ds} of 1.8 V under the maximum trans-conductance condition. For the asymmetric-LDD MOS transistor, the dc bias point is at V_{gs} of 1.2 V and an increased V_{ds} of 2.5 V. Here only 2.5 V is chosen in this study although higher bias voltage can be used after detailed reliability study. The output power is increased by 38% from 130 to 180 mW/mm, as measured at 2.4 GHz under peak PAE condition. The PAE of asymmetric device at low input power is slightly lower than conventional device, which may be due to inferior electron transportation through the potential barrier at drain side. But this effect becomes less affective due to the electron tunneling via potential barrier at high electric field and bias voltage. In addition, broader maximum PAE region is also obtained in the asymmetric-LDD MOS transistor that provides wider design margin, in combination with the slightly increasing peak PAE from 23.5% to 24.9%. Moreover, when both devices are biased for 10 dBm output power measured at 2.4 GHz, the PAE can be improved by 16%. These achieved large improvements of power performance are a new breakthrough in RF Si CMOS transistors and important for wireless communication IC and SoC.

C. Linearity in Saturation

The carrier to third-order inter-modulation product output power (C/IM3) ratio is another important factor for RF power application. We have compared the C/IM3 for the two MOS transistors and the results are shown in Fig. 4. The asymmetric-LDD MOS transistor still shows a slightly improved C/IM3 ratio of 0.7 dB at peak PAE. The improvement is due to the reduced gate-drain coupling capacitance (C_{gd}) by removing the LDD implant under the spacer; this reduces the interference

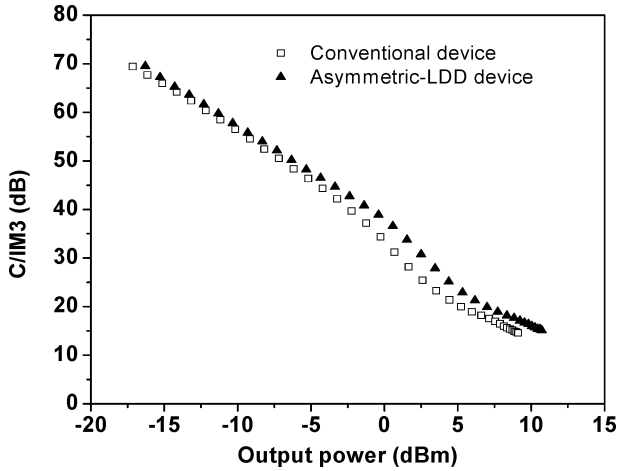

Fig. 4. Carrier to third-order inter-modulation product output power ratio (C/IM3) versus the output power for the two different devices measured at 2.4 GHz.

between gate and drain nodes and therefore improves the linearity. Therefore, significantly better output power density is achieved by the asymmetric-LDD MOS transistor with even slightly better linearity and PAE. However, the drain resistance $(R_{\rm gd})$ is also increased along with reduced $C_{\rm gd}$, which causes an increased threshold voltage.

IV. Conclusion

The low drain breakdown voltage of a conventional CMOS transistor is the major restriction of RF power performance. We have designed an asymmetric-LDD MOS transistor to increase the drain breakdown voltage from 3.6 to 7.0 V. By raising the drain operation voltage beyond conventional CMOS device, the RF output power of this new transistor is improved by as much as 38% at peak PAE, with the added merit of broader peak PAE region and useful for wider design margin. By removing LDD at the drain side but keeping the spacer, an $N^+ - P^-$ depletion region is formed at the drain side. The thickness of this capacitive depletion region is significantly larger than conventional symmetrical design, which allows larger voltage applied to drain. Thus, this drain engineering can improve the drain breakdown voltage and power performance. This new asymmetric-LDD MOS transistor is fully embedded in the standard CMOS logic process provided by foundries without any process modification.

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