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Operations of poly-Si nanowire thin-film transistors with a multiple-gated configuration

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Abstract
In this study, a novel multiple-gated (MG) thin-film transistor (TFT) with poly-Si nanowire (NW) channels is fabricated using a simple process flow. In the proposed new transistors, poly-Si NWs were formed in a self-aligned manner and were precisely positioned with respect to the source/drain, and the side-gate. Moreover, the NW channels are surrounded by three gates, i.e., top-gate, side-gate and bottom-gate, resulting in much stronger gate controllability over the NW channels, and greatly enhanced device performance over the conventional single-gated TFTs. Furthermore, the independently applied top-gate and/or bottom-gate biases could be utilized to adjust the threshold voltage of NW channels in a reliable manner, making the scheme suitable for practical applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Recently, silicon nanowires (NWs) have drawn considerable attention due to their potential applications to areas such as electronics, biology, and photonics. With their inherently high surface-to-volume ratio, Si NWs can provide high surface sensitivity suitable for the construction of sensor devices [1–3]. The severe short-channel effects (SCEs) encountered in conventional nanoscale field-effect transistors (FETs) could also be effectively suppressed [4, 5] due to the improved gate controllability with the NW channel. Moreover, owing to their small volume and the accompanying reduction in defects, the use of NWs as the channel in thin-film transistors (TFTs) has been demonstrated with superior performance [6, 7], in terms of higher carrier mobility and steeper subthreshold slope.

Concurrently, for the operation of silicon-on-insulator (SOI) metal–oxide–semiconductor field-effect transistors (MOSFETs), it has been experimentally and theoretically shown that double- and triple-gated configurations can substantially improve the device performance in terms of higher on-current (I_{ON}), steeper subthreshold slope (SS), as well as suppressed SCEs, owing to the stronger gate controllability over the channel [5, 8]. The combination of an ultrathin channel layer with multiple-gated (MG) structure further improves the device performance [9, 10]. MG NW devices therefore represent a potential and interesting device architecture for practical applications, although several issues relating to device preparation need to be resolved first. For example, the reported bottom-up approaches are usually plagued by concerns such as positioning, alignment, and precise structural parameter control of NWs [1, 3, 6]. On the other hand, advanced lithography tools and expensive materials are required for top-down approaches [4, 5, 11]. To address these issues, we have recently proposed a novel NW TFT fabrication method which features the precise positioning of NWs and good controllability over NW dimensions, while requiring only very simple processing without involving costly production tools or materials [7, 12]. In our previous works, single-gated operation was demonstrated. In this study, with a slight modification in device fabrication and mask design, a unique MG NW TFT is proposed and characterized.

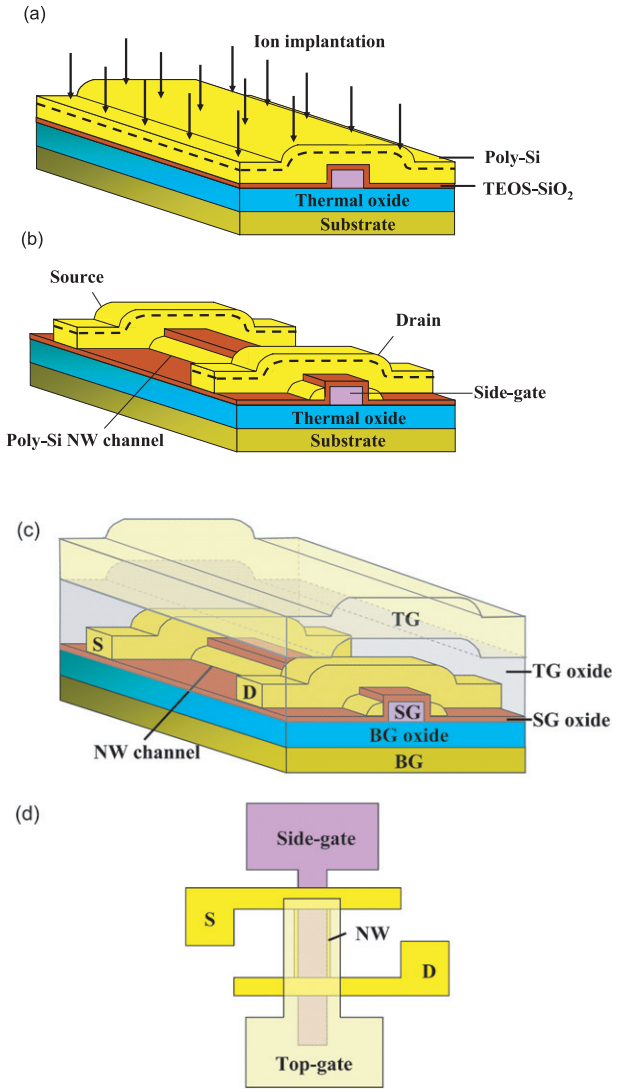

Figure 1. Key steps of NW TFT fabrication. (a) Source/drain ion implantation. The dashed line represents the projected range which is near the top surface due to the low implant energy used. (b) Formation of source, drain and NW channels. The NW channels remain undoped due to the low implant energy used. (c) Stereo view of the fabricated NW TFT. The top-gate, side-gate, and bottom-gate are formed in the structure. (d) Top view of the fabricated device.

2. Device structure and fabrication

Key fabrication steps of the new MG NW device are schematically illustrated in figure 1. First, an n± poly-Si layer was deposited and patterned as the side-gate (SG) on a Si substrate covered with a 100 nm thick thermally grown SiO_2 layer. A 40 nm tetraethyl orthosilicate oxide (TEOS-SiO_2) layer was then deposited by low-pressure chemical vapour deposition (LPCVD) to serve as the SG dielectric, followed by the deposition of 100 nm amorphous Si (a-Si) channel layer. Next, to transform the a-Si layer into polycrystalline state, a solid-phase crystallization (SPC) treatment was executed at 600 °C for 24 h in a furnace. Subsequently, source and drain (S/D) doping was performed by phosphorus ion implantation with a dose of 1×10^{15} cm^{-2} at 15 keV (figure 1(a)). Afterwards, NW channels and S/D regions were formed simultaneously by an anisotropic plasma (Cl_2/HBr) dry-etching step, and the resultant structure is shown in figure 1(b). Note that the low implant energy was chosen to ensure that the dopants were located near the top portion of the poly-Si layer, so the poly-Si NWs remained undoped. The dopant activation was performed at 900 °C for 30 s. A 200 nm thick TEOS was then deposited to serve both as the top-gate (TG) oxide and passivation layer. Afterwards, an Al–Si–Cu metal layer was deposited and patterned to form the TG electrodes as well as S/D and SG contact pads. It is worth noting that the NW channels formed by the unique sidewall spacer etching technique are literally surrounded by the three gates, as schematically shown in figure 1(c). The top view of the fabricated device is shown in figure 1(d). In addition to the SG and TG formed in the fabrication sequence mentioned above, the Si substrate itself serves as the bottom-gate (BG). The process flow and fabricated structure are similar to that described in our previous work [7, 12], except that a TG is added lying over the passivation oxide. It should be noted that for the devices characterized in this work, the oxide thickness between the gate and the NW is 100 nm for the BG, 40 nm for the SG, and 200 nm for the TG. In this configuration, the three gates could be biased either independently or jointly. To reduce the trap density and improve the interface quality, the devices also received a NH_3 plasma treatment at 300 °C for 2 h. It is particularly noteworthy that the overall fabrication process flow is very simple, and involves no costly lithography tools to form the NW structure.

Table 1. Active operating gates used in multiple-gated modes.

Mode	DG-1	DG-2	TriG
Operation gates	SG and TG	SG and BG	SG and TG and BG

Figure 2(a) is a scanning electron microscopy (SEM) photograph showing the top view of a device right after the step of NW and S/D definition (figure 1(b)). To clearly illustrate the structure, the oxide layer between the NWs and the side-gate is deliberately removed. The picture reveals the high fidelity of NW channel alignment with respect to the side-gate as well as the source/drain regions. The cross-sectional SEM image of a fabricated NW TFT with MG structure is shown in figure 2(b). This picture clearly shows that the NW channel is surrounded by the three gates (TG, BG and SG). Also shown in the figure is a close-up transmission electron microscopy (TEM) photograph exhibiting the triangle shape of the NW. The width and thickness of the NW structure defined in the picture are 30 and 40 nm, respectively. From these micrographic analyses, it can be clearly seen that the proposed approach provides a very simple method to form NW-channel devices with multiple gates.

3. Results and discussion

In our previous studies [7, 12], the bias was applied only to the SG for controlling the device switching. Here we examine the drain-current versus gate-voltage (I_D–V_G) characteristics of MG configurations in reference to that of the SG operation. Three MG operation modes specified in table 1 were investigated, including two double-gated modes

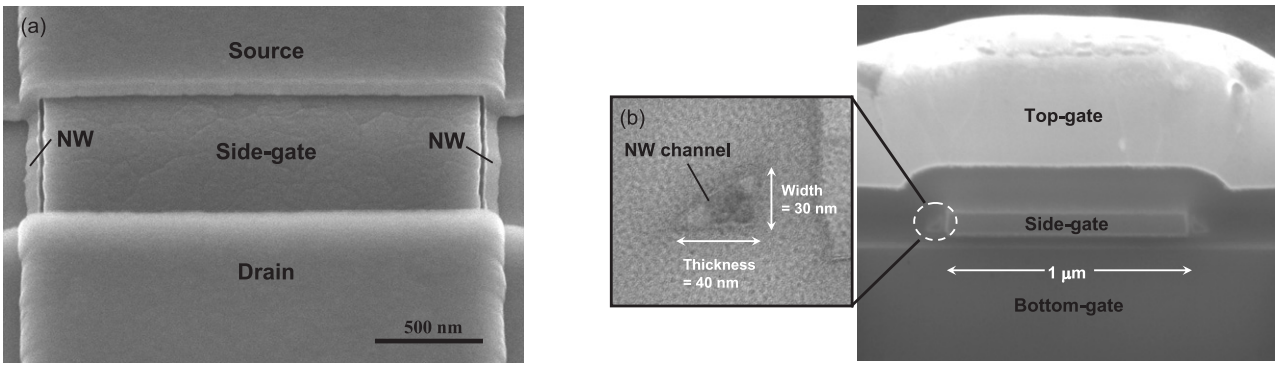

Figure 2. (a) SEM image of an NW TFT before the deposition of passivation oxide and top-gate electrode, showing the self-aligned NW channels. (b) (Right) Cross-sectional view SEM photograph of a fabricated MG TFT showing NW channels surrounded by top-, side- and bottom-gates. (Left) Close-up TEM image of a NW channel specifying the width and thickness.

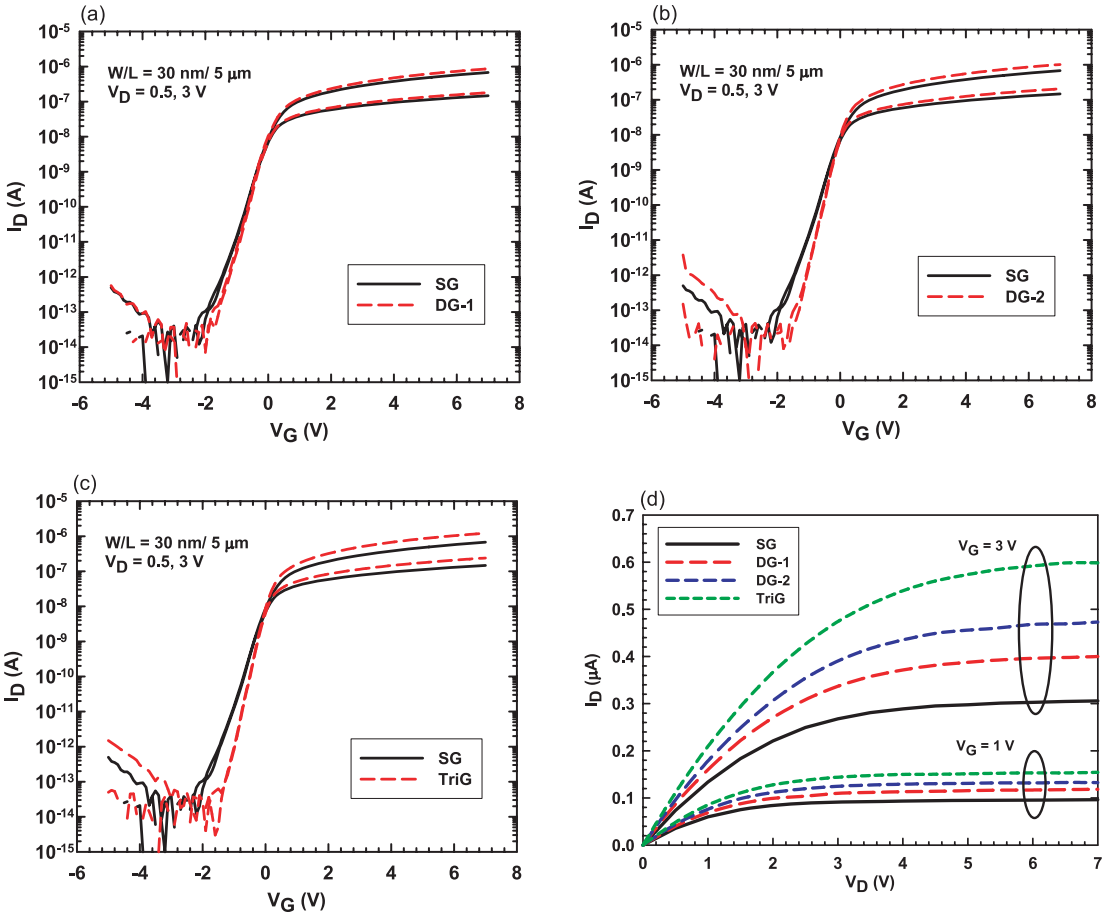

Figure 3. Typical transfer characteristics of an NW TFT under (a) DG-1, (b) DG-2 and (c) TriG modes of operations compared with SG mode, respectively. (d) Comparisons of output characteristics among MG and SG modes of operations.

(DG-1 and DG-2) and one triple-gated (TriG) mode. For the double-gated modes, the remaining gate was grounded throughout the measurements. Figures 3(a)–(c) present and compare the transfer characteristics of an NW device under the three modes of operations with that of SG operation. The significant merits of MG operations include lower threshold voltage ($V_{\rm th}$), steeper SS and higher $I_{\rm ON}$, owing to the stronger gate controllability over the NW channels. With those merits, an on/off current ratio higher than 10^7 is achieved. Output characteristics for all modes of operations are shown in figure 3(d), in which the $I_{\rm ON}$ at $V_{\rm G} = V_{\rm D} = 3$ V are 1.3, 1.5 and 1.8 times that of SG operation under DG-1, DG-2 and TriG modes, respectively. For the two double-gated modes, the performance is better under DG-2 mode. This is mainly attributed to the thinner gate dielectric used for the BG. Figure 4 shows the transconductance ($G_{\rm m} = {\rm d}I_{\rm D}/{\rm d}V_{\rm G}$

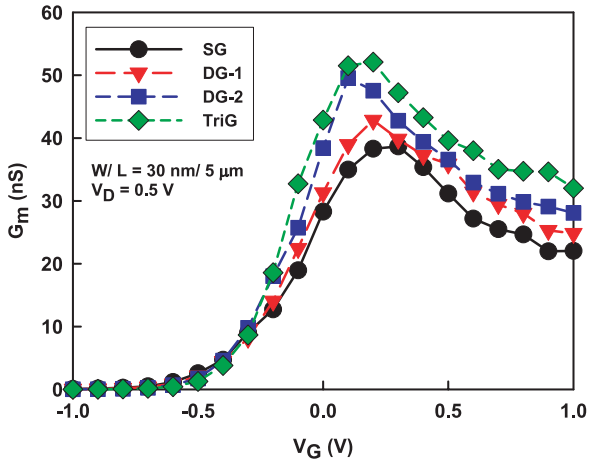

Figure 4. Transconductance characteristics of an NW device under various modes of operation.

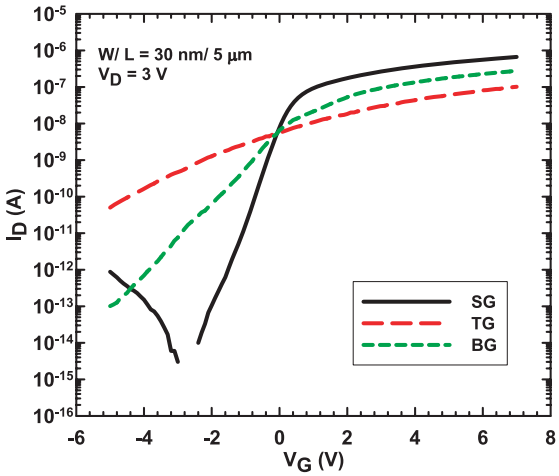

Figure 6. I–V curves of single-gated mode of operation.

at $V_D = 0.5$ V) characteristics under various modes. Due to the more effective conduction width evoked under the active gates, the MG operations indeed yield higher G_m as compared with the SG mode. To visualize this phenomenon, simulated electron densities in the two-dimensional cross-sectional area of the NW channel for on-state operation of DG-1, DG-2 and TriG modes are illustrated in figure 5. The simulation was carried using an ISE TCAD (Integrated Systems Engineering Technology-Computer-Aided Design) tool and the applied voltages to the active gates were all 5 V [13]. It is evident that more carrier density is induced with the MG modes. The enhancement in gate controllability also effectively reduces the subthreshold leakage current path inside the NW. This consistently explains the steeper subthreshold slope of MG modes than that of SG mode. Moreover, the increase in the effective conduction channel width leads to higher I_{ON} and G_m, especially under TriG mode of operation. The electron density is higher around the corners owing to the high electric-field strength. To quantitatively compare device performance among different modes, several important electrical parameters are summarized in table 2.

To further highlight the enhancement in gate controllability under MG configuration, I–V characteristics of a device operated under individual gate control are measured first, and then the sum is compared with that of MG operations. In figure 6, the characteristics of the three individual gate control modes are shown. In the measurements the two remaining gates were grounded; therefore these curves have a common intersection point at zero gate voltage. As can be seen in the figure, TG and BG operations exhibit larger subthreshold slope and lower on-state current than those under SG operation, which is reasonable because of their thicker gate dielectrics.

Table 2. Comparisons of the electrical parameters among various modes of multiple-gated operations.

	SG	DG-1	DG-2	TriG
V_{th} (V)	−0.45	−0.39	−0.34	−0.30
SS (V/dec.)	0.342	0.290	0.265	0.251
I_{ON} (A)	2.7×10^{-7}	3.4×10^{-7}	3.9×10^{-7}	4.8×10^{-7}
$G_{m,max}$ (nS)	42	45	55	60

The effectiveness of the MG configuration in improving the device performance can be understood from the results shown in figures 7–9. In figure 7, the curves denoted as 'SG + TG' indicate the sum of currents under individually side-gated and individually top-gated operations, as shown in figure 6. From the inset in the figure, it can be seen that the on-state current of the DG-1 mode is larger than the sum of the two single-gated modes. On the other hand, the subthreshold current is much smaller than the sum of the two single-gated

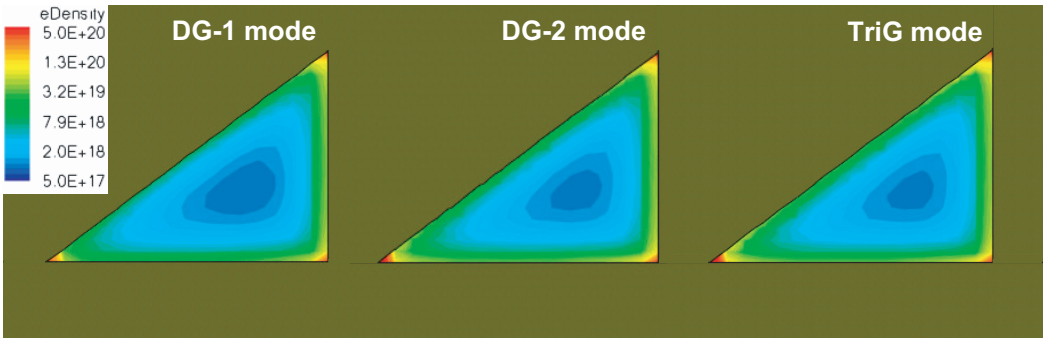

Figure 5. Two-dimensional simulation of electron density (eDensity) in NWs under DG-1, DG-2 and TriG modes of operation. The applied gate voltage is 5 V.

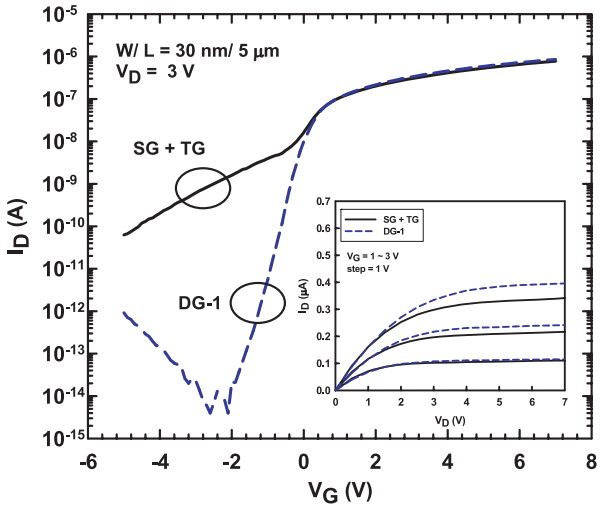

Figure 7. Transfer and output (inset) characteristics for DG-1 operation as compared with the sum of the current of two individual single-gated operations.

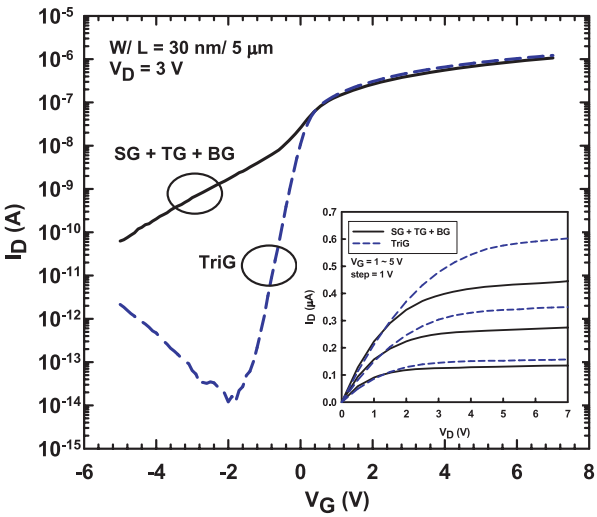

Figure 9. Transfer and output (inset) characteristics for TriG operation as compared with the sum of the current of three individual single-gated operations.

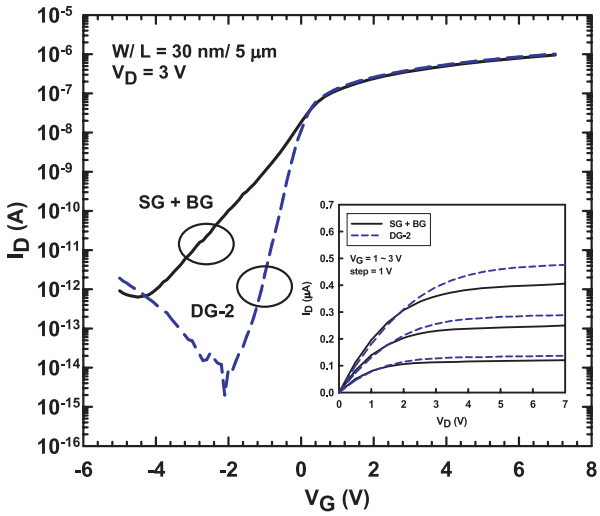

Figure 8. Transfer and output (inset) characteristics for DG-2 operation as compared with the sum of the current of two individual single-gated operations.

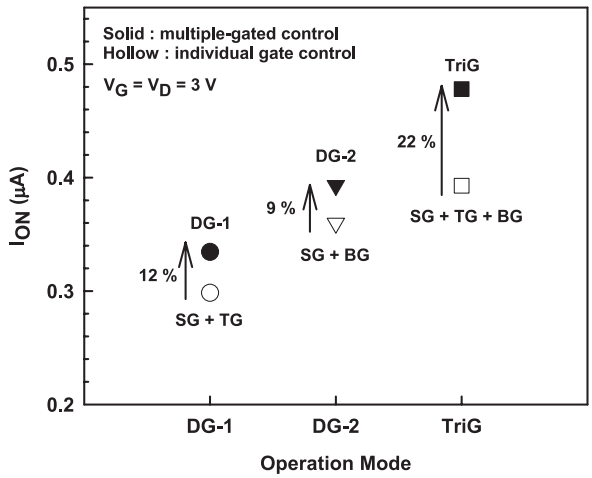

Figure 10. I_{ON} enhancement under MG control for the data shown in figures 7–9. Solid symbols indicate I_{ON} of MG control, whereas hollow ones represent the sum of I_{ON} of individual gate control.

modes. Similar findings are also observed for DG-2 and TriG modes of operations, as depicted in figures 8 and 9, respectively. The above phenomena are attributed to the strong coupling of the two adjacent gates during the MG operation, which tends to increase the effective conduction width in the on-state, leading to a higher conduction current. This tends to reduce the area of the leakage path, and thus leads to a reduced subthreshold leakage. These effects are magnified as the 'body' of NW is tiny. Figure 10 displays the percentage increase in I_{ON} for the MG modes over the sum of individual operations. It can be seen that the TriG mode indeed shows the most significant improvement.

In addition to the MG operations demonstrated above, V_{th} adjustment by applying a fixed TG and/or BG bias is also feasible in the proposed device structure. Figures 11(a)–(c) show typical results in this aspect. In the figures, the SG acts as the active gate for controlling the device switching behaviour. For each curve, a specific voltage (V_{set}) ranging from −4 to 4 V is applied to the TG (V_{TG}, figure 11(a)) or the BG (V_{BG}, figure 11(b)) alone, or jointly (V_{TG-BG}, figure 11 (c)). It can be found that the curves are shifted in parallel by varying the biases. Similar threshold voltage modulation has been studied on double-gated SOI devices previously, and was ascribed to the potential profile adjustment in the NW channel by the V_{set} [8, 14]. Figure 12 shows V_{th} as a function of the applied V_{set} extracted from the data shown in figures 11(a)–(c). The results reveal that V_{th} could be linearly tuned to a suitable range. The magnitude of the slope can be regarded as an indicator that reflects the tuning capability of V_{set}. Among the three cases, the slope is the smallest when V_{set} is applied to the TG only, due to the thick oxide used. The field strength is reduced with a thicker oxide, so the

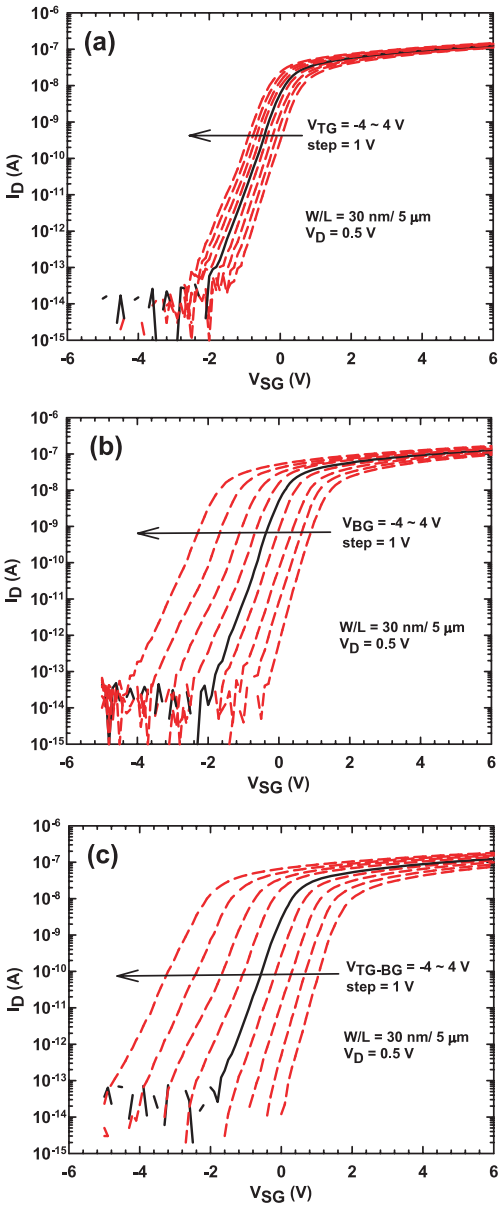

Figure 11. I_D–V_{SG} characteristics of a side-gated transistor with V_{set} applied to (a) the TG, (b) the BG and (c) both TG and BG.

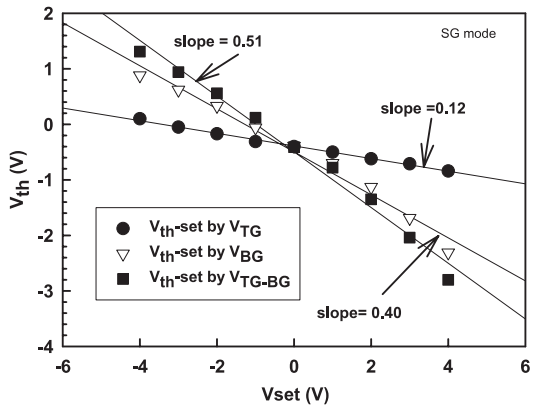

Figure 12. Dependence of V_{th} as a function of V_{set}.

potential adjustment capability is degraded accordingly. The largest slope is obtained when V_{set} is applied to both the TG and BG, thanks to the strong gate-coupling effect mentioned above. Similarly, for DG modes of operations, V_{th} could also be modulated by applying V_{set} to the remaining gate, as depicted in figure 13. These results suggest that the threshold voltage of the new MG NW TFT could be easily adjusted to suit various applications.

For NW devices, the variation of structural parameters such as the feature size of the NW and the gate dielectric thickness, as well as dopant concentrations in the channel, could result in large fluctuation in V_{th}. Yet, in the proposed method, V_{th} could be modulated in an electrical manner, and therefore the issue could be effectively resolved. Note that the unique capability of electrically tuning the threshold voltage in the new NW structure is beneficial not only for circuit applications in electronics, but also for gas and biologic sensing applications. As described in a previous paper [7], the new NW architecture could be applied to chemical and biological sensing purposes, as some portion of the channel is exposed to the environment, as schematically shown in figure 14. After immobilization treatment, receptors are formed on the surface of the exposed channel. During the sensing stage, the receptors can capture the target species contained in the test environment with good selectivity, and the charges brought with the captured target species will modulate the channel conductance. Overall the detection process functions as a virtual gate in the FET operation, and thus in reality the device is doubled-gated when the side-gate is also considered. To make the detection highly sensitive, it would be better if the device is operated in a bias condition in which the channel conductance is most sensitive to the surface charges. This could be achieved by applying a proper voltage (V_{set}) to the side-gate according to the above analyses, as shown in the figure. The applied side-gate voltage could be generated from a control circuit designed and fabricated using modern complementary metal–oxide–semiconductor (CMOS) technology. This certainly increases the feasibility of the new NW device in practical applications.

4. Conclusions

In conclusion, a poly-Si NW device with MG configuration was proposed, fabricated and characterized in this study. The NW channels are surrounded by three gates, i.e., top-gate, side-gate and bottom-gate, fabricated with a very simple and controllable process flow. With MG operations, excellent electrical characteristics such as high on/off current ratio of 10^7 and subthreshold slope of 250 mV/dec. are obtained, which are significantly better than those reported in previous work using only the side-gate to control the device switching. The strong gate-coupling effect of the MG operation, which is ascribed to the tiny body of NW channels, accounts for the observed improvement. Moreover, the independently applied TG or/and BG biases can be employed to regularly adjust the V_{th} of NW channels in a reliable manner. The experimental results indicate that the V_{th} could be modulated by the gates with both positive and negative biases, making the scheme

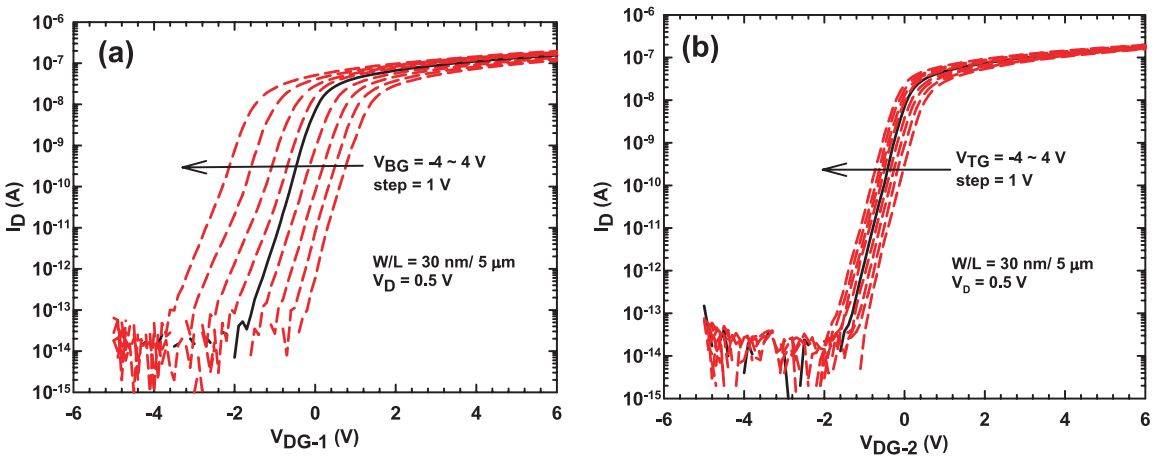

Figure 13. Transfer behaviours of the double-gated transistor with various TG or BG biases: (a) DG-1 mode and (b) DG-2 mode.

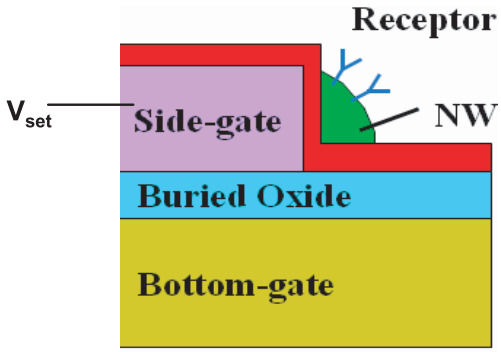

Figure 14. For sensing applications, V_{set} generated from a control circuit (not shown) could be used to set the NW channel potential to a condition most sensitive to the surface charges of the exposing site.

suitable for practical applications. The proposed NW TFT architecture is therefore promising for future manufacturing of high-performance NW devices.

Acknowledgments

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