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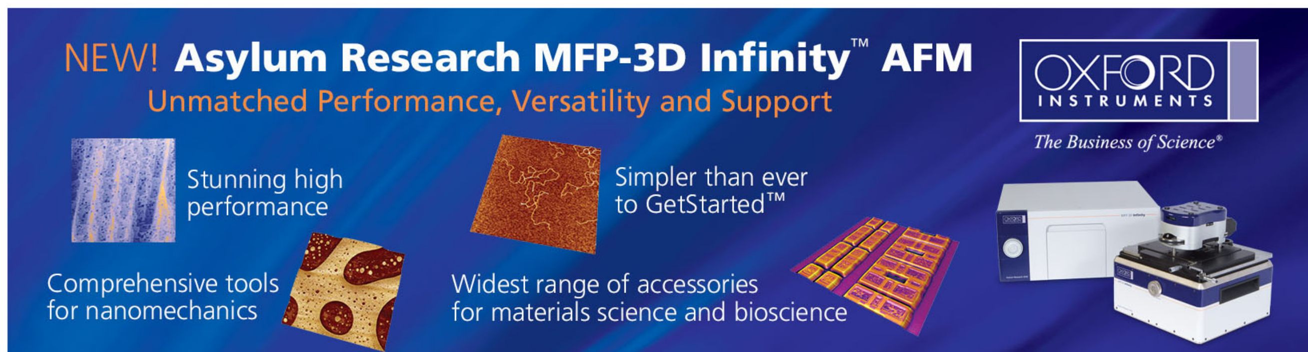

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Nickel nanocrystals with HfO_2 blocking oxide for nonvolatile memory application

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A distributed charge storage with Ni nanocrystals embedded in the SiO_2 and HfO_2 layer has been fabricated in this study. The mean size and aerial density of the Ni nanocrystals are estimated to be about 5 nm and $3.9 \times 10^{12}/cm^2$, respectively. The nonvolatile memory device with Ni nanocrystals exhibits 1 V threshold voltage shift under 4 V write operation. The device has a long retention time with a small charge lose rate. Besides, the endurance of the memory device is not degraded up to 10^6 write/erase cycles. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2743926]

In 1967, Kahng and Sze invented the floating-gate (FG) nonvolatile semiconductor memory at Bell Laboratory.[1] Nonvolatile memory devices with FG structure are being used widely such as mp3 player, digital cameras, and integrated circuit cards at present. The most important one is the limited potential for continued scaling of the device structure. When the tunnel oxide is thinner, the retention characteristics may be degraded. When the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower.[2] The use of a floating gate composed of distributed nanocrystals reduces the problems of charge loss encountered in conventional floating-gate electrically erasable programable read-only memory devices, allowing for thinner tunnel oxide and, thereby, smaller operating voltages, better endurance and retention, and faster program/erase speed.[3] Nanocrystal memory devices employing distributed nanodots as storage elements have exhibited great potential in device applications.[4–10] Among the different materials of nanocrystals, the metal nanocrystal memory possesses several advantages, such as stronger coupling with the conduction channel, a wide range of available work functions, higher density of states around the Fermi level, and smaller energy perturbation due to carrier confinement.[11] Besides, using the high-*k* dielectric as the blocking oxide concentrates and releases the electric fields across the tunnel oxide and the blocking oxide, respectively, under the program/erase mode. Using the high-*k* dielectric as the blocking oxide leads to lower program and erase voltage.[12]

In this letter, we demonstrated the memory characteristics of Ni nanocrystals embedded in SiO_2 and HfO_2, which is desirable for applications of the nonvolatile memory technology. Its implementation is compatible with the current manufacturing technology of semiconductor industry.

Metal-oxide-silicon capacitors were fabricated using silicon *p*-type wafers [(100) orientation]. First, the wafers were chemically cleaned by a standard Radio Corporation of America cleaning. The thin tunnel oxide (3 nm) was thermally grown at 1000 °C in vertical furnace system. Subsequently, a 3-nm-thick nickel layer was deposited onto the tunnel oxide by electron beam evaporation. The Ni wetting layer transformed the Ni nanocrystals after the rapid thermal annealing in the N_2 ambient at 500 °C for 60 s. A 30-nm-thick blocking oxide (HfO_2) was capped by sputter. The parameter of the high-*k* sputtering is 0.3 Å/s as rf power sputter in 150 W under the working pressure of 20 mTorr. The flow rate of Ar/O_2 is 20/5 SCCM (SCCM denotes cubic centimeter per minute at STP). The dielectric constant of HfO_2 is 20. Finally, Al gate electrode was patterned and sintered. The structural analyses were performed by transmission electron microscopy (TEM). The capacitance-voltage (*C-V*) measurements were performed by a precision *LCR* meter HP 4284A to study the electron charging and discharging effects of the Ni nanocrystals.

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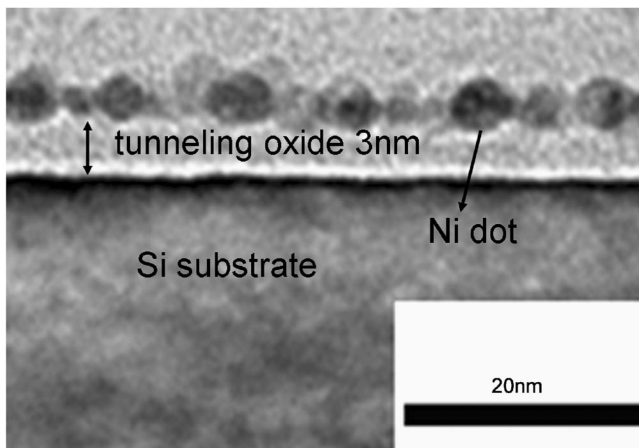

FIG. 1. Cross-section TEM micrographs of a $Ni/SiO_2/Si$ stacked structure.

Figure 1 shows the cross-section TEM of Ni nanocrystal memory structure. The figure presents the structure of Si substrate/tunneling oxide/Ni nanocrystals. The well-separated and spherical Ni nanocrystals are observed. The higher-resolution image confirms the presence of Ni nanocrystals of approximately 5 nm in diameter. The aerial density of the Ni nanocrystals is measured to be $3.9 \times 10^{12}/cm^2$.

Figure 2 presents the *C-V* characteristics of Ni nanocrystals embedded between the SiO_2 and HfO_2 layers. It is found that a low operating voltage, 4 V, causes a significant threshold voltage shift up to ~1 V, which is sufficient to be defined as "1" or "0" for the logic-circuit design. The electrons of the deep inversion layer and holes of the deep accumulation layer were injected from the Si substrate into the nanocrystals, so that the *C-V* hysteresis is counterclockwise. The high-*k* blocking oxide concentrates the electric fields across the tunnel oxide and releases it across the blocking oxide under program and erase mode. This effect leads to lower program and erase voltage. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the Ni nanocrystals by Fowler-Nordheim tunneling. In addition, the Ni nanocrystals do not bear a voltage drop from gate voltage, which means that all the voltages provided from control gate are dropped to tunnel oxide and control oxide and gain advantage over their semiconductor counterparts.

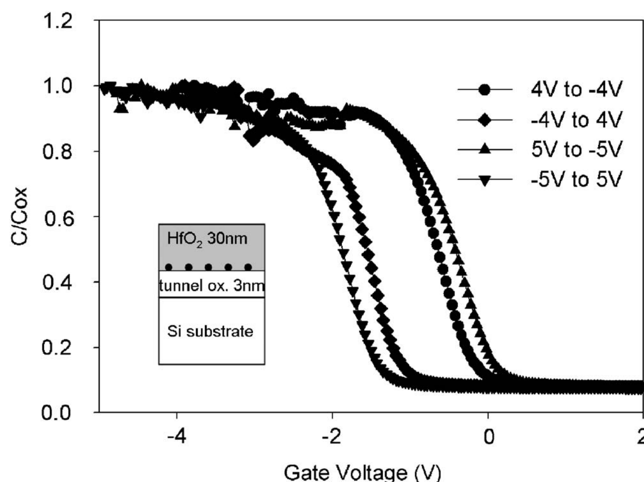

FIG. 2. Capacitance-voltage (*C-V*) hysteresis of Ni nanocrystal memory device after bidirectional sweeps between 4/−4 and 5/−5 V.

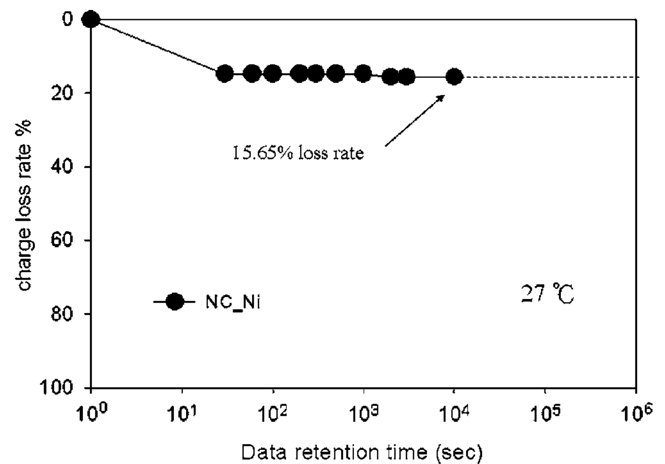

FIG. 3. Retention characteristics of the Ni nanocrystal memory device at room temperature.

The retention characteristics of the Ni nanocrystals were measured at room temperature, as shown in Fig. 3. If there are some leakage paths for the trapping charges, the memory effect will gradually decrease. In Fig. 3, the good retention characteristics can be found and the memory effect without significant decreasing up to 10^4 s. The charge loss rate only decreases to 15.65% after 10^4 s. It is clearly shown that the Ni nanocrystal memory has excellent retention characteristic.

The programing characteristics of Ni nanocrystal memory were studied by stressing samples with a pulse voltage of ±5 V and a pulse width of 5 ms during programing and erasing (P/E). Figure 4 shows the endurance characteristics of Ni nanocrystal memory after different stressing cycles at room temperature. The threshold voltage shift as a function of stressing cycles shows superior endurance. There was no degradation of the threshold voltage shift observed even after 10^6 P/E cycles.

In summary, the nonvolatile memory device with Ni nanocrystals exhibits 1 V threshold voltage shift under 4 V write operation, which is sufficient for a memory device to define the signal 0 and 1. The device has a long retention time with a small charge lose rate. Besides, the endurance of the memory device is not degraded up to 10^6 write/erase cycles.

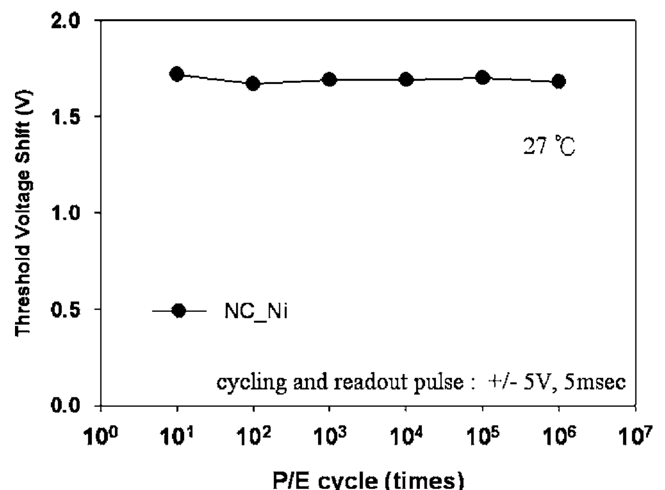

FIG. 4. Endurance characteristics of the Ni nanocrystal memory device at room temperature.

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