Near-infrared femtosecond laser crystallized poly-Si thin film transistors

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Abstract: Polycrystalline silicon (poly-Si) thin film transistors (TFTs) fabricated by near-infrared femtosecond laser annealing (FLA) are demonstrated. The FLA-annealed poly-Si channels exhibit low tail-state, deep-state, and midgap-state densities of grain traps. Characteristics such as field-effect mobility, threshold voltage, and subthreshold slope for FLA-annealed poly-TFTs are comparable to those of conventional approaches. A wide process window for annealing laser fluences was confirmed by examining the changes in electrical parameters for transistors with various channel dimensions.

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1. Introduction

Laser-induced crystallization and activation are now widely recognized as useful techniques for fabrication of various devices [1-6]. Important applications include formation of polycrystalline channels in thin film transistor (**TFTs**) on glass substrates for displays and shallow junction formation in silicon nanoelectronics [2-6, 7-8]. In particular, the excimer laser has been proved to be a powerful tool for annealing of amorphous silicon layers, activation of shallow junctions and fabrication of TFTs [9-12]. Recently, we reported near-infrared (λ= 800 nm) femtosecond laser annealing (**FLA**) for crystallization of amorphous silicon (**a-Si**) and activation of dopant atoms confined in ultra shallow junction regions [13-14]. Unlike continuous-wave laser annealing and excimer laser annealing (**ELA**), the low fluence (~ 45mJ/cm^2) required for FLA suggests that ultrafast or non-thermal melting of semiconductors is the dominant mechanism [1-6, 15-17]. Femtosecond optical pulses can excite significant numbers of the valance electrons in the semiconductor through nonlinear absorption. The photoexcited electron systems then weaken the lattice and lead to structural transformation such as re-crystallization. This can occur while the electronic system and lattice are not in a thermal equilibrium [16]. Grains as large as ~800 nm were obtained using laser fluence as low as ~ 45 mJ/cm^2 [13]. Moreover, the optimal annealing conditions are observed with a relatively broad laser-fluence window for which the grain size variation of the annealed samples are in less than ~30%. On the other hand, we found dopant diffusion in silicon substrates implanted with boron or phosphorous was negligible after FLA-activation. The activation efficiencies were as high as 28-35% [14]. In this letter, we report thin film transistors fabricated on channels crystallized by FLA for the first time. Good transistor characteristics, as confirmed by measurements of electrical parameters and grain trap-state densities were obtained for a wide process window of annealing laser fluences.

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2. Experimental methods

Amorphous Si layers of 100 nm were deposited by low pressure chemical vapor deposition (**LPCVD**) at 550 °C on 500 nm-SiO_2-coated silicon wafers. The active layers for the TFTs were crystallized by line-scanning irradiation of twenty ultrafast (~ 50 fs) near-infrared (λ = 800 nm) laser pulses with fluences of 34-50 mJ/cm^2 (or total laser fluences of 0.68-1.0 J/cm^2). The beam spot size was 8mm×110μm. During the scanning process, the overlapping of neighboring pulses was fixed at 95%. FLA was conduced on a substrate heated at 400 °C in a vacuum chamber. A movie of the annealing process is available online. FLA-crystallized layers were then defined into active regions for transistors with channel length (L)/ channel width (W) of 2μm/2μm, 3μm/3μm, 5μm/5μm, and 10μm/10μm. A SiO_2 gate dielectric layer of 50 nm and polycrystalline silicon gate layer of 150 nm were then grown by LPCVD and patterned for self-aligned phosphorous implantation with dosage of 5×10^{15} cm^{-2}, and energy of 53 keV. After thermal activation and metal connection were performed, n-type transistors were completed. For comparison, TFTs with channels crystallized by furnace annealing (solid phase crystallization, **SPC**) in nitrogen ambient at 600 °C for 24 hours were also processed on the same run. The transfer characteristics (drain current I_d versus gate voltage V_g) of the devices were measured at a drain voltage V_d = 0.1 V, to extract electrical parameters. Grain trap-state densities, n_{GT}, for all TFTs were also examined using the field-effect conductance method [18].

3. Results and discussions

In Fig. 1, we have plotted logarithmic transfer characteristics and linear transconductance (G_m) curves for some representative TFTs fabricated by FLA and SPC.

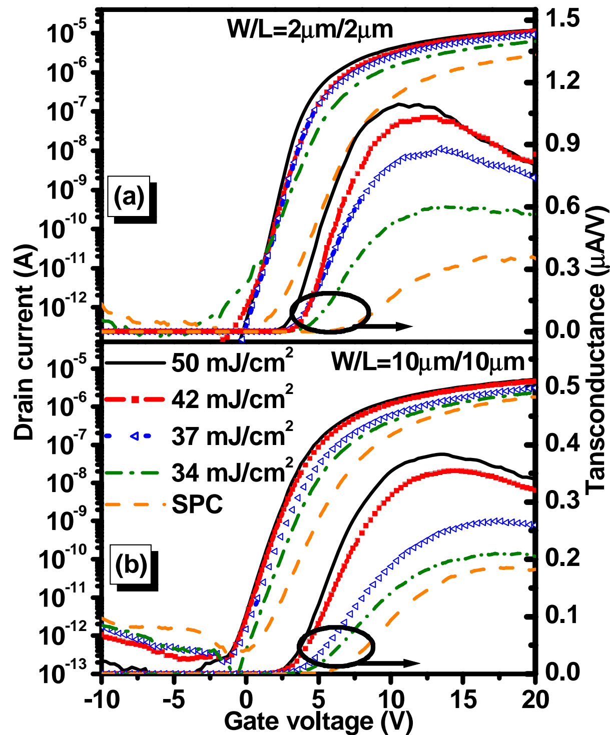

Fig. 1. Transfer characteristics and transconductance versus gate voltage for FLA and SPC processed TFTs with channel dimensions of (a) W = L= 2 μm and (b) W = L= 10 μm.

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For TFTs with channel dimensions of W = L = 10 μm and W = L = 2 μm, the on/off current ratio was better than 10^7. As the laser fluence decreased from 51 to 34 mJ/cm^2, significant decrease of G_m was observed due to the deterioration of crystallinity. Even at the lowest fluence we employed, the maximum G_m of TFTs fabricated by SPC was lower than that of TFTs annealed by FLA. The maximum values of G_m were analyzed to yield the field-effect electron mobility (μ_{FE}). The threshold voltage (V_{th}) and the subthreshold slope (S) were then extracted using the procedure described in reference 19. Electrical parameters of FLA-processed TFTs are presented as functions of channel sizes and laser energy in Fig. 2.

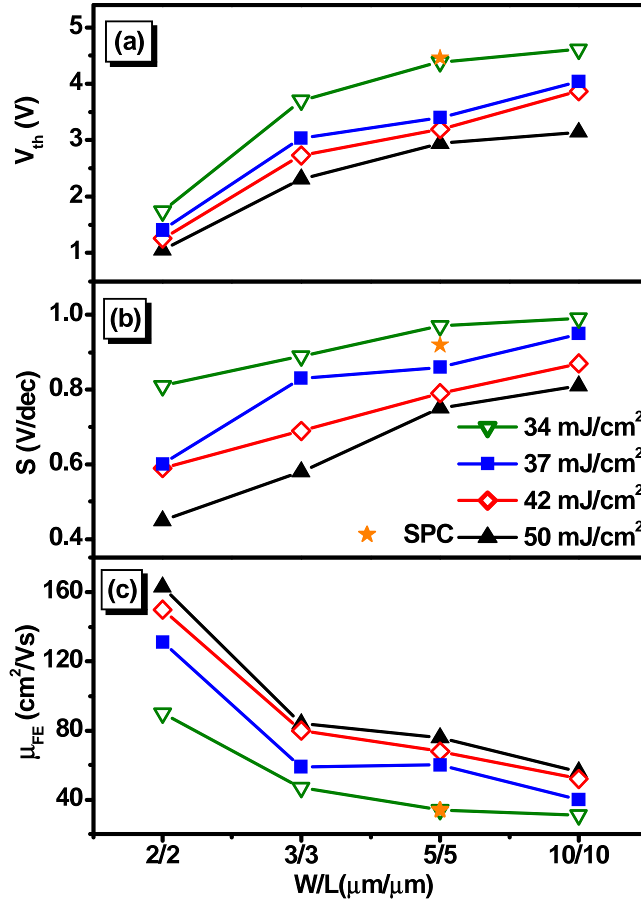

Fig. 2. (a). Threshold voltages, (b) subthreshold slopes and (c) mobilities for TFTs annealed by FLA with different fluences and the SPC process.

It is well-known that the tail-state density of grain traps, N_G, closely correlates with channel crystallinity [20]. We find the values of N_G at an energy (E) ~ 0.5 eV above the Fermi level (E_F), for transistors with channels of 5μm/5μm, decrease from ~3.5×10^{21} to 1.5×10^{21}eV^{-1}cm^{-3} as the laser fluence increases from 37mJ/cm^2 to 50mJ/cm^2. This is shown in Fig. 3. Clearly, larger grains with fewer associated defects were obtained at increasing laser fluence up to 50mJ/cm^2. This reduces considerably the height of the barrier to carrier transportation in the channels. As a result, higher G_m values are obtained (see Fig. 1). Similar trend for μ_{FE} can be observed in Fig. 2, regardless of channel sizes.

Increasing channel crystallinity normally reduces the density of the grain defects, including deep-states defects. Increasing laser fluences, we find that deep-state and

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midgap-state densities of grain traps decrease for the device with channels of 5μm/5μm, to 4×10^{18} cm^{-3} (at $E-E_f$ = **ΔE**= 0.25 eV), and 1×10^{18} $eV^{-1}cm^{-3}$ (at **ΔE**~ 0 eV), respectively (See Fig. 3).

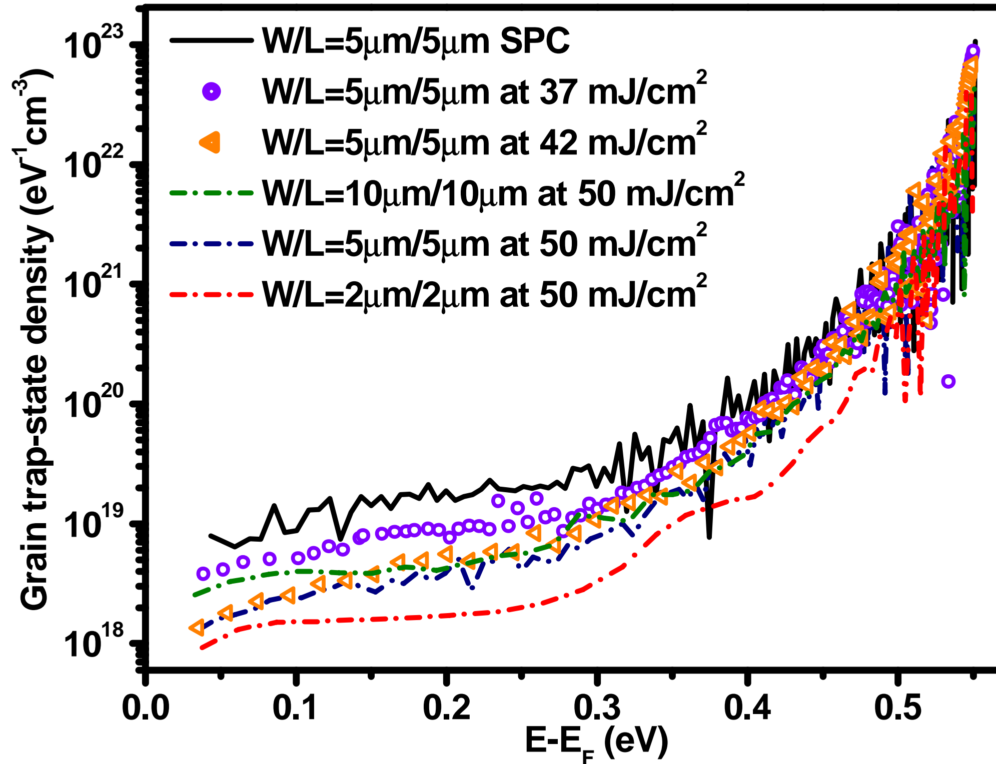

Fig. 3. Grain trap-state density in the energy bandgap of the poly-Si channels of TFTs with different channel dimensions processed by SPC and FLA at various fluences.

Area densities of grain trap-states, N_G, at **ΔE** = 0 eV for devices in Fig. 3, are estimated from $N_G \approx n_{GT}.t_{CLC}$ where t_{CLC} represents the thickness of FLA-crystallized polycrystalline silicon. For the same TFT, we find the values of N_G are in a good agreement with those of the effective trap state densities N_t calculated from subthreshold slope.

It is reasonable to expect that the device performance or electrical characteristics of TFTs should directly correlate with the structural characteristics such as the grain sizes and the surface roughness of amorphous films annealed by different methods. As we have shown in a previous study [13], the grain sizes of FLA-annealed samples are comparable to those of ELA-annealed ones reported in the literature [22]. From XRD (x-ray diffraction) analysis (not shown), we found that the preferred orientations of ELA- and FLA-annealed poly-Si layers are both (111). Raman spectroscopic studies [13, 23] revealed a single sharp peak at 519 cm^{-1} and 515cm^{-1} for FLA- and ELA-annealed poly-Si layers, respectively. The RMS surface roughness of the former (< 10 nm, Ref. 13), is comparable but slightly better than that of the latter (10-20 nm).

Previous workers have shown that the values of N_G were more affected by interface defects associated with channel roughness in ELA processed TFTs [21]. In this work, however, we find that $N_G \approx N_t$. This implies that channel crystallinity rather than channel roughness in such FLA-crystallized polycrystalline silicon layers, which exhibit sub-micro

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grains and smooth surfaces with roughness of ~ 4-9 nm, dominates electrical characteristics of fabricated transistors (See Figs. 2 and 3).

The deep-state dominated subthreshold slope and threshold voltage both follow the trend of reduction in grain deep-states densities with laser fluence (See also Figs. 2 and 3). Similar trend was also observed in ELA-processed devices [20]. The grain trap-state densities in Fig. 3 also show that the FLA-annealed TFTs are superior to SPC-annealed TFTs, consistent with that of the electrical parameters presented in Fig. 2.

In the range of laser fluences of 37-50 mJ/cm^2, the electrical characteristics of TFTs crystallized by FLA vary by at most 30%, regardless of channel sizes. The relatively small variations of electrical parameters for fractional change of fluence ($\Delta E/E$) in FLA is lower than that reported (80%) of TFTs fabricated by ELA [22]. Such a wide FLA-crystallization window as determined by transistor characteristics agrees with our previous studies of structural characteristics of poly-Si crystallized by FLA and grain trap-state densities associated with channel crystallinity as presented herein [13].

The tail-state densities (at $\mathbf{\Delta E}$= 0.5 eV) of FLA-fabricated transistors with different channel sizes are in the range of 6×10^{20} to 1×10^{21} eV^{-1}cm^{-3}. The values are of the same order of magnitude as those obtained from ELA-crystallized polycrystalline silicon layers [22]. As expected, mobilities of FLA-fabricated transistors, $\mu_{FE} \approx$ 80-160 cm^2/Vs, are also comparable to those for ELA-fabricated transistors. We also note that grain trap-state densities for those channels with different sizes but the same crystallinity decline as channel size decreases. This is also in agreement with previous studies using other annealing technologies [24]. Fewer numbers of grain defects in smaller channels will result in better electrical characteristics in TFTs as confirmed in results for FLA-fabricated TFTs (Fig. 2).

4. Conclusion

In summary, polycrystalline silicon (poly-Si) transistors fabricated by near-infrared femtosecond laser annealing were demonstrated for the first time. The FLA-annealed poly-Si channels exhibit low tail-state, deep-state, and midgap-state densities of grain traps of ~1×10^{21}, ~5×10^{18}, and ~9×10^{17} eV^{-1}cm^{-3}. Field-effect mobility, threshold voltage, and subthreshold slope for transistors fabricated on poly-Si annealed with a total fluence of 0.9 J/cm^2 in a line-scan mode were measured to be 80-160 cm^2/Vs, 1-3 V, and 0.4-0.8 V/dec, respectively. These parameters are superior to those of SPC-processed while comparable to those of ELA-fabricated transistors. On the other hand, a much wider FLA process window than ELA was observed. We also show that channel crystallinity rather than channel roughness in such FLA-crystallized polycrystalline silicon layers, which exhibit sub-micro grains and smooth surfaces with roughness of ~ 4-9 nm, dominates electrical characteristics of fabricated transistors.

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