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F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, U. S. Chen, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou

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Using double layer $CoSi_2$ nanocrystals to improve the memory effects of nonvolatile memory devices

F. M. Yang
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

T. C. Chang[a)]
Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan 804, Republic of China; Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 804, Republic of China; and Center for Nanoscience and Nanotechnology, National Sun Yat-sen University, 70 Lien-hai Road, Kaohsiung, Taiwan 804, Republic of China

P. T. Liu
Department of Photonics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China and Display Institute, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

P. H. Yeh[b)] and U. S. Chen
Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan 300, Republic of China

Y. C. Yu and J. Y. Lin
Graduate School of Opto-Electronics Engineering, National Yunlin University of Science and Technology, Yunlin, Taiwan 640, Republic of China

S. M. Sze and J. C. Lou
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

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The nonvolatile memory device with multilayer nanocrystals has advantages such as the memory effects can be increased by the increasing density of the nanocrystals and the whole retention characteristic can be improved. There are much more electrons that can be stored in the double layer than single layer nanocrystal memory device. The double layer $CoSi_2$ nanocrystals have better retention characteristic than the single layer. The good retention characteristic of the double layer device is due to the Coulomb-blockage effects on the top layer nanocrystals from the bottom layer nanocrystals. So, the memory effects of the nonvolatile memory device can be improved by using the double layer nanocrystals. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2742573]

Memory devices employing distributed nanocrystals as storage elements have exhibited great potential to replace conventional dynamic random array memory or flash memories for future high speed and low-power consumer memory devices.[1–5] Nanocrystalline silicon was introduced as a replacement for the conventional floating gate in the nonvolatile memory structure by Tiwari *et al.*[1] To date, most studies have focused on the fabrication on Si and Ge nanocrystals in metal-oxide-semiconductor structure.[6–11] The use of a floating gate composed of distributed nanocrystals reduces the problems of charge loss encountered in conventional floating-gate electrically erasable programable read-only memory devices. It allows thinner tunnel oxide and, thereby, smaller operating voltages, better endurance and retention, and faster program/erase speed.[12,13]

The metal nanocrystal memory possesses several advantages, such as stronger coupling with the conduction channel, a wide range of available work functions, higher density of states around the Fermi level, and smaller energy perturbation due to carrier confinement.[14] Its implementation is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for low-power nanoscaled nonvolatile memory devices.

In the preset study, two sets of samples were prepared. The process flow are as follow; (100) oriented *p*-type silicon wafers were chemically cleaned by a standard RCA cleaning, followed by a dry oxidation in an atmospheric pressure chemical vapor deposition furnace to form a 3-nm-thick tunnel oxide. Subsequently, *a*-Si (3 nm)/Co (3 nm)/*a*-Si (3 nm) layers were deposited onto the tunnel oxide by electron beam evaporation and plasma enhanced chemical vapor deposition. The compared sample with single layer $CoSi_2$ nanocrystals was without the *a*-Si (3 nm) layer. The stacked structure was, afterwards, thermally annealed at 700 °C for 10 min to form the double layer $CoSi_2$ nanocrystals. Subsequently, the 30-nm-thick HfO_2 was capped on the stacked structure. Finally, Al gate electrode was patterned and sintered. The structural analyses were performed by transmission electron microscopy (TEM). The capacitance-voltage (*C-V*) measurements were performed by a precision *LCR* meter HP 4284A to study the electron charging and discharging effects of the $CoSi_2$ nanocrystals.

The inset of Fig. 1 represents a typical bright-field, cross-section TEM image. After dry oxidation, the well-separated and spherical double layer $CoSi_2$ nanocrystals are observed. The $CoSi_2$ nanocrystals were located between the tunnel oxide and the control oxide. The characteristic is beneficial for the reliability and the yield of the memory device.

a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw
b)Electronic mail: phyeh331@gmail.com

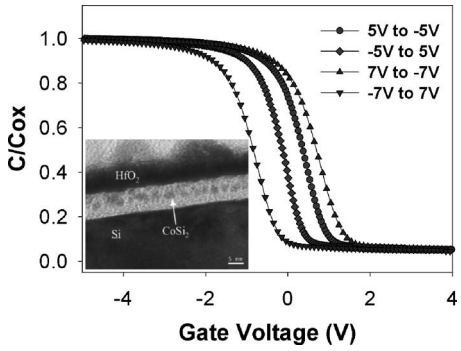

FIG. 1. Capacitance-voltage (*C-V*) hysteresis of $CoSi_2$ nanocrystal memory device after bidirectional sweeps between 5/−5 V and 7/−7 V. The inset is cross-section TEM micrographs of a $CoSi_2$ stacked structure.

Figure 1 shows the forward and reverse sweep capacitance-voltage (*C-V*) characteristics, indicating the electron charging and discharging effects of $CoSi_2$ nanocrystals embedded in dielectrics. The bidirectional *C-V* sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited electron charging effect. In Fig. 1, with the voltage swept from 5 to −5 V and back to 5 V, an outstanding threshold voltage shift of 0.5 V is observed. As the whisked voltage was increased to 7 V, a more obvious *C-V* shift of 1.5 V was seen. It is perceived that the hysteresis is counterclockwise, which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate. The result of *C-V* shift indicated that the charging effects of double layer $CoSi_2$ nanocrystals are more significant than the semiconductor nanocrystals. Figure 2 shows the different memory effects of the single and double layer $CoSi_2$ nanocrystals. There are much more electrons that can be stored in the double layer than single layer nanocrystal memory device. The retention characteristics can be seen in Fig. 3(a). The double layer $CoSi_2$ nanocrystals have better retention characteristic than the single layer. The good retention characteristic of the double layer device is due to the Coulomb-blockage effects on the top layer nanocrystals from the bottom layer nanocrystals, as shown in Fig. 3(b).[15] So, the memory effects of the nonvolatile memory device can be improved by using the double layer nanocrystals. Figure 4 shows the band diagrams of "write" and "erase" operations of the double layer nanocrystals with different gate polarities of the memory device. When the device is written or programed, the electrons directly tunnel from the Si substrate through the tunnel oxide and are trapped in the top and bottom layer $CoSi_2$ nanocrystals. When the device is erased, the electrons may tunnel back to the deep accumulation layer of Si substrate. The control oxide is utilized to prevent the carriers of gate electrode from injecting into the $CoSi_2$ nanocrystals by Fowler-Nordheim tunneling. In addition, the

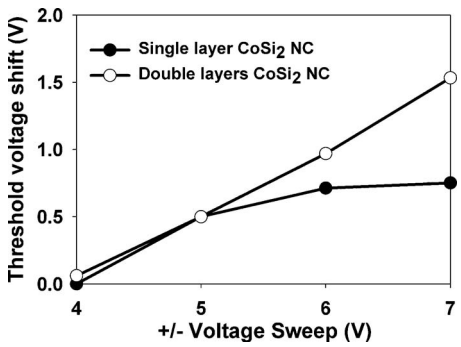

FIG. 2. Different memory effects of the single and double layer $CoSi_2$ nanocrystals.

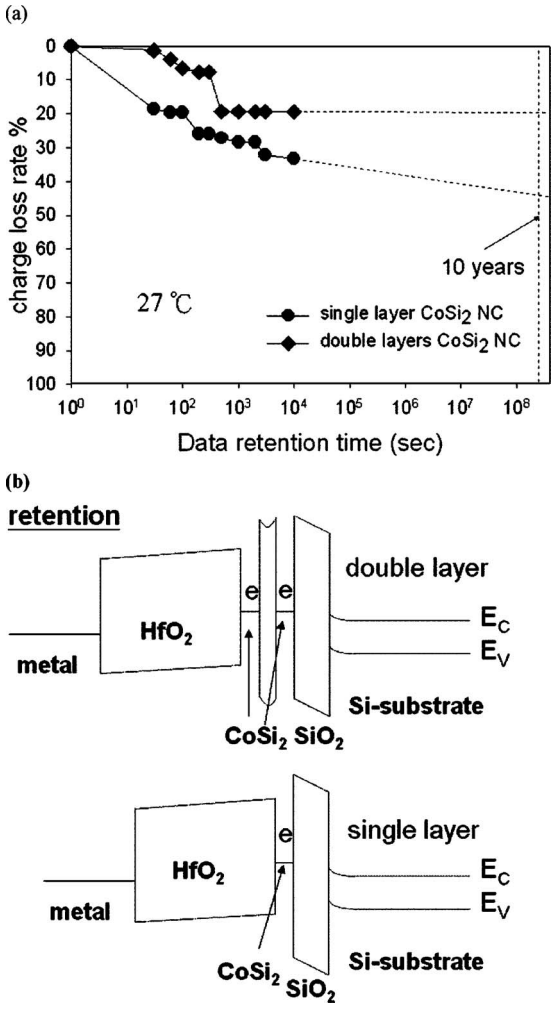

FIG. 3. (a) Data retention characteristics of the $CoSi_2$ nanocrystal memory device. (b) The band diagrams $CoSi_2$ nanocrystal memory device in retention.

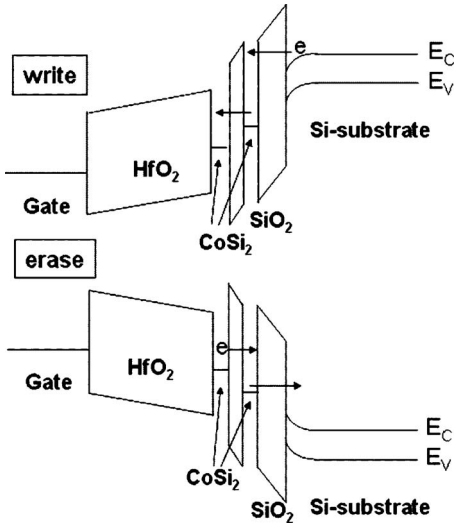

FIG. 4. Band diagrams of "write" and "erase" operations of the double layer nanocrystals with different gate polarities of the memory device.

$CoSi_2$ nanocrystals do not bear a voltage drop from gate voltage, which means all the voltages provided from control gate are dropped to tunnel oxide and control oxide and gain advantage over their semiconductor counterparts. In our approach to fabricate the double layer $CoSi_2$ nanocrystals embedded in dielectrics, a lower programing voltage of 5 V and erasing voltage of −5 V realize a significant threshold voltage shift, which is sufficient to be defined as "1" and "0" by a typical sensing amplifier for a memory device.

In summary, we have demonstrated the electron charging and discharging effects of double layer $CoSi_2$ nanocrystals embedded in dielectrics. The double layer $CoSi_2$ nanocrystals were formed by the thermal annealing of the *a*-Si (3 nm)/Co (3 nm)/*a*-Si (3 nm) multilayer structure. A significant *C-V* hysteresis of voltage shift of 1.5 V is observed under voltage operation of 7 V. The memory effects of the nonvolatile memory device can be improved by using the double layer nanocrystals. The implementation of the present structure is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for low-power nanoscaled nonvolatile memory devices.

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