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A low-power CMOS LNA for ultra-wideband wireless receivers

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Abstract: In this paper, a low-power ultra- wideband (UWB) low-noise amplifier (LNA) is proposed. Here, we propose a structure to combine the common gate with band pass filters, which can reduce parasitic capacitance of the transistor and to achieve input wideband matching. The π-section LC network technique is employed in the LNA to achieve sufficient flat gain. A bias resistor of large value is placed between the source and the body nodes to prevent body effect and reduce noise. Numerical simulation based on TSMC 0.18 μm 1P6M process. It achieved 10.0$\sim$12.4 dB gain from 3 GHz to 10.6 GHz and 3.25 dB noise figure in 8.5 GHz, operates from 1.5 V power supply, and dissipates 3 mW without the output buffer.

Keywords: low noise amplifier, low power, ultra-wideband

Classification: Integrated circuits

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1 Introduction

Ultra-wideband (UWB) communication techniques have attracted great interests in both academia and industry in the past few years for applications in short-range and high-speed wireless mobile system. For such broadband applications, wideband input matching and sufficient gain over the entire bandwidth are important for signal recovery and are also design challenges for ultra-wideband (UWB) low-noise amplifiers (LNAs).

The design of UWB LNA is one of the important challenges, because it connects with the antenna and pre-select filter, and the input matching should be 50 Ω over the whole bandwidth [2]. Low noise amplifier (LNA) is typically the first stage of a receiver with the function of providing enough gain to overcome the noise of subsequent stages. There are several common goals in the design of LNA including low noise figure (NF), a reasonable gain with sufficient linearity, good input matching, and low power consumption.

Three major CMOS UWB LNA design techniques had been reported for wideband communication application. The well-developed distributed amplifier is known as its wide bandwidth, but it requires large power consumption and layout area [3]. The filter design technique and source inductor degeneration technique are employed to incorporate the transistor gate-source capacitance as a part of the LC-ladder matching network and extend the bandwidth to a wide range [2, 4]. A common gate (or the 1/gm termination) amplifier has the highest potential to achieve the wideband input matching, good linearity, and input-output isolation, but it leads to lower gain and higher noise figure than using a common source amplifier. Only a few literatures have reported on the design of a common gate LNA [5].

In this paper, a novel LNA using a π-section LC network and a common-gate combined with a band pass filter is proposed. The LNA achieves a flat gain performance over the frequency range of 3 GHz to 10.6 GHz and also consumes very low power.

2 Circuit Descriptions

Due to the requirement of ultra-wideband, the following issues need to be considered:

- Input matching. (Reflection coefficient)
- Low noise.
- Reasonable gain.
- Low power consuming.

It is well-known that these four issues are trade-offs one another. Here, achieving optimum low power performance is our first priority. Our proposed UWB LNA circuit is shown in Fig. 1 (a), which employs the CMOS process. The proposed LNA can be broken down into three parts.

A. Wideband input matching network

Here, a common-gate amplifier is used as an important component for the input matching network of the proposed LNA. Although the common gate amplifier can easily achieve wideband input matching, good linearity,

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and input-output isolation, its parasitic capacitances of the transistor, will degrade the LNA performance in the high frequency region. Therefore, a two-order band pass filter is also introduced to reduce the parasitic capacitance. Fig. 1 (c) shows lumped element circuits for the two order band-pass filter. Its matching network is adopted for noise and impedance match to the 50 Ohm source with L_1=1 nH, C_1=850 fF, L_s=3.5 nH, C_2+C_{gs}=400 fF

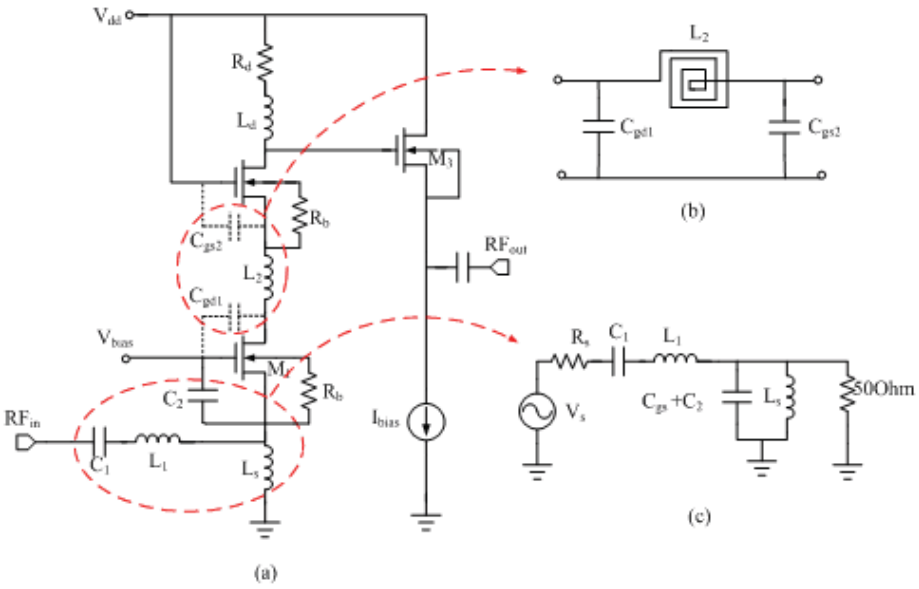

Fig. 1. Circuit schematics (a) Proposed UWB LNA (b) π-section LC network (c) Two-order band pass filter

B. π-section LC network

Flat gain over the entire bandwidth, is another important requirement of the UWB LNA design. However, the shunt of M_1's gate-drain parasitic capacitance, C_{gd1}, and M_2's gate-source parasitic capacitance, C_{gs2}, provides an additional path for the RF signal current to the ground, which leads to power gain reduction especially for the high frequency band. In order to solve this problem, a π-section LC network technique is first adopted and proposed for our design. Fig. 1 (b) shows the circuit of the π-section LC network, which is formed by an inductor and the gate-source parasitic capacitances. The inductor L_2 provides gain peaking on higher frequency corner of pass-band and the inductor L_d provides gain peaking on lower frequency. The inductor L_2 compensate for the gain response from 6 GHz to 10 GHz as shown in Fig. 2 (b). This makes the in-band gain satisfied flat gain within a variation of $\pm$1 dB relative to the average.

C. Noise Figure

According the proposed circuit shown in Fig. 1 and after a lengthy derivation, the noise factor of the Common-Gate LNA is given by

$$F_{CG-LNA} = 1 + \frac{\gamma}{\alpha}\frac{1}{g_{m1}R_s}, \quad (1)$$

Where γ and α are bias-dependent parameters [1], and the induced gate

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noise is neglected.

From (1), the noise factor is decreased when g_{m1} increases, and the factor is equal to $1+\gamma/\alpha$ if the input is matched with $g_{m1}=1/R_s$. Since α s increased with the g_{m1}. It can be easily found that the larger bias resistor is, the smaller the noise factor is. Fig. 2 (c) shows that the noise figure (NF) is smaller when R_b=8 kOhm to compare with the case without R_b.

3 Simulation Results

In simulation, the TSMC 0.18 um CMOS 1P6M process, a low supply voltage of 1.5 V is chosen, and the total power consumption is 3.0 mW. In Fig. 2 (a), S11 and S22 versus signal frequency are illustrated. It is found that the input reflection S11 < -10.44 dB and output matching S22 < -12.05 dB in the range of 3.1∼10.6 GHz. The power gain (S21) is around 10.0∼12.4 dB. 3 dB bandwidth of the LNA is 7.8 GHz and is satisfied the need of UWB. The noise figure of the LNA is shown in Fig. 2 (c). It is found that the noise figure is at least less than 4.4 dB in 3.1∼10.6 GHz and its minimum value is 3.25 dB at 8.5 GHz. The simulation results also show that the input third-order-intercept points (IIP3s) are -1.7 dBm at 3 GHz, -4 dBm at 5 GHz, -3.97 dBm at 6 GHz, -4.5 dBm at 8 GHz, -6 dBm at 10 GHz.

The performance of the proposed LNA is summarized in Table I, with comparison to other recently published ultra-wideband LNAs' simulation results.

Table I. Summary of LNA performance and comparison with published LNA_s

Ref.	Tech.	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)
[2]	0.18um CMOS	2.3-9.2	<-9.9	9.3	4.0	-6.7*	9.0
[2]	0.18um CMOS	2.4-9.5	<-9.4	10.4	4.2	-8.8*	9.0
[3]	0.18um SiGe	0.1-11	<-12	8	2.9	-3.4#	21.6
[4]	0.18um CMOS	3.1-10.6	<-9	17.5	3.1	N/A	33.2
[5]	0.18um CMOS	2-10.1	<9.76	10.2	3.68	-1.0*	7.2
Our work	0.18um CMOS	3-10.6	<-10.4	12.4	3.25	-3.97*	3.1

4 Conclusions

In this paper, a low-voltage and low-power UWB LNA has been designed using a standard TSMC 0.18 um CMOS 1P6M technology. The design uses the common gate combined with band pass filters for the input matching network, which can easily to reduce parasitic capacitance effects of the transistors. The π-section LC network technique is also employed in the LNA to achieve a sufficient and flat gain. A bias resistor of large value is placed

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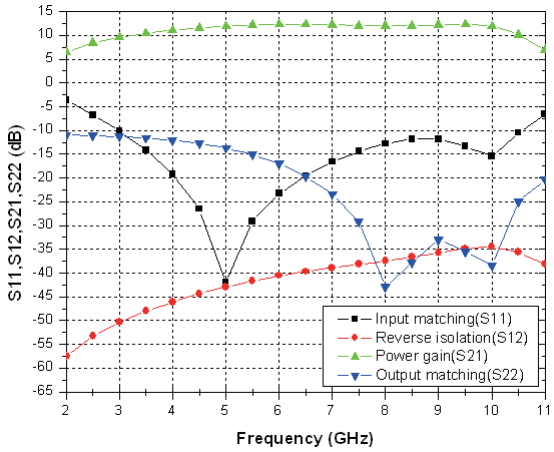
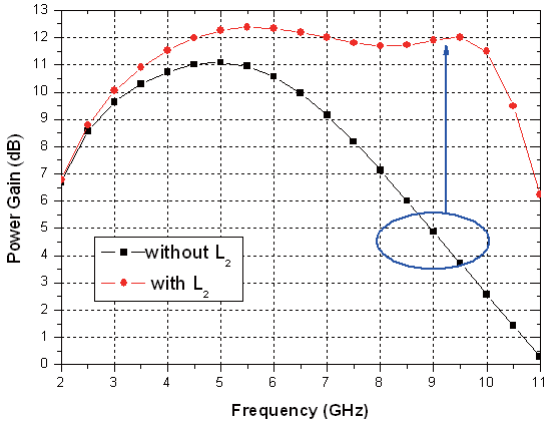


(a)



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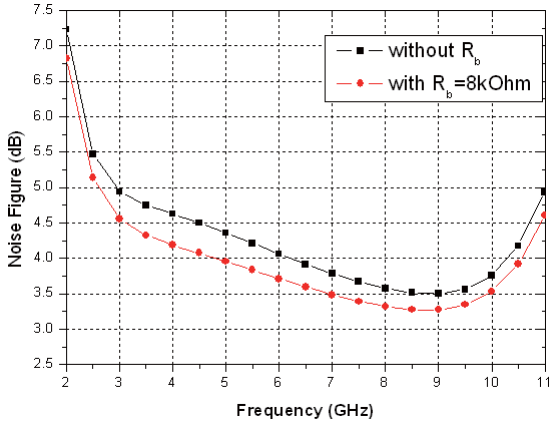

(c)

Fig. 2. Simulation results (a) S-parameters versus signal frequency; (b) Power gain versus signal frequency with L_2; and (c) Noise figure versus signal frequency with or without R_b.

between the source and the body nodes to prevent body effect and reduce noise.

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