

GaInP/GaAs HBT Sub-Harmonic Gilbert Mixers Using Stacked-LO and Leveled-LO Topologies

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Abstract—This paper discusses and demonstrates the most popular sub-harmonic Gilbert mixers in 2- μm GaInP/GaAs HBT technology. High two local oscillators (2LO)-to-RF isolation is important to alleviate the self-mixing problem of the sub-harmonic mixer. The demonstrated GaInP/GaAs HBT stacked-local oscillator (LO) mixer topology has achieved the best 2LO-to-RF isolation when compared with the previous literature. On the other hand, the leveled-LO sub-harmonic mixers have advantages in terms of the high speed and low dc supply voltage at the cost of much larger LO pumping power. Among all the structures, the bottom-LO sub-harmonic mixer has the lowest current consumption and the simplest circuit structure at the expense of the 2LO-to-RF isolation.

Index Terms—DC offset, GaInP/GaAs HBT, Gilbert mixer, self-mixing, sub-harmonic mixer, two local oscillators (2LO)-to-RF isolation.

I. INTRODUCTION

MORE AND more RF transceiver architectures are proposed because wireless communication applications grow rapidly. The heterodyne system has been used for many years; however, the off-chip image rejection surface acoustic wave (SAW) filter limits the circuit integration of the heterodyne system. The active or passive polyphase filters are used in the low-IF system to filter out the image signal, but the polyphase filters occupy too many valuable integrated circuit (IC) estates [1], [2]. The direct-conversion architecture is proposed to increase the integration level. The direct-conversion system eliminates many bulky and expensive off-chip components such as image-rejection and channel-select filters [3]. The RF frequency is arranged to be equal to the local oscillator (LO) frequency in the direct-conversion system and, thus, the image signal is the RF signal itself. As a result, the image-rejection filter is no longer necessary. The direct-conversion structure reduces the manufacturing cost and improves the circuit integration.

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Although the direct-conversion transceiver is highly integrated, many problems such as the dc offset, the LO leakage, the in-phase and quadrature (I/Q) signal mismatch, the even-order distortion, and the flicker noise arise. Most important of all, the LO frequency of the direct-conversion mixer is too close to the RF frequency so that the self-mixing problem caused by the LO leakage can degrade the transceiver performance. In order to prevent the self-mixing problem, sub-harmonic mixer topologies are proposed [4]–[8].

Conventionally, the passive harmonic mixers have been used for many years. The passive diode mixers using the nonlinear property of the diodes and these mixers have super gain compression point ($IP_{1\text{ dB}}$) at the cost of larger conversion loss and larger LO pumping power. On the other hand, sub-harmonic Gilbert mixers usually provide conversion gain at the cost of slower operation speed.

Three distinct sub-harmonic Gilbert mixers topologies based on the double-balanced structure have been proposed. The first topology is the three-level stacked-LO structure [4]–[6]. The working principle of the stacked Gilbert cell is to mix down the RF signal with the quadrature LO signals. On the contrary, the top-LO-configuration [7], and the bottom-LO-configuration [8] mixers are the leveled-LO sub-harmonic structures and their operations are based on the transistor's nonlinearity. In this paper, to the best of our knowledge, all three different types of the sub-harmonic Gilbert mixers are demonstrated using GaInP/GaAs HBT technology for the first time. The pros and cons of the sub-harmonic Gilbert mixers are discussed in Section II.

Ideally, the double balanced sub-harmonic mixer can totally eliminate the two local oscillators (2LO) leakage; however, the 2LO leakage occurs when nonideal effects such as circuit mismatches and the imperfections of the LO signal take place. In addition, the self-mixing problem caused by the 2LO leakage is more pronounced through the substrate coupling. The isolation properties can be improved using the deep N -well in the advance CMOS technologies [9] and the deep trench isolation in the SiGe bipolar technology [10]. Compared with the silicon substrate, the GaInP/GaAs HBT technology possesses a perfect semi-insulating substrate and, thus, the high-frequency 2LO leakage signal cannot leak to the RF port through the GaAs substrate. Since the substrate coupling is eliminated in this study, the 2LO-to-RF isolation performances among the Gilbert sub-harmonic mixer topologies can be fairly investigated. According to our experimental results, the stacked-LO sub-harmonic mixer is the best topology to achieve the highest 2LO-to-RF isolation.

It is easy to generate accurate quadrature signals in the GaInP/GaAs HBT technology. Almost all of the published

sub-harmonic mixers were fabricated on lossy silicon substrates [5]–[8]. The effectiveness of the quadrature signals is limited by the fabrication variation and the silicon substrate parasitic effect. However, the LO quadrature generator, which is often a polyphase filter [1], can be implemented precisely using GaInP/GaAs HBT technology because of the accurate thin-film resistors with 50- Ω sheet resistance, the 0.36-fF/ μm^2 metal–insulator–metal (MIM) Si_3N_4 capacitors, and the semi-insulating GaAs substrate. It is noticed that a capacitor in the standard silicon process has a smaller area and, thus, suffers more from fabrication variation because of the 1-fF/ μm^2 MIM capacitor employed in the silicon process.

The resistor has been widely used in the advance silicon technology, but the process variation is typically larger than 20%. For instance, the typical sheet resistance of the P^+ -poly resistor without silicide is 311 Ω per square with 20% error for the 0.18- μm CMOS technology. Although the sheet resistance of the P^+ -poly resistor with silicide is 7.8 Ω per square and the low resistance is adequate to implement the quadrature generator, the typical process variation of this on-chip resistor is approximately 30%. On the other hand, the thin-film resistors provided by the GaInP/GaAs HBT technology is accurately fabricated because the thickness of the film can be precisely *in situ* monitored during the fabrication. In addition, the semi-insulating substrate assures high- Q on-chip capacitor because the parasitic substrate capacitances and resistances are eliminated by the semi-insulating substrate.

The final advantage of the GaInP/GaAs HBT technology is its low $1/f$ noise corner. The CMOS transistor suffers from the $1/f$ noise because the inversion layer is located adjacent to the Si– SiO_2 interface. Many dangling bonds (traps) existing in this interface make the device $1/f$ noise worse. On the other hand, because the passivated ledge is employed over the extrinsic base surface [11], [12] and the DX center trap in the GaInP material is absent, the GaInP/GaAs HBT technology has low flicker noise. According to the previous literature [13]–[15], the $1/f$ noise dominates the low-frequency noise figure in the direct-conversion mixer. The HBT device in this study has very low $1/f$ noise and the measured slope of the mixer noise figure as a function of the IF frequency validates this characteristic.

II. SUB-HARMONIC GILBERT MIXERS DESIGNS

Here, the design tradeoffs among three sub-harmonic Gilbert mixers are discussed. Each sub-harmonic mixer topology has its own advantage. The stacked-LO structure [16] requires a smaller LO pumping power, but inevitably needs a larger dc supply voltage. The cascode stacked-LO structure makes the 2LO leakage very difficult to leak to the RF port and, thus, the best 2LO-to-RF isolation is achieved in this structure.

On the other hand, the leveled-LO mixers can be potentially operated at higher frequency, but needs a larger LO pumping power. When compared with the stacked-LO mixer, the leveled-LO mixers can operate at higher frequencies because this LO stage operates using the transistor's nonlinearity. The leveled-LO mixers (both the bottom-LO-configuration and the top-LO-configuration mixers) are likely to be faster than the stacked-LO mixer. The bottom-LO-configuration is the simplest topology, but it provides a smaller conversion gain

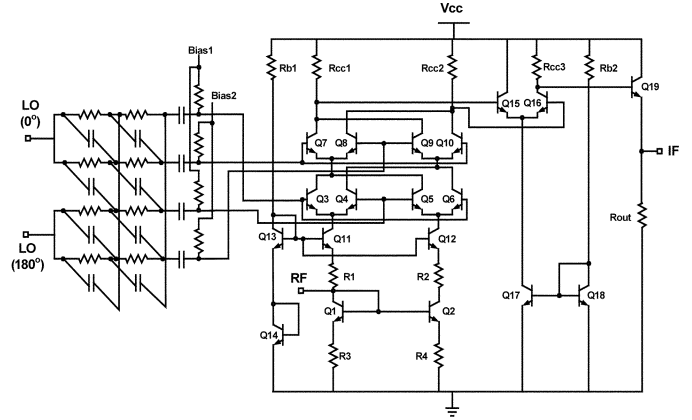


Fig. 1. Schematic of the 5.2-GHz three-level stacked-LO sub-harmonic GaInP/GaAs HBT Gilbert downconversion mixer.

and poor 2LO-to-RF isolation. The bottom-LO-configuration provides the minimal port-to-port isolation due to the circuit topology.

A. 5-GHz Three-Level Stacked-LO Sub-Harmonic Mixer Design

The stacked-LO mixer with two Gilbert cells consumes smaller current because the dc current is reused in the cascode structure. The stacked-LO sub-harmonic Gilbert mixer has two LO ports and one RF port, as shown in Fig. 1.

The bottom LO Gilbert cell transistors (Q_3 – Q_6) are fed by $I+$ and $I-$ LO input signals, while the top LO Gilbert cell transistors (Q_7 – Q_{10}) are fed by $Q+$ and $Q-$ LO input signals. If the I -phase and Q -phase LO signals are, respectively, defined as $\cos \omega_{\text{LO}} t$ and $\sin \omega_{\text{LO}} t$, the equivalent LO signals can be determined as follows:

$$\cos \omega_{\text{LO}} t \cdot \sin \omega_{\text{LO}} t = \frac{1}{2} \sin 2\omega_{\text{LO}} t. \quad (1)$$

Hence, the down-converted IF output frequency of the stacked-LO Gilbert mixer is the difference of the RF and 2LO frequencies. This topology with two stacked HBT-type Gilbert cells only needs very small LO pumping power when compared with the CMOS technologies. Since the transconductance of the HBT is an exponential function of the base–emitter voltage, the current in the LO Gilbert cell can be commutated by the small twist voltage on the order of several thermal voltage V_T .

The stacked-LO cell actually provides a composite switching function, and the simplified stacked-LO sub-harmonic mixer is shown in Fig. 2(a). The switching function of the top and bottom Gilbert cells in Fig. 2(b) are expressed as $S_1(t)$ and $S_2(t)$, respectively. If the signal $S_1(t)$ is behind $S_2(t)$ by a quarter period, the composite switching function represented as $S(t)$ is the exclusive OR function of $S_1(t)$ and $S_2(t)$. As shown in Fig. 2(b), the stacked-LO cell has a switching function $S(t)$, whose switching frequency is doubled. The corresponding paths in the composite switching half-periods A–D are drawn in Fig. 2(a) and only half of the switching paths are drawn for simplicity.

The stacked-LO Gilbert mixer requires quadrature LO signals and, thus, a two-section passive polyphase filter is employed to

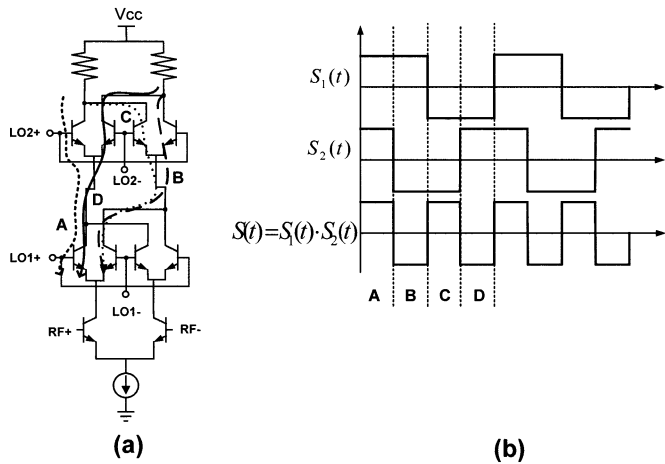


Fig. 2. (a) Simplified schematic of the three-level stacked-LO mixer. (b) Timing diagram of the stacked-LO Gilbert cells.

generate the accurate LO signals. The LO stages are stacked and biased at the different dc levels; hence, four dc blocking capacitors of 2 pF and biasing resistors of 3 k Ω are used in the top and bottom LO stages, as illustrated in Fig. 1.

The common-emitter transistor Q_2 , the common-base transistor Q_{11} , and the resistors R_1 – R_4 form the single-to-differential input stage, when Q_1 and Q_2 are constructed as a current mirror (or the micromixer) [17], [18]. The common-base transistor Q_{11} possesses a good frequency response, and the micromixer topology achieves the impedance matching at the RF input port. Thus, the chip area is saved. An output buffer consisting of an asymmetric differential amplifier and a common-collector output stage are incorporated to combine the IF output differential signals and to perform the output impedance matching.

B. 10-GHz Leveled-LO Sub-Harmonic Mixer Design

The leveled-LO sub-harmonic mixer is an appropriate topology for the high-frequency and low-voltage mixer design. Fig. 3(a) and (b) shows the top-LO-configured leveled-LO mixer [7] and the bottom-LO-configured leveled-LO mixer [8]. By feeding LO signals with proper phases, the even harmonic leveled-LO structure can be employed to commutate RF currents at the rate of 2LO frequency [7]. Compared with the stacked-LO sub-harmonic mixer, the leveled-LO structure uses the transistor's nonlinearity. The 2- μm GaInP/GaAs HBT transistor employed in this study has a maximum f_T of 40 GHz (when the current density is 0.2 mA/ μm^2) and BV_{CEO} of 13 V.

When a step voltage function is stimulated at the base-emitter terminal, the collector output current is generated after a phenomenological time delay τ . The time delay τ was employed in the linear model in the literature [19], [20]. In other words, the I – V characteristic transfer function should be expressed in terms of V_{BE} , V_{CE} , and τ . The output collector current follows the terminal base-emitter and collector-emitter voltages in an adiabatic way only if the operating radian frequency is much less than the reciprocal of the time delay τ . In general, active circuits operate much slower than the time delay τ , which is normally on the order of one-third of the transistor transit-time delay

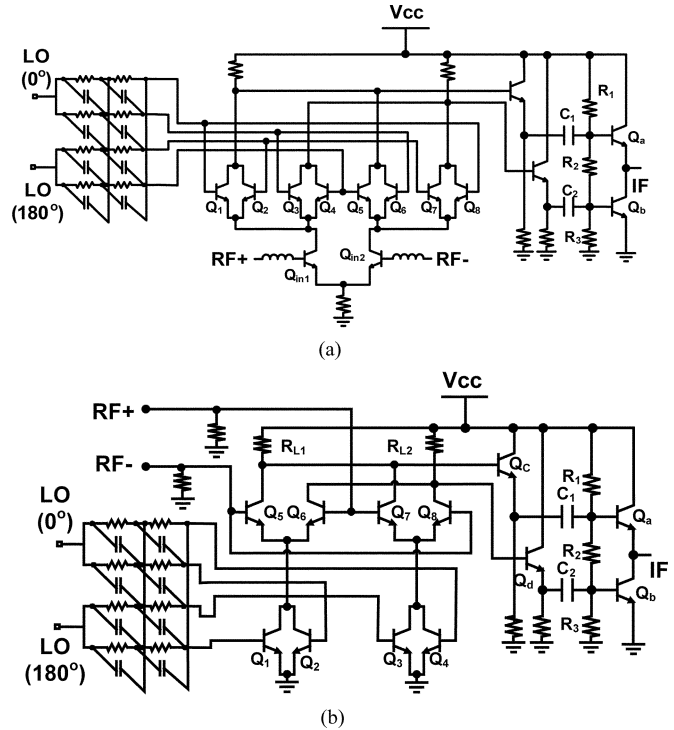


Fig. 3. Schematics of the: (a) top-LO-configured and (b) bottom-LO-configured leveled-LO sub-harmonic mixers.

[19], [20]. Therefore, the transit-time cutoff frequency f_T is still a good practical indication to judge whether the quasi-static model is valid for the second harmonic frequency or not.

The stacked-LO mixer basically trades the head room with higher 2LO-to-RF isolation. Since the stacked-LO topology has smaller head room, the reused biasing current of the LO cell and the RF input stage cannot be very large. On the other hand, there are fewer transistor levels stacked together in the leveled-LO topology and, thus, the biasing current can be larger. In other words, the level-LO topology operates at higher transit time cutoff frequency than the stacked-LO topology does.

1) *Operation of Leveled-LO Sub-Harmonic Stage:* An HBT transistor is a nonlinear device with exponential dependence between the collector current and the base-emitter voltage. The top-LO-configuration is shown in Fig. 3(a). The emitter-coupled pairs consisting of transistor pairs Q_1 – Q_2 to Q_7 – Q_8 forms the leveled-LO cell when their collectors are connected together. If 0° and 180° differential input signals are injected into the leveled-LO Q_1 – Q_2 pair, the fundamental signals are eliminated by shorting the collectors of the differential pair and only the even harmonic currents appear at the collector nodes. Simultaneously, 90° and 270° LO signals are injected into the leveled-LO Q_5 – Q_6 pair to generate the 2LO signal that is out of phase to the 2LO signal generated by leveled-LO Q_1 – Q_2 pair. The transistor pairs Q_1 – Q_2 and Q_5 – Q_6 work together to provide perfect 2LO differential signals [7]. Consequently, this structure can be used for the sub-harmonic mixer, and these emitter-coupled leveled-LO pairs shown in Fig. 3(a) are able to double the LO frequency.

As shown in Fig. 3(a) and (b), the difference between these two types of leveled-LO mixers is the location of the LO cell.

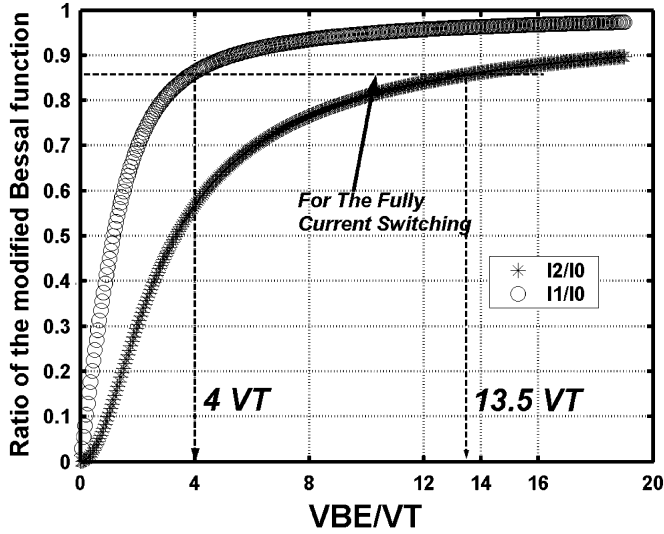


Fig. 4. Simulated ratio of the modified Bessel function as a function of the LO input voltage V_{BE} .

The top-LO-configuration mixer consists of four leveled-LO pairs (Q_1 – Q_8) above the RF input stage, while the bottom-LO-configuration mixer contains two leveled-LO cells under the RF input stage. The differential-quadrature LO signals of the double-balanced structure used in this study can be generated by a two-section polyphase filter.

In order to discuss the operation mechanism of the leveled-LO topology, the HBT exponential I – V transfer function can be expressed as the modified Bessel function [21], [22]. As shown in Fig. 3(a), the transistors Q_1 and Q_2 form a leveled-LO cell. The input LO signals of transistor Q_1 and Q_2 are defined as two out-of-phase signals $\hat{v} \cos \omega t$ and $-\hat{v} \cos \omega t$, respectively. The output collector currents can be described as follows:

$$I_{CQ1} = I_S e^{\frac{\hat{v} \cos \omega t}{V_T}} = I_S [I_0(x) + I_1(x) \cos \omega t + I_2(x) \cos 2\omega t + I_3(x) \cos 3\omega t + \dots] \quad (2a)$$

$$I_{CQ2} = I_S e^{-\frac{\hat{v} \cos \omega t}{V_T}} = I_S [I_0(x) - I_1(x) \cos \omega t + I_2(x) \cos 2\omega t - I_3(x) \cos 3\omega t + \dots] \quad (2b)$$

where x is equal to the ratio of $\frac{\hat{v}}{V_T}$. $I_n(x)$ in (2a) and (2b) is the modified Bessel function.

Since the collector nodes of the transistors Q_1 and Q_2 are tightened together, the overall collector current of the leveled-LO cell is the summation of I_{CQ1} and I_{CQ2} . It is

$$I_{\text{total}} = 2I_S [I_0(x) + I_2(x) \cos 2\omega t + \dots] \quad (3)$$

where $I_0(x)$ is the dc-bias component, and $I_2(x)$ is the 2LO current. Fig. 4 shows the simulated modified Bessel function. The generated 2LO signal $I_2(x)$ is normalized by the dc term $I_0(x)$, as shown in Fig. 4.

The fundamental signal $I_1(x)$ used in the conventional Gilbert mixer is cancelled in the leveled-LO cell. However, the term of $I_1(x)/I_0(x)$ is also simulated and normalized to be compared with $I_2(x)/I_0(x)$. Generally speaking, the conventional LO Gilbert cell begins to fully switch when the ratio of V_{BE}/V_T is equal to 4. According to Fig. 4, the value of $I_1(x)/I_0(x)$ is 0.8635, but that of $I_2(x)/I_0(x)$ is only 0.5682 when the ratio of V_{BE}/V_T is 4 (the value of fully commutation of the conventional Gilbert cell). Therefore, the x of $I_2(x)$ must be $13.5 V_T$ (extra 10.57-dBm pumping power) in order to fully steer the 2LO cell when using the $I_2(x)$ signals. In other words, the leveled-LO cell, which uses the $I_2(x)$ current for the LO switching, definitely requires a much larger LO pumping power than the fundamental active mixer does.

2) *RF and IF Stages*: A series inductor can easily achieve the input impedance matching of the top-LO-configuration mixer. On the contrary, the impedance matching at the RF input port is difficult to be achieved for the bottom-LO-configuration. The RF input stage of the bottom-LO-configuration is above the leveled-LO cell shown in Fig. 3(b). For the RF stage, the emitter is in series with a high resistance caused by the leveled-LO stage. Large inductance and capacitance are required to match the high input impedance of the RF port. As a result, a brute force matching resistor is shunt at the RF input port to save the chip area at the cost of worse noise figure and smaller conversion gain.

In our study, the IF output has a bandwidth of several hundreds megahertz. Since the leveled-LO sub-harmonic mixer is designed for a wider IF output bandwidth, the differential amplifier is not fast enough. As shown in Fig. 3(a) and (b), a unity gain output buffer consisting of a common-collector transistor Q_a and a common-emitter transistor Q_b preserves the isolation properties of the differential signals in a double-balanced mixer structure and simultaneously drives the spectrum analyzer. Two dc blocking capacitors of 8.1 pF are incorporated to bias the output stage here. Practically, a larger blocking capacitor is able to diminish the dc offset to push the lower boundary of the IF bandwidth in a direct-conversion receiver.

Neglecting the substrate leakage, the bottom-LO-configuration inevitably has poor 2LO-to-RF isolation when compared with the top-LO-configuration. Any 2LO leakage power appearing at the collector of the LO transistors (Q_1 – Q_4) easily leaks to the base node of the RF transistors (Q_5 – Q_8) in the bottom-LO-configuration. On the contrary, the 2LO leakage power is hard to leak to the RF port in the top-LO-configuration because the 2LO leakage power has to pass through more transistors to the RF node (from the collector node of LO transistors (Q_1 – Q_8) to the base node of the RF transistors). The cascode topology in the top-LO configuration decreases the signal leakage at the cost of the circuit complexity, and larger biasing currents.

The head room problem limits the biasing current in the demonstrated mixers. The emitter areas of the transistors for the stacked-LO sub-harmonic are all $2 \times 6 \mu\text{m}^2$ excluding the transistors used in the current source and the output buffer. The transistor sizes of the top-LO mixer cores (Q_1 – Q_8) are $2 \times 2 \mu\text{m}^2$, while the sizes of the transistors Q_5 – Q_8 and Q_1 – Q_4 in the bottom-LO mixer cores are $2 \times 2 \mu\text{m}^2$ and $2 \times 4 \mu\text{m}^2$,

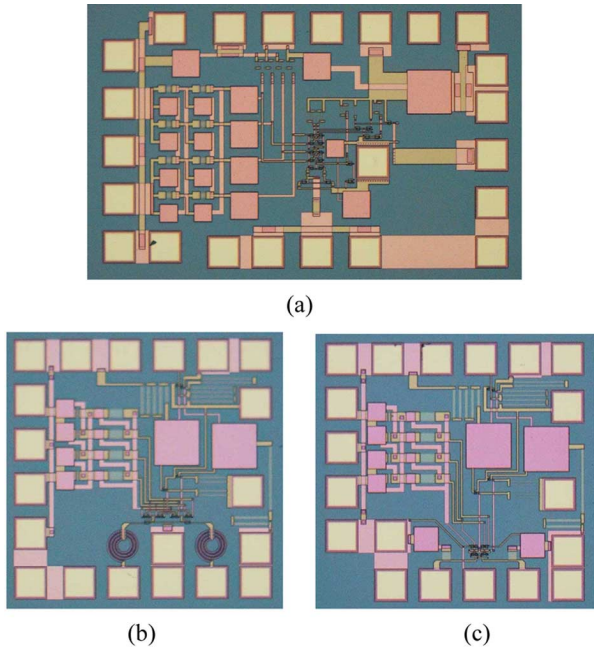


Fig. 5. Die photographs of the: (a) 5.2-GHz stacked-LO sub-harmonic mixer, (b) 10-GHz top-LO-configured sub-harmonic mixer, and (c) 10-GHz bottom-LO-configured sub-harmonic mixer. (a) Stacked-LO configuration. (b) Top-LO configuration. (c) Bottom-LO configuration.

respectively. The device sizes of the mixer core are chosen for the optimal transistor cutoff frequency f_T . The knee voltage of the HBT is around 0.6 V, and the emitter-collector voltages in our study are well designed to prevent the waveform clippings.

III. MEASUREMENT RESULTS

The die photograph of the 5.004-GHz three-level stacked-LO sub-harmonic Gilbert mixer demonstrated in a 2- μm GaInP/GaAs HBT is shown in Fig. 5(a). The LO and IF frequencies are 2.6 GHz and 400 kHz. The emitter areas of the GaInP/GaAs HBTs are 2 $\mu\text{m} \times 6 \mu\text{m}$ for the mixer core and 3 $\mu\text{m} \times 9 \mu\text{m}$ for the output buffer. The dc power supply is 3.3 V and the current consumption is only 4 mA including the output buffer. The die size including probing pads is 1 \times 1.5 mm².

The die photographs of the 10-GHz top-LO-configured and bottom-LO-configured mixers using the same technology are shown in Fig. 5(b) and (c), respectively. The LO and IF frequencies are 5 GHz and 100 MHz. Their die sizes including probing pads are both 1 \times 1 mm². The chip sizes of the leveled-LO sub-harmonic mixers can be shrunk because of the smaller RC values of the polyphase filter in higher frequencies. As shown in Fig. 5(b) and (c), there are two dc blocking capacitors of 8.2 pF. The core current of the top-LO-configuration mixer and the bottom-LO-configuration mixer are 2 and 0.8 mA, respectively. The circuit topology of the bottom-LO-configured mixer is the simplest and, thus, the dc current can be reduced.

An off-chip 180° hybrid and a pair of phase shifters are used to keep the phase accuracy; as a result, the intrinsic performance of the port-to-port isolation in a fully balanced Gilbert mixer is maintained. As shown in Fig. 6, the measured LO-to-IF, LO-to-RF, and 2LO-to-IF isolations are better than -40, -50, and -64 dB for the LO frequencies from 2.5992

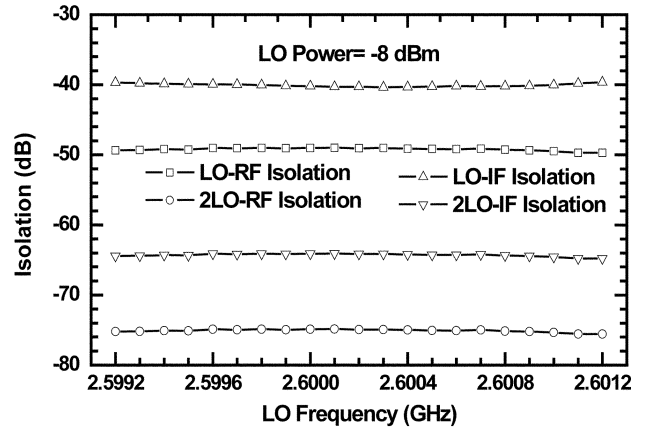


Fig. 6. Measured LO-IF, 2LO-IF, LO-RF, and 2LO-RF isolations as a function of the LO frequency for the stacked-LO sub-harmonic mixers.

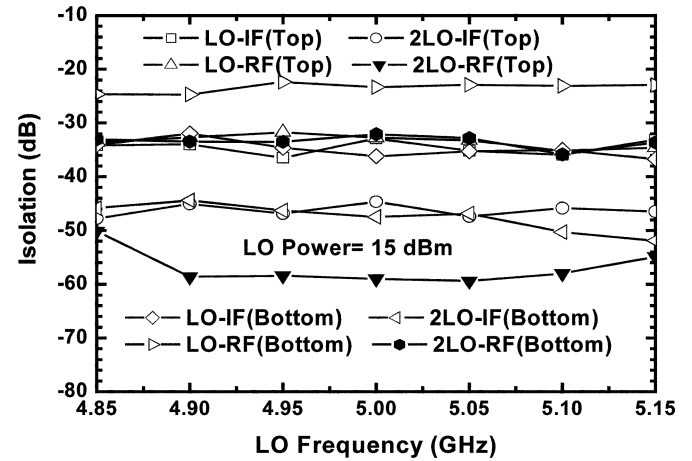


Fig. 7. Measured LO-IF, 2LO-IF, LO-RF, and 2LO-RF isolations as a function of LO frequency for the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

to 2.6012 GHz. The 2LO leakage appearing at the RF port is directly measured by the spectrum analyzer [4]. The measured 2LO-to-RF leakage power is less than -83 dBm when the LO input power equals -8 dBm and the LO frequency is 2.6 GHz. The experimental result shows that the stacked-LO sub-harmonic topology and the GaAs semi-insulating substrate effectively reduce the 2LO-to-RF leakages.

Fig. 7 illustrates the LO-to-IF, 2LO-to-IF, LO-to-RF, and 2LO-to-RF isolations as a function of LO frequency for the leveled-LO sub-harmonic mixers. The top-LO-configured mixer has -32-dB LO-to-RF isolation, -59-dB 2LO-to-RF isolation, -32-dB LO-to-IF isolation, and -46-dB 2LO-to-IF isolation, while the bottom-LO-configured counterpart has the -23-dB LO-to-RF isolation, -32-dB 2LO-to-RF isolation, -35-dB LO-to-IF isolation, and -48-dB 2LO-to-IF isolation.

The 2LO-to-RF isolation of the top-LO-configured mixer is better. The LO-to-RF isolation can be used to indicate the self-mixing problem for the CMOS passive mixer. Compared with the previous literature, the measured performance of the 2LO-to-RF isolations of the stacked-LO sub-harmonic mixers in our study is second to none when the RF frequency is around 5 GHz, as shown in the Table I.

TABLE I
2LO-TO-RF ISOLATIONS OF ACTIVE GILBERT SUB-HARMONIC MIXERS

	2LO-to-RF Isolation(dB)	RF frequency (G Hz)	Technology
Three-level (This Work)	75	5.2	2um GaInP/GaAs HBT
Top-LO (This Work)	59	10	2um GaInP/GaAs HBT
Bottom-LO (This Work)	32	10	2um GaInP/GaAs HBT
Ref[4]	70	2	0.5um SiGe HBT
Ref[6]	50	5-6	0.5um SiGe HBT
Ref[27]	64	5	0.13um CMOS
Ref[29]	35	5-6	0.5um SiGe HBT

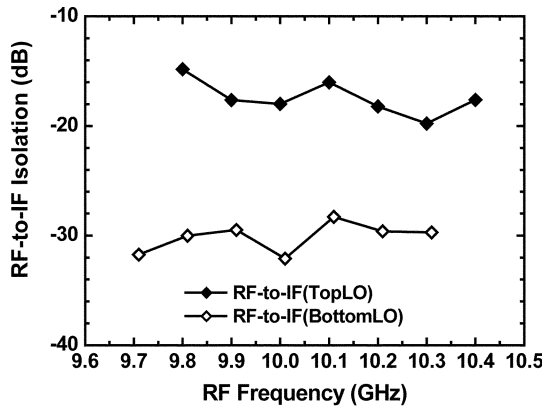


Fig. 8. RF-to-IF isolations as a function of RF frequency of the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

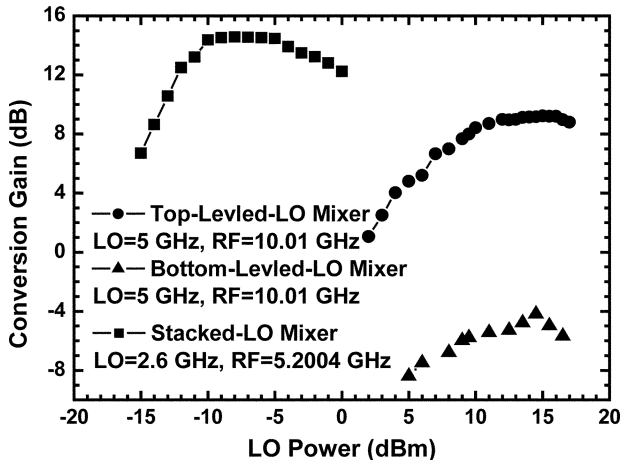


Fig. 9. Measured conversion gain as a function of the LO power of the stacked-LO and leveled-LO mixers.

The measured RF-to-IF isolation of the stacked-LO sub-harmonic mixer is -36 dB when the RF frequency is 5.2004 GHz. The RF-to-IF isolations of the top-LO and the bottom-LO sub-harmonic mixers as a function of RF frequency are shown in Fig. 8. The bottom-LO-configured mixer has better RF-to-IF isolation than the top-LO-configured one does.

Fig. 9 shows the measured conversion gain as a function of the LO power of all the sub-harmonic mixers. The conversion gain of the stacked-LO sub-harmonic mixer is 14.5 dB

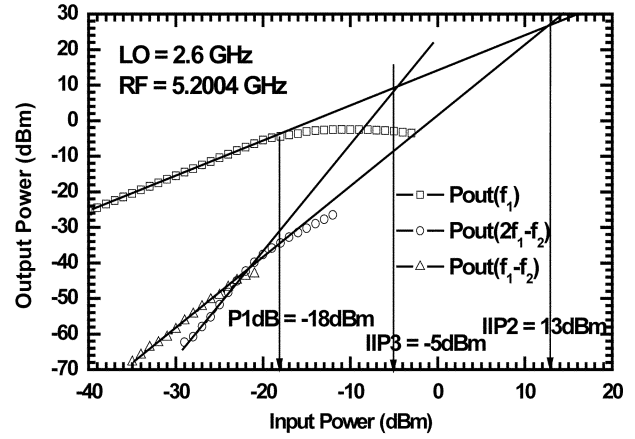


Fig. 10. Measured $IP_{1\text{ dB}}$ and IIP_3 of the stacked-LO sub-harmonic GaInP/GaAs HBT Gilbert downconversion mixer.

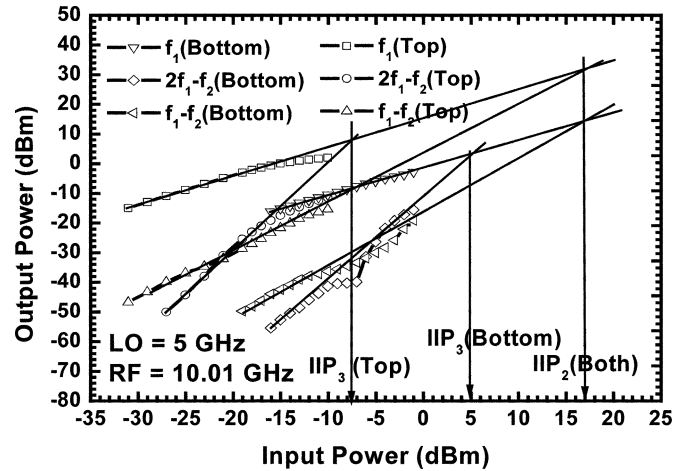


Fig. 11. $P_{1\text{ dB}}$, IIP_3 , and IIP_2 of the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

when LO power is larger than -10 dBm. As shown in Fig. 9, both leveled-LO sub-harmonic mixers require very large LO pumping powers. Compared with the stacked-LO structure, the LO pumping power of the leveled-LO mixer has to be 12 dBm for the optimal conversion gain, while the stacked-LO structure only requires -9 dBm.

As discussed in the Section II-B, the leveled-LO mixer inevitably needs more LO pumping powers for the LO current fully switching, and the reason is that the leveled-LO mixer operates using the transistor second-harmonic currents. The leveled-LO cell requires extra 10 -dBm LO power to perform the current commutation, as analyzed previously. In addition, the loss of the polyphase filter used in the stacked-LO mixer is 2.4 dB, while that of the leveled-LO mixer is approximately 6.5 dB according to our simulation. The measurement result is closed to our analysis as the polyphase loss is considered.

As shown in Fig. 10, the measured $IP_{1\text{ dB}}$, IIP_3 , and IIP_2 performances of the 5.2 -GHz GaInP/GaAs HBT stacked-LO sub-harmonic mixer are -18 , -5 , and 13 dBm, respectively. Fig. 11 shows the measured power performances of the leveled-LO mixer when the IF frequency is 100 MHz. The $IP_{1\text{ dB}}$, IIP_3 , and IIP_2 of the top-LO-configuration are -15 , -7.5 ,

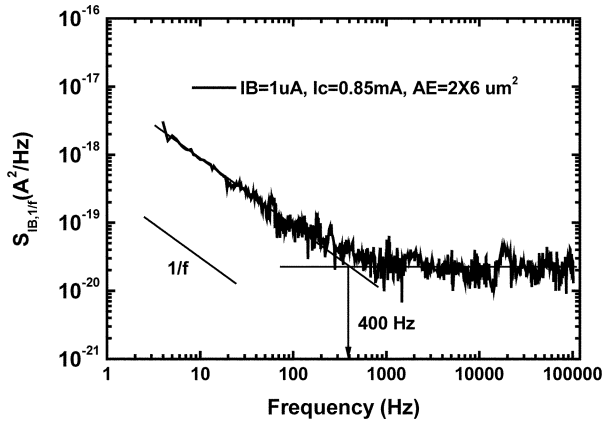


Fig. 12. Measured low-frequency noise spectrum of the GaInP/GaAs HBT ($AE = 2 \times 6 \mu\text{m}^2$, $IC = 0.85 \text{ mA}$, and $IB = 1 \mu\text{A}$).

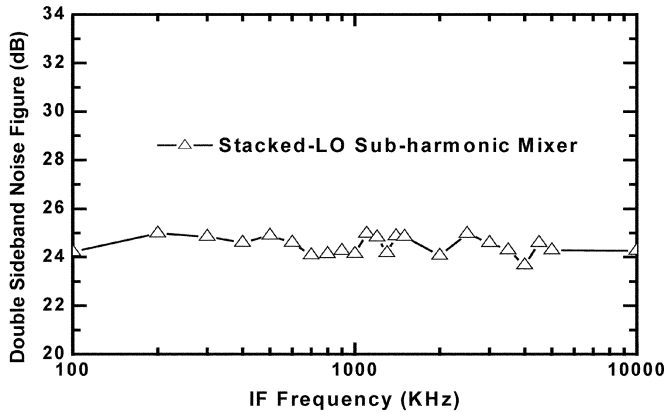


Fig. 13. Measured double-sideband noise figure of the stacked-LO sub-harmonic mixer from 100 kHz to 100 MHz.

and 17 dBm, respectively while the $IP_{1 \text{ dB}}$, IIP_3 , and IIP_2 of the bottom-LO-configuration are -4 , 5, and 17 dBm. The bottom-LO-configuration mixer attains a wider dynamic range because of the higher $IP_{1 \text{ dB}}$ and IP_3 .

The measured $1/f$ noise corner of the GaInP/GaAs HBT device used in the stacked-LO mixer is shown in Fig. 12. The $1/f$ noise corner can be as low as 400 Hz [11], [12]. As shown in Fig. 13, the measured double-sideband noise figure of the stacked-LO sub-harmonic mixer is 24 dB from 100 kHz to 100 MHz. The slope of the measured noise figure is kept constant without the appearance of the $1/f$ noise. According to previous works [13]–[15], the device $1/f$ noise and the parasitic capacitance in the current source dominate the low-frequency noise performance of the direct-conversion mixer.

Some excellent studies of direct-conversion mixers with low $1/f$ noise are achieved in the CMOS technologies. Reducing the noise pulses in LO switches [14], designing new LO switches [23], [24], and canceling the tail current parasitic capacitance with inductors [25] are useful techniques to improve the noise performance of CMOS direct-conversion mixers. The ledge-passivated GaInP/GaAs HBT devices naturally have better $1/f$ noise performance than the CMOS devices [11], [12]. Moreover, the semi-insulating GaAs substrate eliminates the parasitic capacitance at the tail current [13], [14] and, thus, the in-

direct noise no longer degrades the low-frequency noise performance of the GaInP/GaAs HBT mixers. The double-sideband noise figure in this study is not excellent owing to the extra resistors used in the micromixer input stage and the lacking of the noise figure optimization in our circuit. However, the GaInP/GaAs HBT technology potentially can be used to implement very high-performance direct-conversion mixers with low $1/f$ noise.

Recently, the passive CMOS mixers [23], [26]–[28] exhibit excellent noise performance. Although the CMOS device intrinsically has poor $1/f$ performance, the passive CMOS mixer can achieve excellent noise performance and the corner frequency of the noise figure is as low as 30 kHz. The passive CMOS mixer consists of a low noise input transconductance input stage, CMOS switches, and output filters. The low noise figure can be achieved because the low noise transconductance input stage [or the low noise amplifier (LNA)] effectively moderates the noise of the following stage [23], [27] and the large-sized CMOS switch [27], [28] prevents the $1/f$ noise by applying rail-to-rail square wave LO signals [26], [27]. Obviously, the heavily driven square-waved LO pumping signals cannot be employed in the conventional active Gilbert mixer. There might be many advantages using the CMOS passive mixer in terms of the low $1/f$ noise and high IIP_2 ; however, the circuit complexity and the area wasted by the compensation capacitors of the filters [26] are the tradeoffs of CMOS passive mixers.

The measured double-sideband noise figure of the top-LO-configuration sub-harmonic mixer is 24 dB, while the bottom-LO-configuration sub-harmonic mixer exhibits 22-dB double-sideband noise figure when the IF frequency is 50 MHz. Due to the output blocking capacitor, the noise figure is not measured at the low frequencies. The bottom-LO-configuration mixer using fewer transistors has a better double-sideband noise figure, even if the resistor for the input impedance matching may degrade the noise figure, as shown in Fig. 3(b).

The noise of the direct conversion mixer basically results from the LO switch and the RF input stage. Since the $1/f$ noise of the GaInP/GaAs HBT device is very small, the noise level is dominated by the RF input stage thermal noise. Our simulation shows a lower noise figure when compared with the experimental results. The discrepancy between the simulation and measurement are caused by the difficulties in modeling the noise parameters of the HBT device such as base access resistance in the Gummel–Poon model. Thus, the simulated noise might be underestimated. The contribution from the RF input stage transistor might be higher in the real circuit because of the inaccuracy in modeling the base access resistance. Table II summarizes the noise contribution of each device used in the active sub-harmonic mixers. For the stacked-LO topology, the micromixer input stage (R_1 , R_2 , R_4 , Q_1 , and Q_{11}) produces 51% noises. The RF input stage (Q_{in1} and Q_{in2}) of the top-LO configuration produces 48% noises. Finally, 88% of the noises in the bottom-LO sub-harmonic mixer are caused by the RF input stage (Q_5 – Q_8). A low noise input stage is important to improve the noise figure for all the sub-harmonic mixers.

The sub-harmonic mixer using top and bottom LO topologies have the conversion gain of 13 and 0 dB, as depicted in Fig. 14. Both mixers have approximately 300-MHz IF bandwidth. When

TABLE II
SIMULATED NOISE CONTRIBUTION OF EACH DEVICE
FOR THE ACTIVE SUB-HARMONIC MIXERS

Stacked-LO		Top-LO		Bottom-LO	
Q2	15%	Qin1	24%	Q5	22%
Q11	12%	Qin2	24%	Q6	22%
R4	8%	Q1	6%	Q7	22%
R1	8%	Q2	6%	Q8	22%
R2	8%	Q3	6%	RL1	2.6%
Q7	4%	Q4	6%	RL2	2.6%
Q8	4%	Q5	6%	Q1	1.4%
Q9	4%	Q6	6%	Q2	1.4%
Q10	4%	Q7	6%	Q3	1.4%
Rcc1	4%	Q8	6%	Q4	1.4%
Rcc2	4%	The rest	4%	The rest	1.2%
Q3	4%				
Q4	4%				
Q5	4%				
Q6	4%				
The rest	9%				

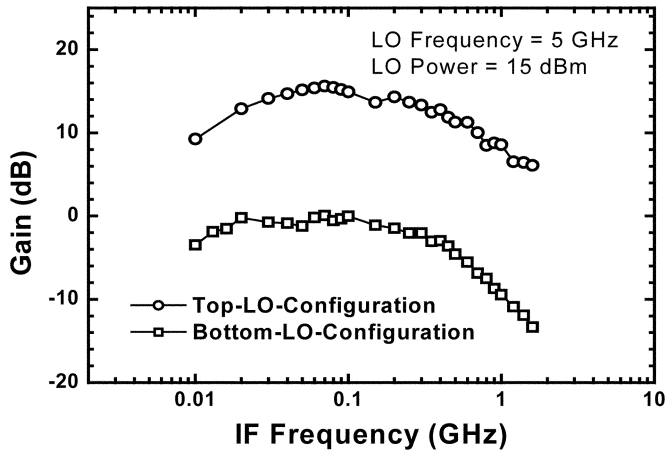


Fig. 14. Conversion gain as a function of the IF frequency of the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

the IF frequency is below 20 MHz, the conversion gain rolls off due to the on-chip dc blocking capacitors in the output buffer.

The return losses of all are shown in Fig. 15. The measured RF S_{11} and IF S_{22} of the stacked-LO mixer are better than -18 and -10 dB, respectively. The measured S_{11} of the bottom-LO-configured mixer is below 10 dB. The S_{11} of the top-LO-configured mixer has a notch at 10 GHz and it is below -10 dB from 8.2 to 12.5 GHz. The inductors used for the impedance matching in the top-LO configuration cause this notch of the RF input return loss. For the leveled-LO mixers, the RF inputs are differential. The experimental results of S_{11} are obtained by measuring one

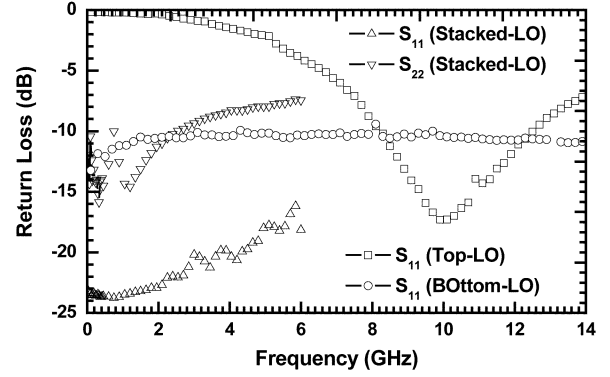


Fig. 15. Measured return loss of the stacked-LO, top-LO-configured, and bottom-LO-configured sub-harmonic mixers.

TABLE III
MEASURED PERFORMANCES

	Three-Level Stacked-LO	Top-LO- Configuration	Bottom-LO- Configuration
RF frequency (GHz)	5.2	10	10
Gain (dB)	14.5	13	0
2LO-to-RF Isolation (dB)	75	59	32
2LO-to-IF Isolation (dB)	64	46	48
LO-to-RF Isolation (dB)	50	32	23
LO-to-IF Isolation (dB)	40	32	35
RF-to-IF Isolation (dB)	36	18	30
IP1dB (dBm)	-18	-15	-4
IIP3 (dBm)	-5	-7.5	5
IIP2 (dBm)	13	17	17
Double Sideband Noise Figure (dB)	24	24	22
DC Current (mA)	4*	2	0.8

* Including the output buffer

of the RF differential ports when the other RF input port is terminated by a $50\text{-}\Omega$ load.

The measured performances of all three different types of the sub-harmonic Gilbert mixers demonstrated in this study are summarized in Table III.

IV. CONCLUSION

In this paper, three different types of Gilbert sub-harmonic mixers have been demonstrated using $2\text{-}\mu\text{m}$ GaInP/GaAs HBT technology. Since the GaAs semi-insulating substrate eliminates the substrate effect, the intrinsic performance of the 2LO-to-RF isolation can be investigated among these three different sub-harmonic mixer topologies. According to our experiment results and analysis, the stacked-LO sub-harmonic mixer is the best topology to achieve the highest 2LO-to-RF

isolation. A record-high 2LO-to-RF isolation is accomplished when RF frequency is around 5 GHz.

The design tradeoffs of these sub-harmonic topologies have been discussed in this paper. The stacked-LO sub-harmonic mixer can operate with the smallest LO pumping power at the cost of a higher dc voltage supply. On the other hand, the leveled-LO sub-harmonic mixers including the top-LO-configured and the bottom-LO-configured mixers can operate in higher frequencies. In addition, there are still some design tradeoffs in the two leveled-LO mixer topologies. The top-LO-configuration mixer has higher conversion gain and 2LO-to-RF isolation, but the bottom-LO-configuration mixer has advantage in terms of the power consumption, linearity, and RF-to-IF isolation.

The measured $1/f$ noise corner of the 2- μm GaInP/GaAs HBT device is approximately 400 Hz, as demonstrated in this paper. The measured slope of the low-frequency noise figure keeps constant from 100 kHz to 100 MHz, and the $1/f$ noise corner does not appear. The HBT device used in this study is adequate to achieve high-performance direct-conversion sub-harmonic mixer with a small low-frequency noise figure.

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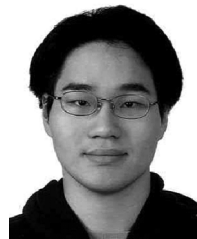
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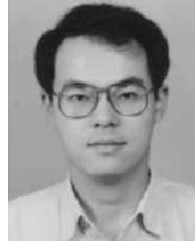
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