Characteristics of Self-Aligned Si/Ge T-Gate Poly-Si Thin-Film Transistors With High ON/OFF Current Ratio

Po-Yi Kuo, Tien-Sheng Chao, *Senior Member, IEEE*, Pei-Shan Hsieh, and Tan-Fu Lei, *Member, IEEE*

***Abstract*—In this paper, we have successfully developed and fabricated self-aligned Si/Ge T-gate poly-Si thin-film transistors (Si/Ge T-gate TFTs) with a thick gate oxide at the gate edges near the source and drain for the first time. The Si/Ge T-gate was formed by selective wet etching of Ge gate layer. The thick gate oxide layer at the gate edges and passivation oxide layer were deposited simultaneously in passivation process. The thick gate oxide at the gate edges effectively reduces the drain vertical and lateral electric fields without additional mask, lightly doped drain, spacer, or subgate bias. The Si/Ge T-gate TFTs not only reduce the OFF-state leakage current but also maintain a high ON-state current. Experimental results show that the Si/Ge T-gate TFTs have low OFF-state leakage currents, improved ON/OFF current ratio, and more saturated output characteristics compared with conventional TFTs.**

***Index Terms*—Germanium, ON/OFF current ratio, polycrystalline silicon thin-film transistors (poly-Si TFTs), self-aligned, Si/Ge T-gate.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) have been widely used in many potential applications including high-density flash memories, active-matrix organic light emitting diode, and active-matrix liquid crystal displays [1]–[4]. Poly-Si TFTs are considered to be promising devices for display system-on-panel applications [5]. However, the large OFF-state leakage current and device instability of poly-Si TFTs are hindrances to the high-performance and high-reliability circuit applications. It is well known that the dominant mechanism of the OFF-state leakage current is the field emission via grain boundary traps due to a high electric field in the drain depletion region. The leakage current is increased with increasing gate and drain voltages which enhance the field emission via grain boundary traps in the depletion region near the drain [6], [7]. In order to increase the reliability and reduce the leakage current, poly-Si TFTs with offset gated, lightly doped drain (LDD), gate-overlapped LDD, floating gate spacer, air cavity, or field-induced drain (FID) structures have been suggested to reduce the electric field near the drain [8]–[14].

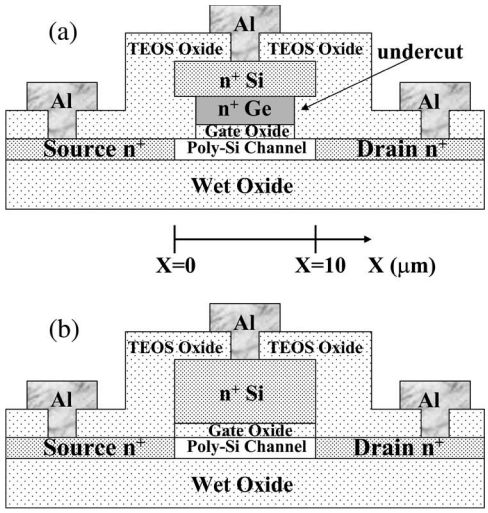

Fig. 1. Schematic cross-sectional device structures of (a) Si/Ge T-gate TFTs and (b) conventional TFTs.

In this paper, a novel self-aligned Si/Ge T-gate poly-Si TFT is proposed and demonstrated. The Si/Ge T-gate was formed by selective wet etching of Ge gate layer. The Ge regions etched at the gate edges were refilled by low-pressure chemical vapor deposition tetraethoxysilane (LPCVD TEOS) oxide in the passivation process. The thick gate oxide layer at the gate edges and the passivation oxide layer were deposited simultaneously in the passivation process. The thick gate oxide at the gate edges effectively reduces the drain vertical and lateral electric fields without additional mask, LDD, spacer, and subgate bias. The lateral electric field within the channel can be lowered by using the lateral selective etching of Ge within the gate stack at the gate edges without extra fabrication cost in the Si/Ge T-gate TFTs. The Si/Ge T-gate TFTs have a reduced OFF-state leakage current at negative voltages, an improved ON/OFF current ratio, and a smaller drain conductance in saturation due to a reduced impact ionization at the drain end of the channel compared with conventional TFTs.

II. Device Structure and Design

Fig. 1 shows the schematic cross-sectional device structures of [Fig. 1(a)] Si/Ge T-gate TFTs and [Fig. 1(b)] conventional

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TABLE I
EXPERIMENTAL SPLIT TABLE OF Si/Ge T-GATE TFTS AND CONVENTIONAL TFTS

Devices	TEOS Gate Oxide	Si / Ge Gate	undercut
Si / Ge $_{50nm}$ T-gate TFTs (400nm)	50nm	150nm / 50nm	400nm
Si / Ge $_{50nm}$ T-gate TFTs (800nm)		150nm / 50nm	800nm
Si / Ge$_{100nm}$ T-gate TFTs (400nm)		100nm / 100nm	400nm
Si / Ge$_{100nm}$ T-gate TFTs (800nm)		100nm / 100nm	800nm
Conventional TFTs		200nm / 0nm	

TFTs. Both devices have the same photomask gate length and perform the same source/drain (S/D) implantation condition. The experimental split table of Si/Ge T-gate TFTs and conventional TFTs is defined in Table I. In Si/Ge T-gate TFTs, the thickness of the thick gate oxide layer at the gate edges is controlled by the thickness of Ge gate layer (50 and 100 nm), and the Ge lateral undercut distances (400 and 800 nm) are controlled by the time of selective wet etching. For example, the Si/Ge$_{50\,nm}$ T-gate TFTs (400 nm) have a 150-nm/50-nm stacked Si/Ge gate layer and a 400-nm Ge lateral undercut distance. The total thickness of stacked Si/Ge gate layer is 200 nm for all devices.

The Si/Ge T-gate TFTs can reduce the vertical electric field near the drain due to the thick gate oxide layer at the gate edges [12]. The poly-Si region under thick gate oxide can be considered as an offset region, and the gate edge over the thick gate oxide serves as a field plate connected with the gate so that the proposed TFTs operate like FID TFTs except a subgate bias [13]. In the OFF-state, the lateral electric field near the drain can be reduced due to the thick gate oxide layer at the gate edges [12]. In the ON-state, a sufficient inversion layer can be induced by the thick gate-edge oxide near the source [14]. In order to demonstrate the reduction in drain lateral electric field in the Si/Ge T-gate TFTs, the electric fields in the TFTs were simulated by using a commercial 2-D numerical simulator for semiconductor devices. Fig. 2 shows the simulated lateral electric field distribution along the channel/gate oxide interface for conventional TFTs and Si/Ge T-gate TFTs with applied biases at [Fig. 2(a)] $V_G = 0$ V and $V_D = 15$ V, and at [Fig. 2(b)] $V_G = -10$ V and $V_D = 10$ V. The simulated result demonstrates that lateral electric field near the drain can be effectively reduced by the Si/Ge T-gate structure. The Si/Ge T-gate TFTs with 100-nm Ge gate layer have the lowest lateral electric field near the drain due to the thickest gate oxide at the gate edges [12].

III. EXPERIMENT

Fig. 3 shows the main fabrication process steps of Si/Ge T-gate TFTs. First, a 100-nm amorphous silicon (a-Si) layer was deposited by LPCVD at 550 °C on oxidized silicon wafers and then was crystallized by solid phase crystallization at

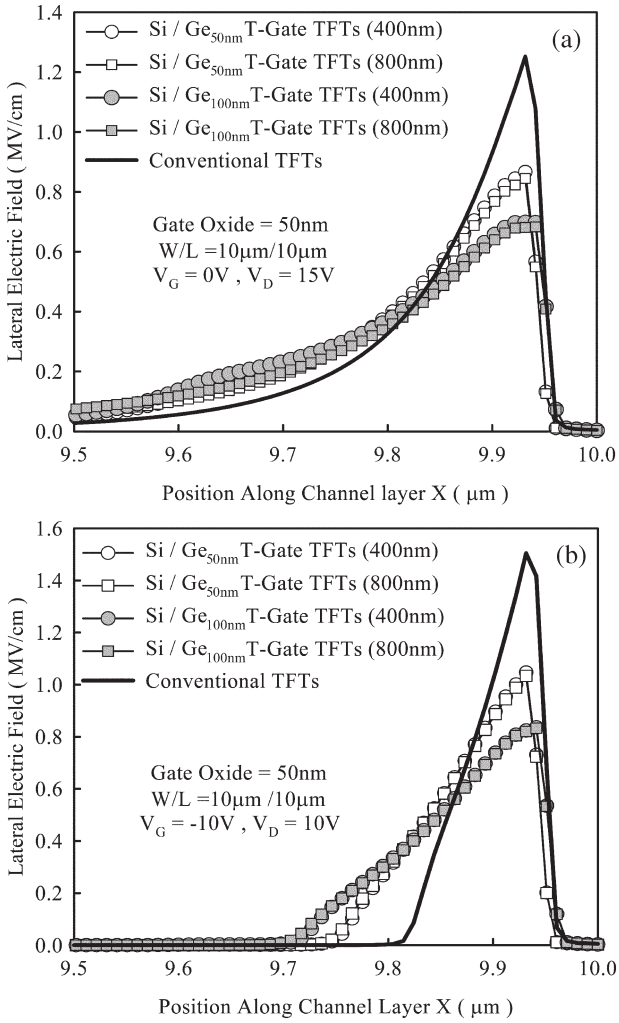

Fig. 2. Simulated lateral electric field distribution along the channel/gate oxide interface for conventional TFTs and Si/Ge T-gate TFTs with applied biases at (a) $V_G = 0$ V and $V_D = 15$ V and at (b) $V_G = -10$ V and $V_D = 10$ V.

600 °C for 24 h. After the patterning of the active region, a 50-nm TEOS gate oxide layer was deposited by LPCVD. Subsequently, a stacked a-Si/a-Ge gate layer was deposited by LPCVD at 550 °C/370 °C. The thickness of the thick gate oxide layer at the gate edges was controlled by the thickness of the Ge gate layer (50 and 100 nm). A phosphorus gate implantation with dose 5×10^{15} cm^{-2} and energy 60 keV was used to form the n^{+-} gate [Fig. 3(a)]. After defining the gate electrode, the Si/Ge T-gate was formed by selective wet etching ($H_2O : H_2O_2$ solution) of Ge gate layer at 75 °C. The Ge lateral undercut distances (400 and 800 nm) of Si/Ge T-gate were controlled by the time of wet etching. Then, the remaining oxide on the S/D region was removed by diluted HF. A self-aligned phosphorus implantation with dose 5×10^{15} cm^{-2} and energy 25 keV was used to form the n$^+$ S/D [Fig. 3(b)]. The Ge undercut regions were refilled by LPCVD TEOS oxide in the passivation process, and dopants were activated by furnace at 600 °C for 12 h. After contact and metallization processes [Fig. 3(c)], NH_3 plasma treatments were implemented after sintering at 400 °C for 30 min. Conventional TFTs with self-aligned n$^+$ S/D and TEOS passivation were also fabricated to serve as control ones.

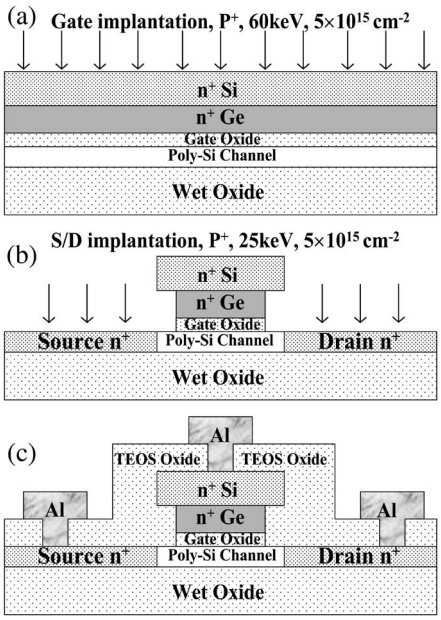

Fig. 3. Main fabrication process steps of Si/Ge T-gate TFTs.

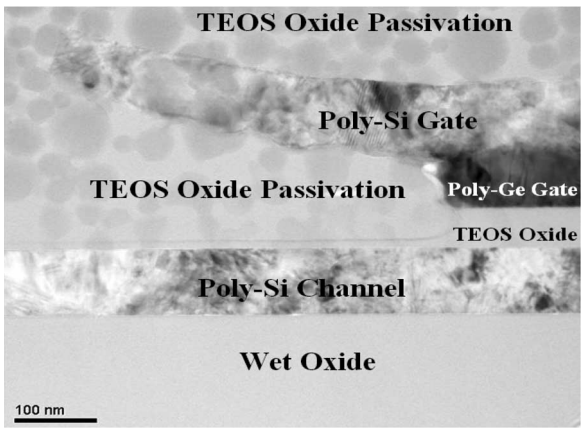

Fig. 4. Cross-sectional TEM microphotograph of Si/Ge T-gate TFTs.

IV. Results and Discussion

Fig. 4 shows the cross-sectional transmission electron microscopy (TEM) microphotograph of Si/Ge T-gate TFTs. The Si/Ge T-gate was successfully obtained on the gate oxide, and the interfacial oxide was not observed in the stacked Si/Ge interface. The Si and Ge gate layers were interalloyed between the stacked Si/Ge interface due to subsequent processes annealing. The undercut regions were fully refilled by LPCVD TEOS oxide in the passivation process, and the thickness of thick gate oxide at the gate edges was controlled by the thickness of the Ge gate layer. In Fig. 4, the thickness of the Ge gate layer is about 100 nm, and the Ge lateral undercut distance of Si/Ge T-gate is about 400 nm. The poly-Si at the gate edges was bent upward by subsequent process-induced thermal stresses. The bending poly-Si at the gate edges brings about gradual variation in the thickness of the gate oxide at the gate edges, and the thickest gate oxide is near the drain. The vertical and lateral electric fields at the drain can be effectively reduced by a thick gate

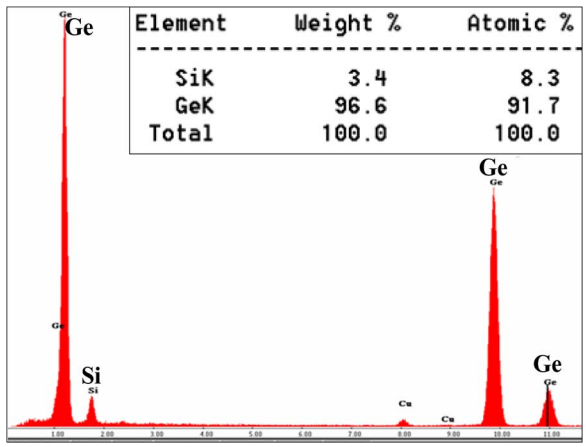

Fig. 5. Composition of pure Ge gate layer extracted from the energy dispersive X-ray spectrometer analysis.

oxide at the gate edges. In addition, the bending poly-Si at the gate edges can promote the refilling ability of LPCVD TEOS. Fig. 5 illustrates the composition of pure Ge gate layer extracted from the energy dispersive X-ray spectrometer analysis. The pure Ge gate layer of Si/Ge T-gate can be easily etched by the wet etching $H_2O : H_2O_2$ (100 : 1) solution at a low temperature of 75 °C. The etching rate is about 2.5 nm/s.

Fig. 6 exhibits the measured transfer characteristics of conventional TFTs and Si/Ge T-gate TFTs with [Fig. 6(a)] $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ and [Fig. 6(b)] $W/L = 10\ \mu\text{m}/5\ \mu\text{m}$. The OFF-state leakage currents of Si/Ge T-gate TFTs are significantly lower than those of conventional TFTs. This is because the lateral electric field near the drain can be effectively reduced by the Si/Ge T-gate structure. Since the thick gate oxide at the gate edges greatly suppresses the lateral drain electric field, the anomalous OFF-state leakage currents of poly-Si TFTs can be controlled by the thickness of the Ge gate layer and the Ge lateral undercut distances [14]. The $\text{Si/Ge}_{100\,\text{nm}}$ T-gate (800 nm) TFTs have the lowest OFF-state leakage currents in the Si/Ge T-gate TFTs. The ON-state currents of Si/Ge T-gate TFTs are slightly lower than those of conventional TFTs. A sufficient inversion layer can be induced by the thick gate-edge oxide near the source. For the Si/Ge T-gate TFTs, the ON-state currents are slightly reduced with increasing thickness of Ge gate layer and Ge lateral undercut distances. The $\text{Si/Ge}_{50\,\text{nm}}$ T-gate (400 nm) TFTs have the highest ON-state currents among all the Si/Ge T-gate TFTs.

Fig. 7 displays the measured OFF-state leakage currents of conventional TFTs and Si/Ge T-gate TFTs with $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ for different drain biases at $V_G = -10$ V. The OFF-state leakage currents of Si/Ge T-gate TFTs are significantly lower than those of conventional TFTs. The OFF-state leakage current is increased with increasing gate and drain voltages which enhance the field emission via grain boundary traps in the depletion region near the drain [6], [7]. In the Si/Ge T-gate TFTs, the lateral electric field near the drain can be greatly reduced due to the thick gate oxide layer at the gate edges, and the OFF-state leakage currents are greatly decreased with increasing thickness of the Ge gate layer and the Ge lateral undercut distances.

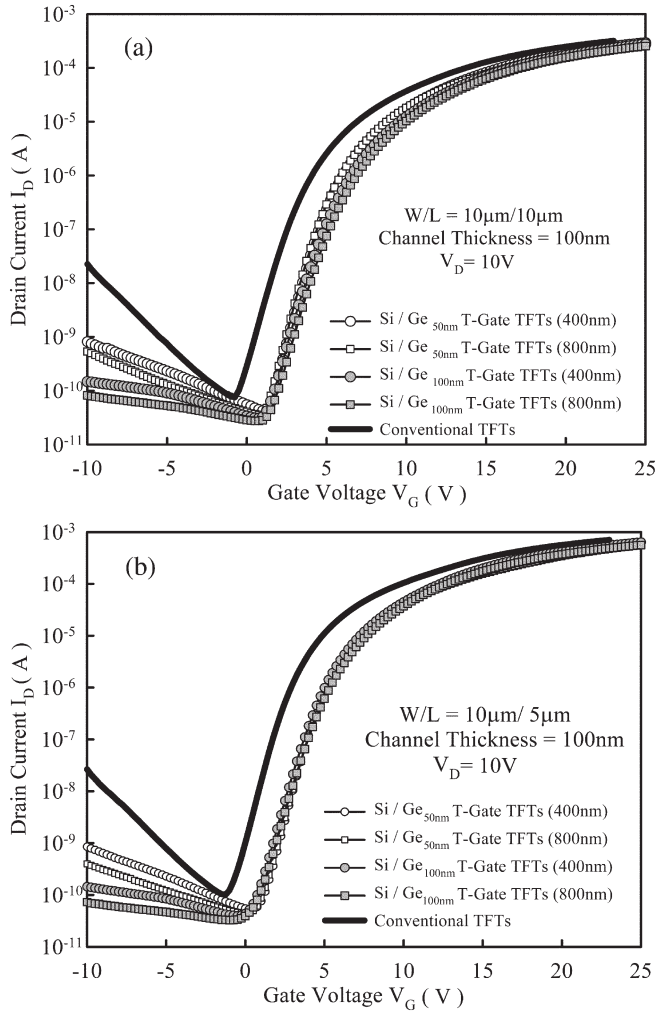

Fig. 6. Measured transfer characteristics of conventional TFTs and Si/Ge T-gate TFTs with (a) $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ and (b) $W/L = 10\ \mu\text{m}/5\ \mu\text{m}$.

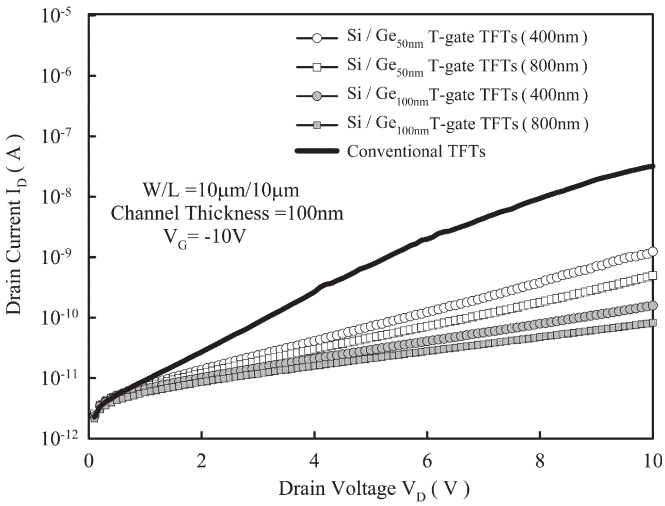

Fig. 7. Measured OFF-state leakage currents of conventional TFTs and Si/Ge T-gate TFTs with $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ for different drain biases at $V_{\text{G}} = -10$ V.

Fig. 8 illustrates the measured ON/OFF current ratio of conventional TFTs and Si/Ge T-gate TFTs with W = 10 μm and different channel length. The ON/OFF current ratio is defined as

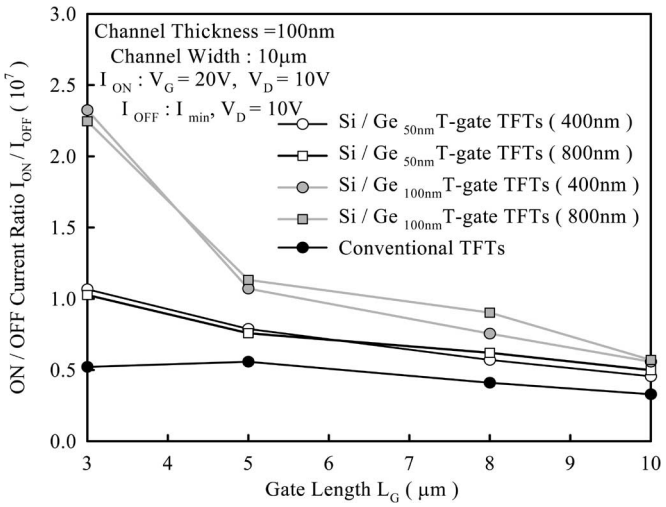

Fig. 8. Measured ON/OFF current ratio of conventional TFTs and Si/Ge T-gate TFTs with W = 10 m and different channel length. The ON/OFF current ratio is defined as the ratio of the ON-state current to the minimum OFF-state leakage current. The ON-state current is defined as drain–current (I_{D}) at $V_{\text{G}} = 20$ V and $V_{\text{DS}} = 10$ V, and the minimum OFF-state leakage current is defined as minimum drain–current (I_{min}) at $V_{\text{DS}} = 10$ V.

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The Si/Ge T-gate TFTs are different from conventional FID TFTs. The conventional FID TFTs need an additional subgate electrode, a large subgate bias, and an additional subgate mask compared with Si/Ge T-gate TFTs. In addition, the conventional FID TFTs have the farther separation of n^+ S/D junction compared with conventional TFTs. In the conventional FID TFTs with a SiO_2 interlayer, a typical subgate bias of more than 60 V is necessary to obtain a high ON/OFF current ratio [13]. The Si/Ge T-gate TFTs and conventional TFTs were fabricated with the same photomask gate length and the same S/D implantation condition. The Si/Ge T-gate TFTs and conventional TFTs have the identical position of S/D junction. The Si/Ge T-gate TFTs only need one gate electrode to obtain a high ON/OFF current ratio.

The output characteristics of conventional TFTs and Si/Ge T-gate TFTs with $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ are shown in Fig. 9. The Si/Ge T-gate TFTs have more saturated output characteristics compared with conventional TFTs. The kink current of Si/Ge T-gate TFTs is reduced considerably compared with that of conventional TFTs. The Si/Ge T-gate TFTs with 100-nm Ge gate layer have the most saturated output characteristics due to the lowest lateral electric field near the drain. The output

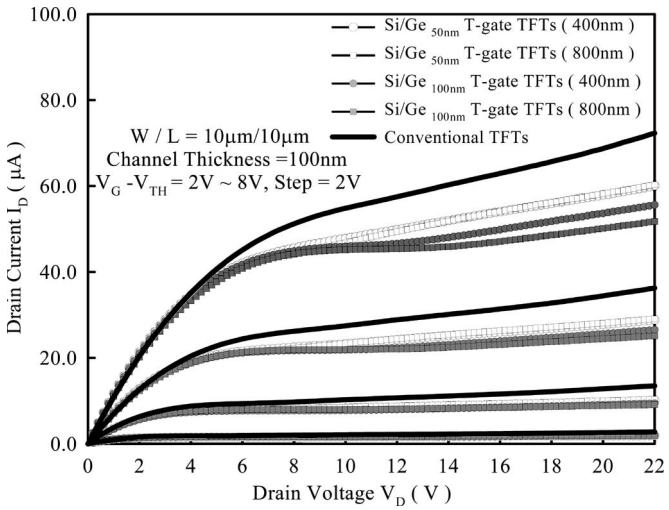

Fig. 9. Output characteristics of conventional TFTs and Si/Ge T-gate TFTs with $W/L = 10\ \mu m/10\ \mu m$.

characteristics exhibit an anomalous increase of current in the saturation regime, often called "kink" effect due to an analogy with silicon-on-insulator devices [15]–[17]. This phenomenon can be attributed to the floating-body effect [18] and the avalanche multiplication enhanced by grain boundary traps [16], particularly in n-channel TFTs. With increasing drain voltage, the added drain–current enhances impact ionization and parasitic bipolar junction transistor effect, which leads to a premature breakdown in return [18], [19]. Since the Si/Ge T-gate TFTs can reduce the vertical and lateral electric fields near the drain due to the thick gate oxide layer at the gate edges and the poly-Si region under thick gate oxide can be considered as an offset region [12], the impact ionization can be effectively reduced, and the avalanche multiplication enhanced by grain boundary traps can be suppressed by the Si/Ge T-gate TFTs [9]–[11].

V. Conclusion

In this paper, a self-aligned Si/Ge T-gate poly-Si TFTs effectively reduce the OFF-state leakage current while still maintaining the ON-state current compared with conventional TFTs. The stacked Si/Ge gate layers were successfully deposited by LPCVD. The thick gate oxide layer at the gate edges and passivation oxide layer were deposited simultaneously in passivation process. The thick gate oxide at the gate edges effectively reduces the vertical and lateral electric fields near the drain without additional mask, LDD, spacer, or subgate bias. The Si/Ge T-gate poly-Si TFTs are proved to be a very promising structure with low OFF-state leakage current, improved ON/OFF current ratio, and saturated output characteristics for display system-on-panel applications.

Acknowledgment

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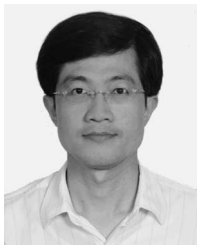

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